Tailored gamification: A review of literature

Gamification is increasingly becoming a pertinent aspect of any UI and UX design. However, a canonical dearth in research and application of gamification has been related to the role of individual differences in susceptibility to gamification and its varied designs. To address this gap, this study reviews the extant corpus of research on tailored gamification (42 studies). The findings of the review indicate that most studies on the field are mostly focused on user modeling for a future personalization, adaptation, or recommendation of game elements. This user model usually contains the users' preferences of play (i.e., player types), and is mostly applied in educational settings. The main contributions of this paper are a standardized terminology of the game elements used in tailored gamification, the discussion on the most suitable game elements for each users' characteristic, and a research agenda including dynamic modeling, exploring multiple characteristics simultaneously, and understanding the effects of other aspects of the interaction on user experience.

General information

Publication status: Published
MoE publication type: A2 Review article in a scientific journal
Organisations: Computing Sciences, Tampere University, Federal University of Rio Grande do Sul, State University of Santa Catarina
Contributors: Klock, A. C. T., Gasparini, I., Pimenta, M. S., Hamari, J.
Publication date: 1 Dec 2020
Peer-reviewed: Yes

Publication information

Journal: International Journal of Human Computer Studies
Volume: 144
Article number: 102495
ISSN (Print): 1071-5819
Original language: English
ASJC Scopus subject areas: Software, Human Factors and Ergonomics, Education, Engineering(all), Human-Computer Interaction, Hardware and Architecture
Keywords: Adaptation, Gamification, Personalization, Recommendation, Systematic review, Tailoring
Electronic versions:

1-s2.0-S1071581920300975-main
DOIs:

10.1016/j.ijhcs.2020.102495
URLs:

http://urn.fi/URN:NBN:fi:tuni-202007036316
Source: Scopus
Source ID: 85086582163
Research output: Contribution to journal › Review Article › Scientific › peer-review

The effect of challenge-based gamification on learning: An experiment in the context of statistics education

Gamification is increasingly employed in learning environments as a way to increase student motivation and consequent learning outcomes. However, while the research on the effectiveness of gamification in the context of education has been growing, there are blind spots regarding which types of gamification may be suitable for different educational contexts. This study investigates the effects of the challenge-based gamification on learning in the area of statistics education. We developed a gamification approach, called Horses for Courses, which is composed of main game design patterns related to the challenge-based gamification; points, levels, challenges and a leaderboard. Having conducted a 2 (read: yes vs. no) x 2 (gamification: yes vs. no) between-subject experiment, we present a quantitative analysis of the performance of 365 students from two different academic majors: Electrical and Computer Engineering (n=279), and Business Administration (n=86). The results of our experiments show that the challenge-based gamification had a positive impact on student learning compared to traditional teaching methods (compared to having no treatment and treatment involving reading exercises). The effect was larger for females or for students at the School of Electrical and Computer Engineering.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, National Technical University of Athens, Tampere University, Gamification Group
Contributors: Legaki, N. Z., Xi, N., Hamari, J., Karpouzis, K., Assimakopoulos, V.
Publication date: 1 Dec 2020
Peer-reviewed: Yes

Publication information

Journal: International Journal of Human Computer Studies
Volume: 144
Article number: 102496

ISSN (Print): 1071-5819
Original language: English
ASJC Scopus subject areas: Software, Human Factors and Ergonomics, Education, Engineering(all), Human-Computer Interaction, Hardware and Architecture
Keywords: Applications in education, Gamification, Human-Computer interface, Statistics education, Teaching forecasting
Electronic versions:
1-s2.0-S1071581920300987-main
DOIs:
10.1016/j.ijhcs.2020.102496
URLs:
http://urn.fi/URN:NBN:fi:tuni-202007036315
Source: Scopus
Source ID: 85086641706
Research output: Contribution to journal › Article › Scientific › peer-review

Some SonarQube issues have a significant but small effect on faults and changes. A large-scale empirical study

Context: Companies frequently invest effort to remove technical issues believed to impact software qualities, such as removing anti-patterns or coding styles violations. Objective: We aim to analyze the diffuseness of SonarQube issues in software systems and to assess their impact on code changes and fault-proneness, considering also their different types and severities. Methods: We conducted a case study among 33 Java projects from the Apache Software Foundation repository. Results: We analyzed 726 commits containing 27K faults and 12M changes in Java files. The projects violated 173 SonarQube rules generating more than 95K SonarQube issues in more than 200K classes. Classes not affected by SonarQube issues are less change-prone than affected ones, but the difference between the groups is small. Non-affected classes are slightly more change-prone than classes affected by SonarQube issues of type Code Smell or Security Vulnerability. As for fault-proneness, there is no difference between non-affected and affected classes. Moreover, we found incongruities in the type and severity assigned by SonarQube. Conclusion: Our result can be useful for practitioners to understand which SonarQube issues should be refactored and for researchers to bridge the missing gaps. Moreover, results can also support companies and tool vendors in identifying SonarQube issues as accurately as possible.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, LUT University
Contributors: Lenarduzzi, V., Saarimäki, N., Taibi, D.
Number of pages: 15
Publication date: Dec 2020
Peer-reviewed: Yes

Publication information

Journal: Journal of Systems and Software
Volume: 170
Article number: 110750
ISSN (Print): 0164-1212
Original language: English
ASJC Scopus subject areas: Software, Information Systems, Hardware and Architecture
Keywords: Change-proneness, Empirical study, Fault-proneness, SonarQube
DOIs:
10.1016/j.jss.2020.110750

Bibliographical note

EXT="Lenarduzzi, Valentina"
Source: Scopus
Source ID: 85087390369
Research output: Contribution to journal › Article › Scientific › peer-review

5G new radio evolution towards sub-THz communications

In this paper, the potential of extending 5G New Radio physical layer solutions to support communications in sub-THz frequencies is studied. More specifically, we introduce the status of third generation partnership project studies related to operation on frequencies beyond 52.6 GHz and note also the recent proposal on spectrum horizons provided by federal communications commission (FCC) related to experimental licenses on 95 GHz-3 THz frequency band. Then, we review the power amplifier (PA) efficiency and output power challenge together with the increased phase noise (PN) distortion effect in terms of the supported waveforms. As a practical example on the waveform and numerology design from the perspective of the PN robustness, link performance results using 90 GHz carrier frequency are provided. The numerical results demonstrate that new, higher subcarrier spacings are required to support high throughput, which requires larger

changes in the physical layer design. It is also observed that new phase-tracking reference signal designs are required to make the system robust against PN. The results illustrate that single-carrier frequency division multiple access is significantly more robust against PN and can provide clearly larger PA output power than cyclic-prefix orthogonal frequency division multiplexing, and is therefore a highly potential waveform for sub-THz communications.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Research group: Wireless Communications and Positioning, Bell Labs
Contributors: Tervo, O., Levanen, T., Pajukoski, K., Hulkkonen, J., Wainio, P., Valkama, M.
Number of pages: 6
Publication date: 1 Mar 2020

Host publication information
Title of host publication: 2nd 6G Wireless Summit 2020 : Gain Edge for the 6G Era, 6G SUMMIT 2020
Publisher: IEEE
ISBN (Electronic): 9781728160474
ASJC Scopus subject areas: Artificial Intelligence, Hardware and Architecture, Signal Processing, Safety, Risk, Reliability and Quality, Computer Networks and Communications, Instrumentation
Keywords: 5G New Radio, 5G NR, Beyond 5G, DFT-s-OFDM, numerology, OFDM, Phase noise, PHY, physical layer, PN , PTRS, SC-FDMA, Spectrum availability, Sub-THz
DOIs:

10.1109/6GSUMMIT49458.2020.9083807
Source: Scopus
Source ID: 85086306147
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Serverless: What it Is, What to Do and What Not to Do
Serverless, the new buzzword, has been gaining a lot of attention from the developers and industry. Cloud vendors such as AWS and Microsoft have hyped the architecture almost everywhere, from practitioners' conferences to local events, to blog posts. In this work, we introduce serverless functions (also known as Function-as-a-Service or FaaS), together with on bad practices experienced by practitioners, members of the Tampere Serverless Meetup group.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Gofore Plc
Contributors: Nupponen, J., Taibi, D.
Number of pages: 2
Pages: 49-50
Publication date: 1 Mar 2020

Host publication information
Title of host publication: 2020 IEEE International Conference on Software Architecture Companion, ICSA-C 2020
Publisher: IEEE
ISBN (Electronic): 9781728174150
ASJC Scopus subject areas: Computer Science Applications, Hardware and Architecture, Software, Information Systems and Management
Keywords: FaaS, Function-as-a-service, Serverless
DOIs:

10.1109/ICSA-C50368.2020.00016
Source: Scopus
Source ID: 85085749334
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

A custom processor for protocol-independent packet parsing
Networking devices such as switches and routers have traditionally had fixed functionality. They have the logic for the union of network protocols matching the application and market segment for which they have been designed. Possibility of adding new functionality is limited. One of the aims of Software Defined Networking is to make packet processing devices programmable. This provides for innovation and rapid deployment of novel networking protocols. The first step in processing of packets is packet parsing. In this paper, we present a custom processor for packet parsing. The parser is protocol-independent and can be programmed to parse any sequence of headers. It does so without the use of a Ternary Content Addressable Memory. As a result, the area and power consumption are noticeably smaller than in the state of the art. Moreover, its output is the same as that of the parser used in the Reconfigurable Match Tables (RMT). With an area no more than that of parsers in the RMT architecture, it sustains aggregate throughput of 3.4 Tbps in the worst case which

is an improvement by a factor of 5.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Electrical Engineering, Research area: Computer engineering, University of Bologna
Contributors: Zolfaghari, H., Rossi, D., Nurmi, J.
Number of pages: 11
Publication date: 1 Feb 2020
Peer-reviewed: Yes
Early online date: 2019

Publication information
Journal: Microprocessors and Microsystems
Volume: 72
ISSN (Print): 0141-9331
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture, Computer Networks and Communications, Artificial Intelligence
Keywords: Advanced program control, Packet parsing, Programmable data plane, Software defined networking
Electronic versions:

A Custom Processor for Protocol-Independent Packet Parsing
DOIs:

10.1016/j.micpro.2019.102910
URLs:

http://urn.fi/URN:NBN:fi:tuni-202001221463
Source: Scopus
Source ID: 85074246120
Research output: Contribution to journal › Article › Scientific › peer-review

Are SonarQube Rules Inducing Bugs?
The popularity of tools for analyzing Technical Debt, and particularly the popularity of SonarQube, is increasing rapidly. SonarQube proposes a set of coding rules, which represent something wrong in the code that will soon be reflected in a fault or will increase maintenance effort. However, our local companies were not confident in the usefulness of the rules proposed by SonarQube and contracted us to investigate the fault-proneness of these rules. In this work we aim at understanding which SonarQube rules are actually fault-prone and to understand which machine learning models can be adopted to accurately identify fault-prone rules. We designed and conducted an empirical study on 21 well-known mature open-source projects. We applied the SZZ algorithm to label the fault-inducing commits. We analyzed the fault-proneness by comparing the classification power of seven machine learning models. Among the 202 rules defined for Java by SonarQube, only 25 can be considered to have relatively low fault-proneness. Moreover, violations considered as 'bugs' by SonarQube were generally not fault-prone and, consequently, the fault-prediction power of the model proposed by SonarQube is extremely low. The rules applied by SonarQube for calculating technical debt should be thoroughly investigated and their harmfulness needs to be further confirmed. Therefore, companies should carefully consider which rules they really need to apply, especially if their goal is to reduce fault-proneness.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Lappeenranta University of Technology
Contributors: Lenarduzzi, V., Lomio, F., Huttunen, H., Taibi, D.
Number of pages: 11
Pages: 501-511
Publication date: 1 Feb 2020

Host publication information
Title of host publication: SANER 2020 - Proceedings of the 2020 IEEE 27th International Conference on Software Analysis, Evolution, and Reengineering
Publisher: IEEE
Editors: Kontogiannis, K., Khomh, F., Chatzigeorgiou, A., Fokaefs, M., Zhou, M.
ISBN (Electronic): 9781728151434
ASJC Scopus subject areas: Organizational Behavior and Human Resource Management, Hardware and Architecture, Software, Safety, Risk, Reliability and Quality, Computer Networks and Communications
Keywords: architectural smells, code smells, coding style, machine learning, SonarQube, static analysis, Technical Debt
DOIs:

10.1109/SANER48275.2020.9054821

Bibliographical note
EXT="Lenarduzzi, Valentina"
Source: Scopus
Source ID: 85083565109
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Anthropometric clothing measurements from 3D body scans
We propose a full processing pipeline to acquire anthropometric measurements from 3D measurements. The first stage of our pipeline is a commercial point cloud scanner. In the second stage, a pre-defined body model is fitted to the captured point cloud. We have generated one male and one female model from the SMPL library. The fitting process is based on non-rigid iterative closest point algorithm that minimizes overall energy of point distance and local stiffness energy terms. In the third stage, we measure multiple circumference paths on the fitted model surface and use a nonlinear regressor to provide the final estimates of anthropometric measurements. We scanned 194 male and 181 female subjects, and the proposed pipeline provides mean absolute errors from 2.5 to 16.0 mm depending on the anthropometric measurement.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Research group: Vision, NOMO Technologies Ltd
Contributors: Yan, S., Wirta, J., Kämäräinen, J.
Number of pages: 11
Publication date: 2020
Peer-reviewed: Yes

Publication information
Journal: Machine Vision and Applications
Volume: 31
Issue number: 1-2
Article number: 7
ISSN (Print): 0932-8092
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture, Computer Vision and Pattern Recognition, Computer Science Applications
Keywords: 3D body model, Anthropometric measurement, Non-rigid ICP
Electronic versions:

Anthropometric clothing measurements 2020
DOIs:

10.1007/s00138-019-01054-4
URLs:

http://urn.fi/URN:NBN:fi:tuni-202006116044
Source: Scopus
Source ID: 85078296322
Research output: Contribution to journal › Article › Scientific › peer-review

Censor-Based Cooperative Multi-Antenna Spectrum Sensing with Imperfect Reporting Channels
The present contribution proposes a spectrally efficient censor-based cooperative spectrum sensing (C-CSS) approach in a sustainable cognitive radio network that consists of multiple antenna nodes and experiences imperfect sensing and reporting channels. In this context, exact analytic expressions are first derived for the corresponding probability of detection, probability of false alarm, and secondary throughput, assuming that each secondary user (SU) sends its detection outcome to a fusion center only when it has detected a primary signal. Capitalizing on the findings of the analysis, the effects of critical measures, such as the detection threshold, the number of SUs, and the number of employed antennas, on the overall system performance are also quantified. In addition, the optimal detection threshold for each antenna based on the Neyman-Pearson criterion is derived and useful insights are developed on how to maximize the system throughput with a reduced number of SUs. It is shown that the C-CSS approach provides two distinct benefits compared with the conventional sensing approach, i.e., without censoring: i) the sensing tail problem, which exists in imperfect sensing environments, can be mitigated; and ii) less SUs are ultimately required to obtain higher secondary throughput, rendering the system more sustainable.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Research group: Wireless Communications and Positioning, Electrical Engineering, Taiyuan University of Science and Technology, University of Waterloo, Khalifa University, University of Surrey, University of London, Simon Fraser University

Contributors: Li, M., Alhussein, O., Sofotasios, P. C., Muhaidat, S., Yoo, P. D., Liang, J., Wang, A.
Number of pages: 13
Pages: 48-60
Publication date: 2020
Peer-reviewed: Yes

Publication information
Journal: IEEE Transactions on Sustainable Computing
Volume: 5
Issue number: 1
ISSN (Print): 2377-3782
Original language: English
ASJC Scopus subject areas: Computational Theory and Mathematics, Hardware and Architecture, Software, Renewable Energy, Sustainability and the Environment, Control and Optimization
Keywords: censoring, cooperative spectrum sensing, energy detection, energy efficiency, imperfect reporting channels, multi-antenna systems, Sustainble computing
DOIs:

10.1109/TSUSC.2019.2896667
Source: Scopus
Source ID: 85081759371
Research output: Contribution to journal › Article › Scientific › peer-review

Does code quality affect pull request acceptance? An empirical study
Background: Pull requests are a common practice for making contributions and reviewing them in both open-source and industrial contexts.
Objective: Our goal is to understand whether quality flaws such as code smells, anti-patterns, security vulnerabilities, and coding style violations in a pull request's code affect the chance of its acceptance when reviewed by a maintainer of the project.
Method: We conducted a case study among 28 Java open-source projects, analyzing the presence of 4.7 M code quality flaws in 36 K pull requests. We analyzed further correlations by applying logistic regression and six machine learning techniques. Moreover, we manually validated 10% of the pull requests to get further qualitative insights on the importance of quality issues in cases of acceptance and rejection.
Results: Unexpectedly, quality flaws measured by PMD turned out not to affect the acceptance of a pull request at all. As suggested by other works, other factors such as the reputation of the maintainer and the importance of the delivered feature might be more important than other qualities in terms of pull request acceptance.
Conclusions:. Researchers have already investigated the influence of the developers' reputation and the pull request acceptance. This is the first work investigating code style violations and specifically PMD rules. We recommend that researchers further investigate this topic to understand if different measures or different tools could provide some useful measures.

General information
Publication status: E-pub ahead of print
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, LUT University
Contributors: Lenarduzzi, V., Nikkola, V., Saarimäki, N., Taibi, D.
Number of pages: 14
Publication date: 2020
Peer-reviewed: Yes

Publication information
Journal: Journal of Systems and Software
Volume: 171
Article number: 110806
ISSN (Print): 0164-1212
Original language: English
ASJC Scopus subject areas: Software, Information Systems, Hardware and Architecture
Keywords: Machine learning, PMD rules, Pull requests
Electronic versions:

Does code quality affect pull request 2020
DOIs:

10.1016/j.jss.2020.110806
URLs:

http://urn.fi/URN:NBN:fi:tuni-202009187047

Bibliographical note

EXT="Lenarduzzi, Valentina"
INT=comp,"Nikkola, Vili"
Source: Scopus
Source ID: 85090024069
Research output: Contribution to journal › Article › Scientific › peer-review

Does migrating a monolithic system to microservices decrease the technical debt?

Background: The migration from a monolithic system to microservices requires a deep refactoring of the system. Therefore, such a migration usually has a big economic impact and companies tend to postpone several activities during this process, mainly to speed up the migration itself, but also because of the demand for releasing new features.
Objective: We monitored the technical debt of an SME while it migrated from a legacy monolithic system to an ecosystem of microservices. Our goal was to analyze changes in the code technical debt before and after the migration to microservices.
Method: We conducted a case study analyzing more than four years of the history of a twelve-year-old project (280K Lines of Code) where two teams extracted five business processes from the monolithic system as microservices. For the study, we first analyzed the technical debt with SonarQube and then performed a qualitative study with company members to understand the perceived quality of the system and the motivation for possibly postponed activities.
Results: The migration to microservices helped to reduce the technical debt in the long run. Despite an initial spike in the technical debt due to the development of the new microservice, after a relatively short period of time the technical debt tended to grow slower than in the monolithic system.

General information

Publication status: Published
MoE publication type: A2 Review article in a scientific journal
Organisations: Computing Sciences, LUT University
Contributors: Lenarduzzi, V., Lomio, F., Saarimäki, N., Taibi, D.
Number of pages: 16
Publication date: 2020
Peer-reviewed: Yes

Publication information

Journal: Journal of Systems and Software
Volume: 169
Article number: 110710
ISSN (Print): 0164-1212
Original language: English
ASJC Scopus subject areas: Software, Information Systems, Hardware and Architecture
Keywords: Architectural debt, Code quality, Microservices, Refactoring, Technical debt
DOIs:
10.1016/j.jss.2020.110710

Bibliographical note

EXT="Lenarduzzi, Valentina"
Source: Scopus
Source ID: 85087383887
Research output: Contribution to journal › Review Article › Scientific › peer-review

Energy Efficiency Analysis of Collaborative Compressive Sensing Scheme in Cognitive Radio Networks

In this paper, we investigate the energy efficiency of conventional collaborative compressive sensing (CCCS) scheme, focusing on balancing the tradeoff between energy efficiency and detection accuracy in cognitive radio environment. In particular, we derive the achievable throughput, energy consumption and energy efficiency of the CCCS scheme, and formulate an optimization problem to determine the optimal values of parameters which maximize the energy efficiency of the CCCS scheme. The maximization of energy efficiency is proposed as a multi-variable, non-convex optimization problem, and we provide approximations to reduce it to a convex optimization problem. We highlight that errors due to these approximations are negligible. Subsequently, we analytically characterize the tradeoff between dimensionality reduction and collaborative sensing performance of the CCCS scheme i.e. the implicit tradeoff between energy saving and detection accuracy. It is shown that the resulting loss due to compression can be recovered through collaboration, which improves the overall energy efficiency of the system.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Research group: Wireless Communications and Positioning, Electrical Engineering, Birla Institute of Technology & Science, PES University, Khalifa University, University of Texas at Dallas, University of Warwick
Contributors: Kishore, R., Gurugopinath, S., Muhaidat, S., Sofotasios, P. C., Dianati, M., Al-Dhahir, N.

Number of pages: 13
Pages: 1056-1068
Publication date: 2020
Peer-reviewed: Yes

Publication information
Journal: IEEE Transactions on Cognitive Communications and Networking
Volume: 6
Issue number: 3
ISSN (Print): 2332-7731
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Computer Networks and Communications, Artificial Intelligence
Keywords: Achievable throughput, Cognitive radio, Collaboration, collaborative compressive sensing, Compressed sensing, Energy consumption, energy consumption, energy efficiency, Optimization, Sensors, spectrum sensing., Throughput
DOIs:
10.1109/TCCN.2020.3007901
Source: Scopus
Source ID: 85090232901
Research output: Contribution to journal › Article › Scientific › peer-review

Vehicle Attribute Recognition by Appearance: Computer Vision Methods for Vehicle Type, Make and Model Classification
This paper studies vehicle attribute recognition by appearance. In the literature, image-based target recognition has been extensively investigated in many use cases, such as facial recognition, but less so in the field of vehicle attribute recognition. We survey a number of algorithms that identify vehicle properties ranging from coarse-grained level (vehicle type) to fine-grained level (vehicle make and model). Moreover, we discuss two alternative approaches for these tasks, including straightforward classification and a more flexible metric learning method. Furthermore, we design a simulated real-world scenario for vehicle attribute recognition and present an experimental comparison of the two approaches.

General information
Publication status: E-pub ahead of print
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Research group: Multimedia Research Group - MRG
Contributors: Ni, X., Huttunen, H.
Publication date: 2020
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
ISSN (Print): 1939-8018
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Image classification, Metric learning, Vehicle attribute recognition
Electronic versions:
Ni-Huttunen2020_Article_VehicleAttributeRecognitionByA
DOIs:
10.1007/s11265-020-01567-6
URLs:
http://urn.fi/URN:NBN:fi:tuni-202007076341
Source: Scopus
Source ID: 85086837300
Research output: Contribution to journal › Article › Scientific › peer-review

Gamified coding: Toy robots and playful learning in early education
This paper explores the activity of coding with smart toy robots Dash and Botley as a part of playful learning in the Finnish early education context. The findings of our study demonstrate how coding with the two toy robots was approached, conducted and played by Finnish preschoolers aged 5-6 years. The main conclusion of the study is that preschoolers used the toy robots with affordances related to coding mainly in developing gamified play around them by designing tracks for the toys, programming the toys to solve obstacle paths, and competing in player-generated contests of dexterity, speed and physically mobile play.

General information
Publication status: Published

MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Research group: TUT Game Lab, University of Turku School of Cultural Production and Landscape Studies, Prizztech Ltd.
Contributors: Heljakka, K., Ihamaki, P., Tuomi, P., Saarikoski, P.
Number of pages: 6
Pages: 800-805
Publication date: 1 Dec 2019

Host publication information
Title of host publication: Proceedings - 6th Annual Conference on Computational Science and Computational Intelligence, CSCI 2019
Publisher: IEEE
Article number: 9071010
ISBN (Electronic): 9781728155845
ASJC Scopus subject areas: Artificial Intelligence, Computer Networks and Communications, Signal Processing, Hardware and Architecture, Computational Theory and Mathematics
Keywords: Coding, Gamification, Physical play, Programming, Toy robots
DOIs:

10.1109/CSCI49370.2019.00152
Source: Scopus
Source ID: 85084738629
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Optimized wake-up scheme with bounded delay for energy-efficient MTC
The limitations of state-of-the-art cellular modems prevent achieving low-power and low-latency Machine Type Communications (MTC) based on current power saving mechanisms alone. Recently, the concept of wake-up scheme has been proposed to enhance battery lifetime of 5G devices, while reducing the buffering delay. The existing wake-up algorithms use static operational parameters that are determined by the radio access network at the start of the userâ™s session. In this paper, the average power consumption of the wake-up enabled MTC UE is modeled by using a semi-Markov process and then optimized through a delay-constrained optimization problem, by which the optimal wake-up cycle is obtained in closed form. Numerical results show that the proposed solution reduces the power consumption of an optimized Discontinuous Reception (DRX) scheme by up to 40% for a given delay requirement.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Helsinki RanD Center, Huawei Technologies Oy (Finland). Co. Ltd., Centre Tecnologic de Telecomunicacions de Catalunya
Contributors: Rostami, S., Lagen, S., Costa, M., DIni, P., Valkama, M.
Publication date: 1 Dec 2019

Host publication information
Title of host publication: 2019 IEEE Global Communications Conference, GLOBECOM 2019 - Proceedings
Publisher: IEEE
Article number: 9013534
ISBN (Electronic): 9781728109626
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems, Signal Processing, Information Systems and Management, Safety, Risk, Reliability and Quality, Media Technology, Health Informatics
Keywords: 5G, DRX, Energy efficiency, MTC, Wake-up schemes
DOIs:

10.1109/GLOBECOM38437.2019.9013534
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Prototyping directional UAV-based wireless access and backhaul systems
Providing sufficient mobile coverage during mass public events or critical situations is a highly challenging task for the network operators. To fulfill the extreme capacity and coverage demands within a limited area, several augmenting solutions might be used. Among them, novel technologies like a fleet of compact base stations mounted on Unmanned Aerial Vehicles (UAVs) are gaining momentum because of their time- and cost- efficient deployment. Despite the fact that the concept of aerial wireless access networks has been investigated recently in many research studies, there are still numerous practical aspects that require further understanding and extensive evaluation. Taking this as a motivation, in this paper, we develop the concept of continuous wireless coverage provisioning by the means of UAVs and assess its usability in mass scenarios with thousands of users. With our system-level simulations as well as a measurement campaign, we take into account a set of important parameters including weather conditions, UAV speed, weight, power consumption, and millimeter- wave (mmWave) antenna configuration. As a result, we provide more realistic data about the

performance of the access and backhaul links together with the practical lessons learned about the design and real-world applicability of the UAV-enabled wireless access networks.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Department of Telecommunications, Brno University of Technology
Contributors: Gerasimenko, M., Pokorny, J., Schneider, T., Sirjov, J., Andreev, S., Hosek, J.
Publication date: 1 Dec 2019

Host publication information
Title of host publication: 2019 IEEE Global Communications Conference, GLOBECOM 2019 - Proceedings
Publisher: IEEE
Article number: 9014228
ISBN (Electronic): 9781728109626
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems, Signal Processing, Information Systems and Management, Safety, Risk, Reliability and Quality, Media Technology, Health Informatics
DOIs:

10.1109/GLOBECOM38437.2019.9014228
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Software architecture design in global software development: An empirical study
In Global Software Development (GSD), the additional complexity caused by global distance requires processes to ease collaboration difficulties, reduce communication overhead, and improve control. How development tasks are broken down, shared and prioritized is key to project success. While the related literature provides some support for architects involved in GSD, guidelines are far from complete. This paper presents a GSD Architectural Practice Framework reflecting the views of software architects, all of whom are working in a distributed setting. In-depth interviews with architects from seven different GSD organizations revealed a complex set of challenges and practices. We found that designing software for distributed teams requires careful selection of practices that support understanding and adherence to defined architectural plans across sites. Teams used Scrum which aided communication, and Continuous Integration which helped solve synchronization issues. However, teams deviated from the design, causing conflicts. Furthermore, there needs to be a balance between the self-organizing Scrum team methodology and the need to impose architectural design decisions across distributed sites. The research presented provides an enhanced understanding of architectural practices in GSD companies. Our GSD Architectural Practice Framework gives practitioners a cohesive set of warnings, which for the most part, are matched by recommendations.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Research area: Software engineering, University of Limerick
Contributors: Sievi-Korte, O., Richardson, I., Beecham, S.
Publication date: 1 Dec 2019
Peer-reviewed: Yes

Publication information
Journal: Journal of Systems and Software
Volume: 158
Article number: 110400
ISSN (Print): 0164-1212
Ratings:

Scopus rating (2019): CiteScore 7.8 SJR 0.772 SNIP 2.387
Original language: English
ASJC Scopus subject areas: Software, Information Systems, Hardware and Architecture
Keywords: Empirical study, Global software development, GSD, GSE, Scrum, Software architecture
DOIs:

10.1016/j.jss.2019.110400
URLs:

http://urn.fi/URN:NBN:fi:tuni-202001151274. Embargo ends: 18/09/21
Source: Scopus
Source ID: 85072283236
Research output: Contribution to journal › Article › Scientific › peer-review

Programming languages for data-Intensive HPC applications: A systematic mapping study

A major challenge in modelling and simulation is the need to combine expertise in both software technologies and a given scientific domain. When High-Performance Computing (HPC) is required to solve a scientific problem, software development becomes a problematic issue. Considering the complexity of the software for HPC, it is useful to identify programming languages that can be used to alleviate this issue. Because the existing literature on the topic of HPC is very dispersed, we performed a Systematic Mapping Study (SMS) in the context of the European COST Action cHiPSet. This literature study maps characteristics of various programming languages for data-intensive HPC applications, including category, typical user profiles, effectiveness, and type of articles. We organised the SMS in two phases. In the first phase, relevant articles are identified employing an automated keyword-based search in eight digital libraries. This lead to an initial sample of 420 papers, which was then narrowed down in a second phase by human inspection of article abstracts, titles and keywords to 152 relevant articles published in the period 2006–2018. The analysis of these articles enabled us to identify 26 programming languages referred to in 33 of relevant articles. We compared the outcome of the mapping study with results of our questionnaire-based survey that involved 57 HPC experts. The mapping study and the survey revealed that the desired features of programming languages for data-intensive HPC applications are portability, performance and usability. Furthermore, we observed that the majority of the programming languages used in the context of data-intensive HPC applications are text-based general-purpose programming languages. Typically these have a steep learning curve, which makes them difficult to adopt. We believe that the outcome of this study will inspire future research and development in programming languages for data-intensive HPC applications.

General information

Publication status: E-pub ahead of print
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Research group: MMDM, Universidade Nova de Lisboa, University of Torino, Der Technischen Universitat Wien Fakultät für Elektrotechnik und Informationstechnik, University of Stirling, Universidade de Lisboa, University of Latvia, NOVA University of Lisbon, University of Amsterdam, Aristotle University of Thessaloniki, Linköping University, Queen's University, Belfast, Northern Ireland, Linnaeus University, Kalmar, Instituto Superior de Engenharia de Lisboa
Contributors: Amaral, V., Norberto, B., Goulão, M., Aldinucci, M., Benkner, S., Bracciali, A., Carreira, P., Celms, E., Correia, L., Grelck, C., Karatza, H., Kessler, C., Kilpatrick, P., Martiniano, H., Mavridis, I., Pllana, S., Respício, A., Simão, J., Veiga, L., Visa, A.
Number of pages: 17
Publication date: 8 Nov 2019
Peer-reviewed: Yes

Publication information

Journal: Parallel Computing
Volume: 91
Article number: 102584
ISSN (Print): 0167-8191
Ratings:

Scopus rating (2019): CiteScore 2.9 SJR 0.346 SNIP 1.104
Original language: English
ASJC Scopus subject areas: Software, Theoretical Computer Science, Hardware and Architecture, Computer Networks and Communications, Computer Graphics and Computer-Aided Design, Artificial Intelligence
Keywords: Big data, Data-intensive applications, Domain-Specific language (DSL), General-Purpose language (GPL), High performance computing (HPC), Programming languages, Systematic mapping study (SMS)
DOIs:

10.1016/j.parco.2019.102584
Source: Scopus
Source ID: 85076201522
Research output: Contribution to journal › Article › Scientific › peer-review

Action-Oriented Programming Model: Collective Executions and Interactions in the Fog

Today's dominant design for the Internet of Things (IoT) is a Cloud-based system, where devices transfer their data to a back-end and in return receive instructions on how to act. This view is challenged when delays caused by communication with the back-end become an obstacle for IoT applications with, for example, stringent timing constraints. In contrast, Fog Computing approaches, where devices communicate and orchestrate their operations collectively and closer to the origin of data, lack adequate tools for programming secure interactions between humans and their proximate devices at the network edge. This paper fills the gap by applying Action-Oriented Programming (AcOP) model for this task. While originally the AcOP model was proposed for Cloud-based infrastructures, presently it is re-designed around the notion of coalescence and disintegration, which enable the devices to collectively and autonomously execute their operations in the Fog by serving humans in a peer-to-peer fashion. The Cloud's role has been minimized—it is being leveraged as a development and deployment platform.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Electrical Engineering, Department of Computer Science, University of Helsinki, National Research University Higher School of Economics
Contributors: Mäkitalo, N., Aaltonen, T., Raatikainen, M., Ometov, A., Andreev, S., Koucheryavy, Y., Mikkonen, T.
Publication date: 1 Nov 2019
Peer-reviewed: Yes

Publication information
Journal: Journal of Systems and Software
Volume: 157
Article number: 110391
ISSN (Print): 0164-1212
Ratings:

Scopus rating (2019): CiteScore 7.8 SJR 0.772 SNIP 2.387
Original language: English
ASJC Scopus subject areas: Software, Information Systems, Hardware and Architecture
Keywords: Edge computing, Fog Computing, Programming model, Proximity-based computing, Socio-technical systems
Electronic versions:

1-s2.0-S0164121219301669-main
DOIs:

10.1016/j.jss.2019.110391
URLs:

http://urn.fi/URN:NBN:fi:tuni-201909173345

Bibliographical note
EXT="Mäkitalo, Niko"
EXT="Mikkonen, Tommi"
Source: Scopus
Source ID: 85070882337
Research output: Contribution to journal › Article › Scientific › peer-review

Feasibility of FPGA accelerated IPsec on cloud
Hardware acceleration for famous VPN solution, IPsec, has been widely researched already. Still it is not fully covered and the increasing latency, throughput, and feature requirements need further evaluation. We propose an IPsec accelerator architecture in an FPGA and explain the details that need to be considered for a production ready design. This research considers the IPsec packet processing without IKE to be offloaded on an FPGA in an SDN network. Related work performance rates in 64 byte packet size for throughput is 1–2 Gbps with 0.2 ms latency in software, and 1–4 Gbps with unknown latencies for hardware solutions. Our proposed architecture is capable to host 1000 concurrent tunnels and have 10 Gbps throughput with only 10 µs latency in our test network. Therefore the proposed design is efficient even with voice or video encryption. The architecture is especially designed for data centers and locations with vast number of concurrent IPsec tunnels. The research confirms that FPGA based hardware acceleration increases performance and is feasible to integrate with the other server infrastructure.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Research area: Information security, Baseband ASIC R&D, Nokia Siemens Networks
Contributors: Vajaranta, M., Oinonen, A., Hämäläinen, T. D., Viitamäki, V., Markunmäki, J., Kulmala, A.
Publication date: 1 Nov 2019
Peer-reviewed: Yes

Publication information
Journal: Microprocessors and Microsystems
Volume: 71
Article number: 102861
ISSN (Print): 0141-9331
Ratings:

Scopus rating (2019): CiteScore 3 SJR 0.303 SNIP 0.879
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture, Computer Networks and Communications, Artificial Intelligence
Keywords: Accelerator, IPsec, Offloading, SDN
DOIs:

10.1016/j.micpro.2019.102861

Bibliographical note
EXT="Viitamäki, Vili"
EXT="Kulmala, Ari"
Source: Scopus
Source ID: 85070320729
Research output: Contribution to journal › Article › Scientific › peer-review

An icon that everyone wants to click: How perceived aesthetic qualities predict app icon successfulness
Mobile app markets have been touted as fastest growing marketplaces in the world. Every day thousands of apps are published to join millions of others on app stores. The competition for top grossing apps and market visibility is fierce. The way an app is visually represented can greatly contribute to the amount of attention an icon receives and to its consequent commercial performance. Therefore, the icon of the app is of crucial importance as it is the first point of contact with the potential user/customer amidst the flood of information. Those apps that fail to arouse attention through their icons danger their commercial performance in the market where consumers browse past hundreds of icons daily. Using semantic differential scale (22 adjective pairs), we investigate the relationship between consumer perceptions of app icons and icon successfulness, measured by 1)overall evaluation of the icon, 2)willingness to click the icon, 3)willingness to download the imagined app and, 4)willingness to purchase the app. The study design was a vignette study with random participant (n = 569)assignment to evaluate 4 icons (n = 2276)from a total of pre-selected 68 game app icons across 4 categories (concrete, abstract, character and text). Results show that consumers are more likely to interact with app icons that are aesthetically pleasing and convey good quality. Particularly, app icons that are perceived unique, realistic and stimulating lead to more clicks, downloads and purchases.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Gamification Group, Tampere University, University of Turku
Contributors: Jylhä, H., Hamari, J.
Number of pages: 13
Pages: 73-85
Publication date: 1 Oct 2019
Peer-reviewed: Yes

Publication information
Journal: International Journal of Human Computer Studies
Volume: 130
ISSN (Print): 1071-5819
Ratings:

Scopus rating (2019): CiteScore 5.8 SJR 0.756 SNIP 2.163
Original language: English
ASJC Scopus subject areas: Software, Human Factors and Ergonomics, Education, Engineering(all), Human-Computer Interaction, Hardware and Architecture
Keywords: Aesthetics, Digital marketing, Graphical user interfaces, Iconography, Mobile apps, Semantic differential
Electronic versions:

1-s2.0-S1071581918301794-main
DOIs:

10.1016/j.ijhcs.2019.04.004
URLs:

http://urn.fi/URN:NBN:fi:tty-201907081945
Source: Scopus
Source ID: 85067993498
Research output: Contribution to journal › Article › Scientific › peer-review

The Double Shadowed κ-μ Fading Model
In this paper, we introduce a new fading model which is capable of characterizing both the shadowing of the dominant component and composite shadowing which may exist in wireless channels. More precisely, this new model assumes a κ-μ envelope where the dominant component is fluctuated by a Nakagami-m random variable (RV) which is preceded (or succeeded) by a secondary round of shadowing brought about by an inverse Nakagami-m RV. We conveniently refer to this as the double shadowed κ-μ fading model. In this context, novel closed-form and analytical expressions are developed for a range of channel related statistics, such as the probability density function, cumulative distribution function, and moments. All of the derived expressions have been validated through Monte-Carlo simulations and reduction to a number of well-known special cases. It is worth highlighting that the proposed fading model offers remarkable flexibility as it includes the κ-μ, η-μ, Rician shadowed, double shadowed Rician, κ-μ shadowed, κ-μ/inverse gamma and η-μ/inverse gamma distributions as special cases.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research group: Wireless Communications and Positioning, Electrical Engineering, Queen's University, Belfast, Northern Ireland, Universidade Estadual de Campinas, Center on Cyber-Physical Systems, Khalifa University, Tampere University of Applied Sciences
Contributors: Simmons, N., Nogueira Da Silva, C. R., Cotton, S. L., Sofotasios, P. C., Ki Yoo, S., Yacoub, M. D.
Publication date: 1 Oct 2019

Host publication information
Title of host publication: 2019 International Conference on Wireless and Mobile Computing, Networking and Communications, WiMob 2019
Publisher: IEEE
ISBN (Electronic): 9781728133164

Publication series
Name: International Conference on Wireless and Mobile Computing, Networking and Communications
ISSN (Print): 2161-9646
ISSN (Electronic): 2161-9654
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Software
DOIs:

10.1109/WiMOB.2019.8923336
Source: Scopus
Source ID: 85077583520
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Towards Algebraic Modeling of GPU Memory Access for Bank Conflict Mitigation
Graphics Processing Units (GPU) have been widely used in various fields of scientific computing, such as in signal processing. GPUs have a hierarchical memory structure with memory layers that are shared between GPU processing elements. Partly due to the complex memory hierarchy, GPU programming is non-Trivial, and several aspects must be taken into account, one being memory access patterns. One of the fastest GPU memory layers, shared memory, is grouped into banks to enable fast, parallel access for processing elements. Unfortunately, it may happen that multiple threads of a GPU program may access the same shared memory bank simultaneously causing a bank conflict. If this happens, program execution slows down as memory accesses have to be rescheduled to determine which instruction to execute first. Bank conflicts are not taken into account automatically by the compiler, and hence the programmer must detect and deal with them prior to program execution. In this paper, we present an algebraic approach to detect bank conflicts and prove some theoretical results that can be used to predict when bank conflicts happen and how to avoid them. Also, our experimental results illustrate the savings in computation time.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Research area: Computer engineering, Tampere University
Contributors: Ferranti, L., Boutellier, J.
Number of pages: 6
Pages: 103-108
Publication date: 1 Oct 2019

Host publication information
Title of host publication: 2019 IEEE International Workshop on Signal Processing Systems, SiPS 2019
Publisher: IEEE
ISBN (Electronic): 9781728119274
ASJC Scopus subject areas: Electrical and Electronic Engineering, Signal Processing, Applied Mathematics, Hardware and Architecture
Keywords: block matching, Graphics processing units, memory hierarchy, OpenCL
DOIs:

10.1109/SiPS47522.2019.9020385

Bibliographical note
INT=comp,"Ferranti, Luca"
Source: Scopus
Source ID: 85082393531
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

An approval of MPPT based on pv cell's simplified equivalent circuit during fast-shading conditions

The partial shading conditions significantly affect the functionality of solar power plants despite the presence of multiple maximum power point tracking systems. The primary cause of this problem is the presence of local maxima in the power–current and/or power–voltage characteristic curves that restrict the functionality of the conventional maximum power point tracking systems. The present article proposes a modified algorithm based on the simplified equivalent circuit of solar cells to improve the functionality of traditional maximum power point tracking systems. This algorithm provides a method for regularly monitoring the photo-current of each solar module. The upper and lower boundaries of the regulating parameter such as current or voltage are decided very precisely, which is helpful to find the location of the global maximum. During a sequential search, the control system accurately determines the lower and upper boundaries of the global maximum. Simultaneously, the maximum power point tracking system increases the photovoltaic current up to one of these boundaries and applies one of the conventional algorithms. Additionally, the control system regularly monitors the photovoltaic characteristics and changes the limits of regulating parameter concerning any change in global maximum location. This proposed method is fast and precise to locate the global maximum boundaries and to track global maximum even under fast-changing partial shading conditions. The improved performance and overall efficiency are validated by simulation study for variable solar irradiance.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Automation Technology and Mechanical Engineering, Ariel University Center of Samaria
Contributors: Rajput, S., Averbukh, M., Yahalom, A., Minav, T.
Number of pages: 14
Publication date: 1 Sep 2019
Peer-reviewed: Yes

Publication information

Journal: Electronics (Switzerland)
Volume: 8
Issue number: 9
Article number: 1060
ISSN (Print): 2079-9292
Ratings:

Scopus rating (2019): CiteScore 1.9 SJR 0.303 SNIP 1.088
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Signal Processing, Hardware and Architecture, Computer Networks and Communications, Electrical and Electronic Engineering
Keywords: Equivalent circuit, Global maximum, Maximum power point tracking, Partial shading, Photovoltaic system, Solar module
Electronic versions:

electronics-08-01060-v2
DOIs:

10.3390/electronics8091060
URLs:

http://urn.fi/URN:NBN:fi:tuni-201912126797
Source: Scopus
Source ID: 85075081647
Research output: Contribution to journal › Article › Scientific › peer-review

Model checking and validity in propositional and modal inclusion logics

Propositional and modal inclusion logic are formalisms that belong to the family of logics based on team semantics. This article investigates the model checking and validity problems of these logics. We identify complexity bounds for both problems, covering both lax and strict team semantics. By doing so, we come close to finalizing the programme that aims to completely classify the complexities of the basic reasoning problems for modal and propositional dependence, independence and inclusion logics.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Tampere University, Leibniz Universität Hannover, University of Helsinki, Hasselt University
Contributors: Hella, L., Kuusisto, A., Meier, A., Virtema, J.
Number of pages: 26
Pages: 605-630
Publication date: 1 Sep 2019
Peer-reviewed: Yes

Publication information
Journal: JOURNAL OF LOGIC AND COMPUTATION
Volume: 29
Issue number: 5
ISSN (Print): 0955-792X
Ratings:

Scopus rating (2019): CiteScore 2.8 SJR 0.786 SNIP 1.481
Original language: English
ASJC Scopus subject areas: Software, Theoretical Computer Science, Arts and Humanities (miscellaneous), Hardware and Architecture, Logic
Keywords: complexity, Inclusion logic, model checking, team semantics, validity problem
DOIs:

10.1093/logcom/exz008
Source: Scopus
Source ID: 85080893187
Research output: Contribution to journal › Article › Scientific › peer-review

2-volt Solution-Processed, Indium Oxide (In_2O_3) Thin Film Transistors on flexible Kapton

Semiconductor devices based upon silicon have powered the modern electronics revolution through advanced manufacturing processes. However, the requirement of high temperatures to create crystalline silicon devices has restricted its use in a number of new applications, such as printed and flexible electronics. Thus, developments with high mobility solution-processable metal oxides, surpassing α-Si in many instances, is opening a new era for flexible and wearable electronics. However, high operating voltages and relatively high deposition temperatures required for metal oxides remain impediments for the flexible devices. Here, the fabrication of low operating voltage, flexible thin film transistors (TFT) using a solution processed indium oxide In_2O_3) channel material with room temperature deposited anodized high-κ aluminum oxide (Al_2O_3) for gate dielectrics are reported. The flexible TFTs operates at low voltage V_{ds} of 2 V, with threshold voltage V_{th} 0.42 V, on/off ratio 10^3 and subthreshold swing (SS) 420 mV/dec. The electron mobility (μ), extracted from the saturation regime, is 2.85 cm^2/V.s and transconductance, gm, is 38 μS.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Research group: Laboratory for Future Electronics, Ohio State University
Contributors: Bhalerao, S. R., Lupo, D., Berger, P. R.
Number of pages: 3
Publication date: 1 Aug 2019

Host publication information
Title of host publication: 2019 IEEE International Flexible Electronics Technology Conference, IFETC 2019
Publisher: IEEE
ISBN (Electronic): 9781728117782
ASJC Scopus subject areas: Electrical and Electronic Engineering, Mechanics of Materials, Electronic, Optical and Magnetic Materials, Hardware and Architecture
DOIs:

10.1109/IFETC46817.2019.9073721
Source: Scopus
Source ID: 85084666179
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

6K and 8K effective resolution with 4K HEVC decoding capability for 360 video streaming

The recent Omnidirectional MediA Format (OMAF) standard, which specifies the delivery of 360° video content, supports only equirectangular projection (ERP) and cubemap projection and their region-wise packing with a limitation on video decoding capability to the maximum resolution of 4K (e.g., 4,096 × 2,048). Streaming of 4K ERP content allows only a limited viewport resolution, which is lower than the resolution of many current head-mounted displays (HMDs). Therefore, to take full advantage of high-resolution HMDs, delivery of 360° video content beyond 4K resolution needs to be enabled. In this regard, we propose two specific mixed-resolution packing schemes of 6K (e.g., 6,144 × 3,072) and 8K (e.g., 8,192 × 4,096) ERP content and their realization in tile-based streaming, while complying with the 4K decoding constraint and the High Efficiency Video Coding standard. The proposed packing schemes offer 6K and 8K effective resolution at the viewport. Using our proposed test methodology, experimental results indicate that the proposed layouts significantly decrease streaming bitrates when compared to mixed-quality viewport-adaptive streaming of 4K ERP. Our results further indicate that 8K-effective packing outperforms 6K-effective packing especially in high-quality videos.

General information
Publication status: Published

MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Nokia Technologies
Contributors: Zare, A., Homayouni, M., Aminlou, A., Hannuksela, M. M., Gabbouj, M.
Publication date: 1 Aug 2019
Peer-reviewed: Yes

Publication information
Journal: ACM Transactions on Multimedia Computing, Communications and Applications
Volume: 15
Issue number: 2s
Article number: 68
ISSN (Print): 1551-6857
Ratings:

Scopus rating (2019): CiteScore 5.6 SJR 0.922 SNIP 1.633
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Computer Networks and Communications
Keywords: 360° video coding and streaming, Adaptive streaming, HEVC, OMAF, Virtual reality
DOIs:

10.1145/3335053

Bibliographical note
EXT="Zare, Alireza"
EXT="Aminlou, Alireza"
Source: Scopus
Source ID: 85071141770
Research output: Contribution to journal › Article › Scientific › peer-review

Are architectural smells independent from code smells? An empirical study
Background. Architectural smells and code smells are symptoms of bad code or design that can cause different quality problems, such as faults, technical debt, or difficulties with maintenance and evolution. Some studies show that code smells and architectural smells often appear together in the same file. The correlation between code smells and architectural smells, however, is not clear yet; some studies on a limited set of projects have claimed that architectural smells can be derived from code smells, while other studies claim the opposite. Objective. The goal of this work is to understand whether architectural smells are independent from code smells or can be derived from a code smell or from one category of them. Method. We conducted a case study analyzing the correlations among 19 code smells, six categories of code smells, and four architectural smells. Results. The results show that architectural smells are correlated with code smells only in a very low number of occurrences and therefore cannot be derived from code smells. Conclusion. Architectural smells are independent from code smells, and therefore deserve special attention by researchers, who should investigate their actual harmfulness, and practitioners, who should consider whether and when to remove them.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, University Milano-Bicocca, Alten Italia
Contributors: Arcelli Fontana, F., Lenarduzzi, V., Roveda, R., Taibi, D.
Number of pages: 18
Pages: 139-156
Publication date: 1 Aug 2019
Peer-reviewed: Yes

Publication information
Journal: Journal of Systems and Software
Volume: 154
ISSN (Print): 0164-1212
Ratings:

Scopus rating (2019): CiteScore 7.8 SJR 0.772 SNIP 2.387
Original language: English
ASJC Scopus subject areas: Software, Information Systems, Hardware and Architecture
Keywords: Architectural smells, Code smells, Empirical analysis, Technical debt
DOIs:

10.1016/j.jss.2019.04.066
Source: Scopus
Source ID: 85064869442
Research output: Contribution to journal › Article › Scientific › peer-review

AEx: Automated Customization of Exposed Datapath Soft-Cores

High-level synthesis tools aim to produce hardware designs out of software descriptions with a goal to lower the bar in FPGA usage for software engineers. Despite their recent progress, however, HLS tools still require FPGA target specific pragmas and other modifications to the originally processor-targeting source code descriptions. Customized soft core based overlay architectures provide a software programmable layer on top of the FPGA fabric. The benefit of this approach is that a platform independent compiler target is presented to the programs, which lowers the porting burden, and online repurposing the same configuration is natural by just switching the executed program. The main drawback, like with any overlay architecture, are the additional implementation overheads the overlay imposes to the resource consumption and the maximum operating frequency. In this paper we show how by utilizing the efficient structure of Transport-Triggered Architectures (TTA), soft-cores can be customized automatically to benefit from the flexible FPGA fabric while still presenting a comfortable software layer to the users. The results compared to previously published non-specialized TTA soft cores indicate equal or better execution times, while the program image size is reduced by up to 49%, and overall resource utilization improved from 10% to 60%.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Research area: Computer engineering, Tampere University
Contributors: Hirvonen, A., Tervo, K., Kultala, H., Jääskelainen, P.
Number of pages: 8
Pages: 35-42
Publication date: Aug 2019

Host publication information

Title of host publication: Proceedings - Euromicro Conference on Digital System Design, DSD 2019
Publisher: IEEE
Editors: Konofaos, N., Kitsos, P.
ISBN (Electronic): 9781728128610

Publication series

Name: Proceedings - Euromicro Conference on Digital System Design, DSD 2019
ASJC Scopus subject areas: Hardware and Architecture, Information Systems, Information Systems and Management
Keywords: FPGA, high level synthesis, programmable overlays, soft cores, Transport-Triggered Architecture
DOIs:

10.1109/DSD.2019.00016
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Blockchain Technology for Smartphones and Constrained IoT Devices: A Future Perspective and Implementation

The blockchain technology is currently penetrating different sides of modern ICT community. Most of the devices involved in blockchain-related processes are specially designed targeting only the mining aspect. At the same time, the use of wearable and mobile devices may also become a part of blockchain operation, especially during the charging time. The paper considers the possibility of using a large number of constrained devices supporting the operation of the blockchain. The utilization of such devices is expected to improve the efficiency of the system and also to attract a more substantial number of users. Authors propose a novel consensus algorithm based on a combination of Proof-of-Work (PoW), Proof-of-Activity (PoA), and Proof-of-Stake (PoS). The paper first overviews the existing strategies and further describes the developed cryptographic primitives used to build a blockchain involving mobile devices. A brief numerical evaluation of the designed system is also provided in the paper.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Enecuum HK Limited, ITMO University, St. Petersburg State University of Telecommunication
Contributors: Zhidanov, K., Bezzateev, S., Afanasyeva, A., Sayfullin, M., Vanurin, S., Bardinova, Y., Ometov, A.
Number of pages: 8
Pages: 20-27
Publication date: 1 Jul 2019

Host publication information

Title of host publication: 21st IEEE Conference on Business Informatics, CBI 2019
Publisher: IEEE
Editors: Becker, J., Pastor, O., Kornyshova, E., Korepanov, V. O., Tsukanova, O. A., Albornoz, J. B., Fedyanin, D., Burkov, V., Nazarov, D. M., Novikov, D., Uskenbaeva, R., Shchepkin, A. V.
Article number: 8808043

ISBN (Electronic): 9781728106502
ASJC Scopus subject areas: Business, Management and Accounting (miscellaneous), Management Information Systems , Hardware and Architecture, Information Systems, Information Systems and Management, Control and Optimization
Keywords: applications, blockhcain, distributed systems, future perspective, networks
Electronic versions:

Blockchain Technology for Smartphones and Constrained IoT Devices A Future Perspective and Implementation
DOIs:

10.1109/CBI.2019.10092
URLs:

http://urn.fi/URN:NBN:fi:tuni-202001151290

Bibliographical note
EXT="Zhidanov, Konstantin"
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Input magnitude data setting in error-reduction algorithm for one-dimensional discrete phase retrieval problem
In this paper we discuss how does the input magnitude data setting influence the behavior of error-reduction algorithm in the case of the one-dimensional discrete phase retrieval problem. We present experimental results related to the convergence or stagnation of the algorithm. We also discuss the issue of the zeros distribution of the solution, when the solution of the problem exists.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, FETTI, Technical University of Cluj-NapocaUniversitatea Tehnica din Cluj-Napoca
Contributors: Rusu, C., Astola, J.
Publication date: 1 Jul 2019

Host publication information
Title of host publication: ISSCS 2019 - International Symposium on Signals, Circuits and Systems
Publisher: IEEE
Article number: 8801743
ISBN (Electronic): 9781728138961
ASJC Scopus subject areas: Computer Vision and Pattern Recognition, Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
DOIs:

10.1109/ISSCS.2019.8801743

Bibliographical note
EXT="Rusu, Corneliu"
Source: Scopus
Source ID: 85071848180
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Acceptance and perceptions of interactive location-tracking displays
Tracking the location of people and their mobile devices creates opportunities for new and exciting ways of interacting with public technology. For instance, users can transfer content from public displays to their mobile device without touching it, because location tracking allows automatic recognition of the target device. However, many uncertainties remain regarding how users feel about interactive displays that track them and their mobile devices, and whether their experiences vary based on the setting. To close this research gap, we conducted a 24-participant user study. Our results suggest that users are largely willing - even excited - to adopt novel location-tracking systems. However, users expect control over when and where they are tracked, and want the system to be transparent about its ownership and data collection. Moreover, the deployment setting plays a much bigger role on people's willingness to use interactive displays when location tracking is involved.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Ludwig Maximilian University, Tampere University
Contributors: Mäkelä, V., Linna, J., Keskinen, T., Hakulinen, J., Turunen, M.
Publication date: 12 Jun 2019

Host publication information
Title of host publication: Pervasive Displays 2019 - 8th ACM International Symposium on Pervasive Displays, PerDis 2019

Publisher: ACM
Editors: Gentile, V., Cauchard, J. R.
Article number: a17
ISBN (Electronic): 9781450367516
ASJC Scopus subject areas: Computer Science Applications, Hardware and Architecture, Computer Networks and Communications, Computer Graphics and Computer-Aided Design
Keywords: Acceptance, Location tracking, Location-based services, Mobile devices, Perceptions, Privacy, Public displays , Trust, Ubiquitous computing
DOIs:
10.1145/3321335.3324931
URLs:
http://urn.fi/URN:NBN:fi:tuni-201910013614
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Socially inspired relaying and proactive mode selection in mmWave vehicular communications

As the Internet of Vehicles matures and acquires its social flavor, novel wireless connectivity enablers are being demanded for reliable data transfer in high-rate applications. The recently ratified New Radio communications technology operates in millimeter-wave (mmWave) spectrum bands and offers sufficient capacity for bandwidth-hungry services. However, seamless operation over mmWave is difficult to maintain on the move, since such extremely high frequency radio links are susceptible to unexpected blockage by various obstacles, including vehicle bodies. As a result, proactive mode selection, that is, migration from infrastructure- to vehicle-based connections and back, is becoming vital to avoid blockage situations. Fortunately, the very social structure of interactions between the neighboring smart cars and their passengers may be leveraged to improve session continuity by relaying data via proximate vehicles. This paper conceptualizes the socially inspired relaying scenarios, conducts underlying mathematical analysis, continues with a detailed 3-D modeling to facilitate proactive mode selection, and concludes by discussing a practical prototype of a vehicular mmWave platform.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Electrical Engineering, University of California, Los Angeles
Contributors: Moltchanov, D., Kovalchukov, R., Gerasimenko, M., Andreev, S., Koucheryavy, Y., Gerla, M.
Number of pages: 12
Pages: 5172-5183
Publication date: 1 Jun 2019
Peer-reviewed: Yes

Publication information

Journal: IEEE Internet of Things Journal
Volume: 6
Issue number: 3
ISSN (Print): 2327-4662
Ratings:
Scopus rating (2019): CiteScore 12.6 SJR 2.607 SNIP 4.11
Original language: English
ASJC Scopus subject areas: Signal Processing, Information Systems, Hardware and Architecture, Computer Science Applications, Computer Networks and Communications
Keywords: Internet of Things, Millimeter wave (mmWave) communication, Social network services, Vehicular ad hoc networks
Electronic versions:
Socially-Inspired Relaying 2019
DOIs:
10.1109/JIOT.2019.2898420
URLs:
http://urn.fi/URN:NBN:fi:tuni-202001311720
Source: Scopus
Source ID: 85067875266
Research output: Contribution to journal › Article › Scientific › peer-review

Opportunistic ambient backscatter communication in RF-Powered cognitive radio networks

In the present contribution, we propose a novel opportunistic ambient backscatter communication (ABC) framework for radio frequency (RF)-powered cognitive radio (CR) networks. This framework considers opportunistic spectrum sensing (SS) integrated with ABC and harvest-then-transmit (HTT) operation strategies. Novel analytic expressions are derived for the average throughput, the average energy consumption and the energy efficiency (EE) in the considered set up. These

expressions are represented in closed-form and have a tractable algebraic representation which renders them convenient to handle both analytically and numerically. In addition, we formulate an optimization problem to maximize the EE of the CR system operating in mixed ABC - and HTT - modes, for a given set of constraints, including primary interference and imperfect SS constraints. Capitalizing on this, we determine the optimal set of parameters which in turn comprise the optimal detection threshold, the optimal degree of trade-off between the CR system operating in the ABC - and HTT - modes and the optimal data transmission time. Extensive results from respective computer simulations are also presented for corroborating the corresponding analytic results and to demonstrate the performance gain of the proposed model in terms of EE.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Research group: Wireless Communications and Positioning, Electrical Engineering, Khalifa University, Birla Institute of Technology & Science, PES University, University of Texas at Dallas
Contributors: Kishore, R., Gurugopinath, S., Sofotasios, P. C., Muhaidat, S., Al-Dhahir, N.
Number of pages: 14
Pages: 413-426
Publication date: Jun 2019
Peer-reviewed: Yes

Publication information
Journal: IEEE Transactions on Cognitive Communications and Networking
Volume: 5
Issue number: 2
Article number: 8672817
ISSN (Print): 2332-7731
Ratings:

Scopus rating (2019): CiteScore 6.5 SJR 1.802 SNIP 2.427
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Computer Networks and Communications, Artificial Intelligence
Keywords: Ambient backscatter communication, cognitive radio networks, energy detection, energy efficiency, wireless power transfer
DOIs:

10.1109/TCCN.2019.2907090
Source: Scopus
Source ID: 85063386334
Research output: Contribution to journal › Article › Scientific › peer-review

Towards Efficient Code Generation for Exposed Datapath Architectures

Coarse-grained reconfigurable architectures and other exposed datapath architectures such as transport-triggered architectures come with a high energy efficiency promise for accelerating data oriented workloads. Their main drawback results from the push of complexity from the architecture to the programmer; compiler techniques that allow starting from a higher-level programming language and generate code efficiently to such architectures robustly is still an open research area. In this article we survey the known main sources of challenges and outline a generic processor architecture template that covers the most common architecture variations along with a proposal for a common code generation framework for such challenging architectures.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Eindhoven University of Technology
Contributors: Vadivel, K., Jordans, R., Stujik, S., Corporaal, H., Jääskeläinen, P., Kultala, H.
Number of pages: 4
Pages: 86-89
Publication date: 27 May 2019

Host publication information
Title of host publication: Proceedings of the 22nd International Workshop on Software and Compilers for Embedded Systems, SCOPES 2019
Publisher: ACM
Editor: Stuijk, S.
ISBN (Electronic): 9781450367622
ASJC Scopus subject areas: Hardware and Architecture, Software
Keywords: CGRA, code generation, energy efficiency, reconfigurable architectures, scheduling, TTA
DOIs:

10.1145/3323439.3323990
Source: Scopus
Source ID: 85066039585
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Asterism: Decentralized file sharing application for mobile devices

Most applications and services rely on central authorities. This introduces a single point of failure to the system. The central authority must be trusted to have data stored by the application available at any given time. More importantly, the privacy of the user depends on the service provider capability to keep the data safe. A decentralized system could be a solution to remove the dependency from a central authority. Moreover, due to the rapid growth of mobile device usage, the availability of decentralization must not be limited only to desktop computers. In this work we aim at studying the possibility to use mobile devices as a decentralized file sharing platform without any central authorities. This was done by implementing Asterism, a peer-to-peer file-sharing mobile application based on the Inter-Planetary File System. We validate the results by deploying and measuring the application network usage and power consumption in multiple different devices. Results show that mobile devices can be used to implement a worldwide distributed file sharing network. However, the file sharing application generated large amounts of network traffic even when no files were shared. This was caused by the chattiness of the protocol of the underlying peer-to-peer network. Consequently, constant network traffic prevented the mobile devices from entering to deep sleep mode. Due to this the battery life of the devices was greatly degraded.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Tampere University of Applied Sciences
Contributors: Heinisuo, O., Lenarduzzi, V., Taibi, D.
Number of pages: 10
Pages: 38-47
Publication date: 9 May 2019

Host publication information

Title of host publication: 2019 7th IEEE International Conference on Mobile Cloud Computing, Services, and Engineering, MobileCloud 2019
Publisher: IEEE
ISBN (Electronic): 9781728104638
ASJC Scopus subject areas: Computer Science Applications, Hardware and Architecture, Computer Networks and Communications
Keywords: Decentralized file sharing, InterPlanetary File System, Mobile, Peer-to-peer, Sailfish OS
DOIs:
10.1109/MobileCloud.2019.00013
Source: Scopus
Source ID: 85066483944
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Artificial intelligence yesterday, today and tomorrow

Artificial Intelligence (AI) is one of the current emerging technologies. In the history of computing AI has been in the similar role earlier - almost every decade since the 1950s, when the programming language Lisp was invented and used to implement self-modifying applications. The second time that AI was described as one of the frontier technologies was in the 1970s, when Expert Systems (ES) were developed. A decade later AI was again at the forefront when the Japanese government initiated its research and development effort to develop an AI-based computer architecture called the Fifth Generation Computer System (FGCS). Currently in the 2010s, AI is again on the frontier in the form of (self-)learning systems manifesting in robot applications, smart hubs, intelligent data analytics, etc. What is the reason for the cyclic reincarnation of AI? This paper gives a brief description of the history of AI and also answers the question above. The current AI “cycle” has the capability to change the world in many ways. In the context of the CE conference, it is important to understand the changes it will cause in education, the skills expected in different professions, and in society at large.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Tallinn University of Technology, University of Lapland, Computer Science Institute
Contributors: Jaakkola, H., Henno, J., Mäkelä, J., Thalheim, B.
Number of pages: 8
Pages: 860-867
Publication date: 1 May 2019

Host publication information

Title of host publication: 2019 42nd International Convention on Information and Communication Technology, Electronics and Microelectronics, MIPRO 2019 - Proceedings
Publisher: IEEE
Editors: Skala, K., Car, Z., Pale, P., Huljenic, D., Janjic, M., Koricic, M., Sruk, V., Ribaric, S., Grbac, T. G., Butkovic, Z., Cicin-Sain, M., Skvorc, D., Mauher, M., Babic, S., Gros, S., Vrdoljak, B., Tijan, E.
ISBN (Electronic): 9789532330984
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems, Energy Engineering and Power Technology, Electrical and Electronic Engineering, Electronic, Optical and Magnetic Materials
Keywords: Artificial Intelligence, Computer, Computer-supported decision-making, Deep learning, Education, Emerging technology, Expert Systems, Fifth Generation Computer, Frontier technology, Learning, Lisp, Prolog
DOIs:

10.23919/MIPRO.2019.8756913
URLs:

http://docs.mipro-proceedings.com/proceedings/mipro_2019_proceedings.pdf
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Error analysis of NOMA-based user cooperation with SWIPT

The present contribution analyzes the performance of non-orthogonal multiple access (NOMA)-based user cooperation with simultaneous wireless information and power transfer (SWIPT). In particular, we consider a two-user NOMA-based cooperative SWIPT scenario, in which the near user acts as a SWIPT-enabled relay that assists the farthest user. In this context, we derive analytic expressions for the pairwise error probability (PEP) of both users assuming the both amplify-and-forward (AF) and decode-and-forward (DF) relay protocols. The derived expressions are expressed in closed-form and have a tractable algebraic representation which renders them convenient to handle both analytically and numerically. In addition to this, we derive a simple asymptotic closed-form expression for the PEP in the high signal-to-noise ratio (SNR) regime which provide useful insights on the impact of the involved parameters on the overall system performance. Capitalizing on this, we subsequently quantify the maximum achievable diversity order of both users. It is shown that numerical and simulation results corroborate the derived analytic expressions. Furthermore, the offered results provide interesting insights into the error rate performance of each user, which are expected to be useful in future designs and deployments of NOMA based SWIPT systems.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research group: Wireless Communications and Positioning, Electrical Engineering, Taiyuan University of Science and Technology, Khalifa University, University of Surrey, Center on Cyber-Physical Systems, Simon Fraser University
Contributors: Li, S., Bariah, L., Muhaidat, S., Sofotasios, P., Liang, J., Wang, A.
Number of pages: 7
Pages: 507-513
Publication date: 1 May 2019

Host publication information

Title of host publication: Proceedings - 15th Annual International Conference on Distributed Computing in Sensor Systems, DCOSS 2019
Publisher: IEEE
ISBN (Electronic): 9781728105703
ASJC Scopus subject areas: Computer Networks and Communications, Computer Science Applications, Hardware and Architecture, Health Informatics, Instrumentation, Transportation, Communication
Keywords: NOMA, Wireless Power Transfer
DOIs:

10.1109/DCOSS.2019.00098
Source: Scopus
Source ID: 85071915507
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Intelligent data service for farmers

The agricultural sector in Finland has been lagging behind in digital development. Development has long been based on increasing production by investing in larger machines. Over the past decade, change has begun to take place in the direction of digitalization. One of the challenges is that different manufacturers are trying to get farmers' data on their own closed cloud services. In the worst case, farmers may lose an overall view of their farms and opportunities for deeper data analysis because their data is located in different services. The goals and previously studied challenges of the 'MIKÄ DATA' project are described in this research. This project will build an intelligent data service for farmers, which is based on the Oskari platform. In the 'Peltodata' service, farmers can see their own field data and many other data sources layer

by layer. The project is focused on the study of machine learning techniques to develop harvest yield prediction and find out the correlation between many data sources. The 'Peltodata' service will be ready at the end of 2019.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences
Contributors: Linna, P., Narra, N., Grönman, J.
Number of pages: 4
Pages: 1072-1075
Publication date: 1 May 2019

Host publication information
Title of host publication: 2019 42nd International Convention on Information and Communication Technology, Electronics and Microelectronics, MIPRO 2019 - Proceedings
Publisher: IEEE
Editors: Skala, K., Car, Z., Pale, P., Huljenic, D., Janjic, M., Koricic, M., Sruk, V., Ribaric, S., Grbac, T. G., Butkovic, Z., Cicin-Sain, M., Skvorc, D., Mauher, M., Babic, S., Gros, S., Vrdoljak, B., Tijan, E.
ISBN (Electronic): 9789532330984
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems, Energy Engineering and Power Technology, Electrical and Electronic Engineering, Electronic, Optical and Magnetic Materials
Keywords: Agriculture, Artificial intelligence, Platform
DOIs:

10.23919/MIPRO.2019.8756688
URLs:

http://docs.mipro-proceedings.com/proceedings/mipro_2019_proceedings.pdf
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Reducing crossbar costs in the match-action pipeline
Software Defined Networking (SDN) is a new networking paradigm in which the control plane and data plane are decoupled. Throughout the recent years, a number of architectures have emerged for protocol-independent packet processing. One such architecture is the Protocol Independent Switch Architecture (PISA). It is a programmable and protocol-independent architecture composed of a number of Match and Action stages. Inside each of these stages is a crossbar to generate the search key and another crossbar to provide the input to the Action Units. In this paper, we design and explore alternative interconnection schemes with the aim of finding the most area- and power-efficient interconnection structure. Moreover, we propose further modifications to the interconnection structure, as a result of which the on-chip area of both match and action crossbars will be reduced by more than 70 % and power dissipation will be reduced by 25.8 % and 23.1 % for match and action crossbars respectively.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Research group: Wireless Communications and Positioning, University of Bologna
Contributors: Zolfaghari, H., Rossi, D., Nurmi, J.
Publication date: 1 May 2019

Host publication information
Title of host publication: 2019 IEEE 20th International Conference on High Performance Switching and Routing, HPSR 2019
Publisher: IEEE
ISBN (Electronic): 9781728116860

Publication series
Name: IEEE International Conference on High Performance Switching and Routing, HPSR
ISSN (Print): 2325-5595
ISSN (Electronic): 2325-5609
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
Keywords: Crossbar, Protocol Independent Switch Architecture, Software Defined Networking
Electronic versions:

Reducing crossbar costs in the match-action pipeline 2019
DOIs:

10.1109/HPSR.2019.8808105
URLs:

http://urn.fi/URN:NBN:fi:tuni-202002272402

Bibliographical note
jufoid=72023
Source: Scopus
Source ID: 85071943335
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Teaching for virtual work
Universities are still mainly preparing students for the world, where 'do something useful', i.e. 'do something with your hands' was the main principle and work was done during strictly regulated time. But world has changed and traditional areas of human activity (what also are the main target in University courses) are rapidly diminishing. More important have become virtual products - computer programs, mobile apps, social networks, new types of digital currencies, IOT (voice in your bathroom suggesting to buy the next model of Alexa), video games, interactive TV, virtual reality etc. Most of these new areas are not present in current curricula and there are problems with involving them in curricula - (working) students know (some aspects of) these areas better than many of university teachers, since corresponding knowledge is not yet present in textbooks - it is present only on Internet. The Internet strongly influences both what we teach and how we teach.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Tallinn University of Technology, University of Lapland
Contributors: Henno, J., Jaakkola, H., Mäkelä, J.
Number of pages: 9
Pages: 818-826
Publication date: 1 May 2019

Host publication information
Title of host publication: 2019 42nd International Convention on Information and Communication Technology, Electronics and Microelectronics, MIPRO 2019 - Proceedings
Publisher: IEEE
Editors: Skala, K., Car, Z., Pale, P., Huljenic, D., Janjic, M., Koricic, M., Sruk, V., Ribaric, S., Grbac, T. G., Butkovic, Z., Cicin-Sain, M., Skvorc, D., Mauher, M., Babic, S., Gros, S., Vrdoljak, B., Tijan, E.
ISBN (Electronic): 9789532330984
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems, Energy Engineering and Power Technology, Electrical and Electronic Engineering, Electronic, Optical and Magnetic Materials
DOIs:

10.23919/MIPRO.2019.8756778
URLs:

http://docs.mipro-proceedings.com/proceedings/mipro_2019_proceedings.pdf
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

A Semantic Meta-Model Repository for Lightweight M2M
One of the biggest problems in managing devices for the Internet of Things (IoT) is the ability for a management server to independently discover and retrieve data models for vendor-specific devices. At the same time, several device management methods also lack methods for device vendors to share their data models in a consistent manner. This paper presents the design and implementation of a repository that can flexibly accommodate many needs with regards to these issues, and allows device vendors to publish semantically similar data models as well as attach meta-data to these models. A Machine-to-Machine (M2M) communication interface also allows a management server to communicate with the repository. We show how these techniques can be used with the Lightweight Machine-to-Machine (LWM2M) standard.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Research area: Information security, Ericsson
Contributors: Silverajan, B., Zhao, H., Kamath, A.
Number of pages: 5
Pages: 468-472
Publication date: 11 Apr 2019

Host publication information
Title of host publication: 2018 IEEE International Conference on Communication Systems, ICCS 2018
Publisher: IEEE
ISBN (Electronic): 9781538678640
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems and Management, Aerospace Engineering

Keywords: data model repository, IoT device management, LWM2M
DOIs:

10.1109/ICCS.2018.8689185
Source: Scopus
Source ID: 85065038511
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Exploiting Multipath Terahertz Communications for Physical Layer Security in beyond 5G Networks

Terahertz (THz) band communications, capable of achieving the theoretical capacity of up to several terabits-per-second, are one of the attractive enablers for beyond 5G wireless networks. THz systems will use extremely directional narrow beams, allowing not only to extend the communication range but also to partially secure the data already at the physical layer. The reason is that, in most cases, the Attacker has to be located within the transmitter beam in order to eavesdrop the message. However, even the use of very narrow beams results in the considerably large area around the receiver, where the Attacker can capture all the data. In this paper, we study how to decrease the message eavesdropping probability by leveraging the inherent multi-path nature of the THz communications. We particularly propose sharing the data transmission over multiple THz propagation paths currently available between the communicating entities. We show that, at a cost of the slightly reduced link capacity, the message eavesdropping probability in the described scheme decreases significantly even when several Attackers operate in a cooperative manner. The proposed solution can be utilized for the transmission of the sensitive data, as well as to secure the key exchange in THz band networks beyond 5G.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Research group: Wireless Communications and Positioning, State University of New York
Contributors: Petrov, V., Moltchanov, D., Jornet, J. M., Koucheryavy, Y.
Number of pages: 8
Pages: 865-872
Publication date: 1 Apr 2019

Host publication information

Title of host publication: INFOCOM 2019 - IEEE Conference on Computer Communications Workshops, INFOCOM WKSHPS 2019
Publisher: IEEE
ISBN (Electronic): 9781728118789
ASJC Scopus subject areas: Hardware and Architecture, Signal Processing, Information Systems and Management, Safety, Risk, Reliability and Quality, Computer Networks and Communications
Electronic versions:

Exploiting Multipath Terahertz Communications 2019
DOIs:

10.1109/INFCOMW.2019.8845312
URLs:

http://urn.fi/URN:NBN:fi:tuni-202002031781
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Sensing-throughput tradeoff for superior selective reporting-based spectrum sensing in energy harvesting HCRNs

In this paper, we investigate the performance of conventional cooperative sensing (CCS) and superior selective reporting (SSR)-based cooperative sensing in an energy harvesting (EH)-enabled heterogeneous cognitive radio network (HCRN). In particular, we derive expressions for the achievable throughput of both schemes and formulate nonlinear integer programming problems, in order to find the throughput-optimal set of spectrum sensors scheduled to sense a particular channel, given primary user (PU) interference and EH constraints. Furthermore, we present novel solutions for the underlying optimization problems based on the cross-entropy (CE) method, and compare the performance with exhaustive search and greedy algorithms. Finally, we discuss the tradeoff between the average achievable throughput of the SSR and CCS schemes, and highlight the regime where the SSR scheme outperforms the CCS scheme. Notably, we show that there is an inherent tradeoff between the channel available time and the detection accuracy. Our numerical results show that, as the number of spectrum sensors increases, the channel available time gains a higher priority in an HCRN, as opposed to detection accuracy.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Electrical Engineering
Contributors: Kishore, R., Gurugopinath, S., Muhaidat, S., Sofotasios, P. C., Dobre, O. A., Al-Dhahir, N.
Number of pages: 12

Pages: 330-341
Publication date: 22 Mar 2019
Peer-reviewed: Yes

Publication information
Journal: IEEE Transactions on Cognitive Communications and Networking
Volume: 5
Issue number: 2
Article number: 8672813
ISSN (Print): 2332-7731
Ratings:

Scopus rating (2019): CiteScore 6.5 SJR 1.802 SNIP 2.427
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Computer Networks and Communications, Artificial Intelligence
Keywords: Achievable throughput, cognitive radio networks, cross-entropy algorithm, heterogeneous networks, superior selective reporting
DOIs:

10.1109/TCCN.2019.2906915
Source: Scopus
Source ID: 85063413206
Research output: Contribution to journal › Article › Scientific › peer-review

Advancements in Solution Processable Devices using Metal Oxides For Printed Internet-of-Things Objects
Internet-of-things (IoT) objects are expected to exceed 75 billion objects by 2020, and a large part of the expansion is expected to be at a finer granularity than existing silicon-based IoT objects (i.e. tablets and cell phones) can deliver [1]. Currently, placing a room light or a thermostat on the internet for remote control is considered progressive. However, if printed electronics can achieve performance increases, then IoT objects could be affixed to almost anything, such as coffee creamer cartons, cereal boxes, or that missing sock. Each of these IoT objects could be driving a sensor, perhaps position, temperature or pressure, essentially a multitude of applications. In order for IoT objects to emulate a simple postage stamp, with self-powering from energy scavenging and local energy storage, all housed in a non-toxic flexible form factor, advances in solution processable devices need to occur.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Ohio State University, Wayne State University
Contributors: Berger, P. R., Li, M., Mattei, R. M., Niang, M. A., Talisa, N., Tripepi, M., Harris, B., Bhalerao, S. R., Chowdhury, E. A., Winter, C. H., Lupo, D.
Number of pages: 3
Pages: 160-162
Publication date: 1 Mar 2019

Host publication information
Title of host publication: 2019 Electron Devices Technology and Manufacturing Conference, EDTM 2019
Publisher: IEEE
ISBN (Electronic): 9781538665084
ASJC Scopus subject areas: Electrical and Electronic Engineering, Electronic, Optical and Magnetic Materials, Instrumentation, Hardware and Architecture
Keywords: ALD, CMOS and SOI, energy scavenging, IoT, low-power electronics, Manufacturing, NDR, tunnel diodes
DOIs:

10.1109/EDTM.2019.8731322
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

A Framework for Design and Implementation of Adaptive Digital Predistortion Systems
Digital predistortion (DPD) has important applications in wireless communication for smart systems, such as, for example, in Internet of Things (IoT) applications for smart cities. DPD is used in wireless communication transmitters to counteract distortions that arise from nonlinearities, such as those related to amplifier characteristics and local oscillator leakage. In this paper, we propose an algorithm-architecture-integrated framework for design and implementation of adaptive DPD systems. The proposed framework provides energy-efficient, real-time DPD performance, and enables efficient reconfiguration of DPD architectures so that communication can be dynamically optimized based on time-varying communication requirements. Our adaptive DPD design framework applies Markov Decision Processes (MDPs) in novel ways to generate optimized runtime control policies for DPD systems. We present a GPU-based adaptive DPD system that is derived using our design framework, and demonstrate its efficiency through extensive experiments.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Research area: Computer engineering, Computing Sciences, University of Maryland , Georgia Institute of Technology, Department of Electrical and Computer Engineering
Contributors: Li, L., Deaville, P., Sapio, A., Anttila, L., Valkama, M., Wolf, M., Bhattacharyya, S. S.
Number of pages: 5
Pages: 112-116
Publication date: 1 Mar 2019

Host publication information
Title of host publication: Proceedings 2019 IEEE International Conference on Artificial Intelligence Circuits and Systems, AICAS 2019
Publisher: IEEE
ISBN (Electronic): 9781538678848
ASJC Scopus subject areas: Artificial Intelligence, Hardware and Architecture, Electrical and Electronic Engineering
Keywords: dataflow modeling, digital predistortion, Markov decision processes, Smart systems
DOIs:

10.1109/AICAS.2019.8771476
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Challenges of Multi-Factor Authentication for Securing Advanced IoT Applications
The unprecedented proliferation of smart devices together with novel communication, computing, and control technologies have paved the way for A-IoT. This development involves new categories of capable devices, such as high-end wearables, smart vehicles, and consumer drones aiming to enable efficient and collaborative utilization within the smart city paradigm. While massive deployments of these objects may enrich people's lives, unauthorized access to said equipment is potentially dangerous. Hence, highly secure human authentication mechanisms have to be designed. At the same time, human beings desire comfortable interaction with the devices they own on a daily basis, thus demanding authentication procedures to be seamless and user-friendly, mindful of contemporary urban dynamics. In response to these unique challenges, this work advocates for the adoption of multi-factor authentication for A-IoT, such that multiple heterogeneous methods - both well established and emerging - are combined intelligently to grant or deny access reliably. We thus discuss the pros and cons of various solutions as well as introduce tools to combine the authentication factors, with an emphasis on challenging smart city environments. We finally outline the open questions to shape future research efforts in this emerging field.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Electrical Engineering, National Research University Higher School of Economics, ITMO University, Electrical Engineering Department, University of California, Los Angeles (UCLA)
Contributors: Ometov, A., Petrov, V., Bezzateev, S., Andreev, S., Koucheryavy, Y., Gerla, M.
Number of pages: 7
Pages: 82-88
Publication date: 1 Mar 2019
Peer-reviewed: Yes

Publication information
Journal: IEEE Network
Volume: 33
Issue number: 2
ISSN (Print): 0890-8044
Ratings:

Scopus rating (2019): CiteScore 21.6 SJR 2.773 SNIP 3.323
Original language: English
ASJC Scopus subject areas: Software, Information Systems, Hardware and Architecture, Computer Networks and Communications
Electronic versions:

Challenges of Multi-Factor Authentication for Securing Advanced IoT (A-IoT) Applications
DOIs:

10.1109/MNET.2019.1800240
URLs:

http://urn.fi/URN:NBN:fi:tuni-202001151303
Source: Scopus
Source ID: 85063775257
Research output: Contribution to journal › Article › Scientific › peer-review

Elastic Neural Networks for Classification

In this work we propose a framework for improving the performance of any deep neural network that may suffer from vanishing gradients. To address the vanishing gradient issue, we study a framework, where we insert an intermediate output branch after each layer in the computational graph and use the corresponding prediction loss for feeding the gradient to the early layers. The framework-which we name Elastic network-is tested with several well-known networks on CIFAR10 and CIFAR100 datasets, and the experimental results show that the proposed framework improves the accuracy on both shallow networks (e.g., MobileNet) and deep convolutional neural networks (e.g., DenseNet). We also identify the types of networks where the framework does not improve the performance and discuss the reasons. Finally, as a side product, the computational complexity of the resulting networks can be adjusted in an elastic manner by selecting the output branch according to current computational budget.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Computing Sciences, Research area: Computer engineering, University of Maryland
Contributors: Zhou, Y., Bai, Y., Bhattacharyya, S. S., Huttunen, H.
Number of pages: 5
Pages: 251-255
Publication date: 1 Mar 2019

Host publication information

Title of host publication: Proceedings 2019 IEEE International Conference on Artificial Intelligence Circuits and Systems, AICAS 2019
Publisher: IEEE
ISBN (Electronic): 9781538678848
ASJC Scopus subject areas: Artificial Intelligence, Hardware and Architecture, Electrical and Electronic Engineering
Keywords: classification, deep convolutional neural network, regularization, vanishing gradient
DOIs:
10.1109/AICAS.2019.8771475

Bibliographical note

INT=comp,"Bai, Yue"
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Analysis of an efficient parallel implementation of active-set Newton algorithm

This paper presents an analysis of an efficient parallel implementation of the active-set Newton algorithm (ASNA), which is used to estimate the nonnegative weights of linear combinations of the atoms in a large-scale dictionary to approximate an observation vector by minimizing the Kullback–Leibler divergence between the observation vector and the approximation. The performance of ASNA has been proved in previous works against other state-of-the-art methods. The implementations analysed in this paper have been developed in C, using parallel programming techniques to obtain a better performance in multicore architectures than the original MATLAB implementation. Also a hardware analysis is performed to check the influence of CPU frequency and number of CPU cores in the different implementations proposed. The new implementations allow ASNA algorithm to tackle real-time problems due to the execution time reduction obtained.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing, Research group: Audio research group - ARG, Universitat Politècnica de València
Contributors: San Juan Sebastián, P., Virtanen, T., Garcia-Molla, V. M., Vidal, A. M.
Number of pages: 12
Pages: 1298-1309
Publication date: Mar 2019
Peer-reviewed: Yes
Early online date: 19 May 2018

Publication information

Journal: Journal of Supercomputing
Volume: 75
Issue number: 3
ISSN (Print): 0920-8542
Ratings:
Scopus rating (2019): CiteScore 3.9 SJR 0.432 SNIP 1.181
Original language: English
ASJC Scopus subject areas: Software, Theoretical Computer Science, Information Systems, Hardware and Architecture

Keywords: Convex optimization, Multicore, Newton algorithm, Parallel computing, Sparse representation
DOIs:
10.1007/s11227-018-2423-5
Source: Scopus
Source ID: 85047129085
Research output: Contribution to journal › Article › Scientific › peer-review

LordCore: Energy-Efficient OpenCL-Programmable Software-Defined Radio Coprocessor

This paper proposes a single instruction multiple data (SIMD) processor, which is programmed with high-level OpenCL language. The low-power processor is customized for executing multiple-input-multiple-output (MIMO) detection algorithms at a high performance while consuming very little power making it suitable for software-defined radio (SDR) applications. The novel combination of SIMD operations on a transport programmed multicore datapath allows saving power on both the execution front end and the back end, leading to very good energy efficiency with a compiler programmable design. We demonstrate the feasibility of the architecture with the layered orthogonal lattice detector and minimum mean-square-error MIMO algorithms, which can be used as a software-defined radio implementation of the 3GPP local thermal equilibrium r11 standard. Compared to other state-of-the-art SDR architectures, the proposed design adds features that improve programmer productivity with an insignificant power and area impact

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Computing Sciences, Research area: Computer engineering, Nokia Technologies, NVIDIA
Contributors: Kultala, H., Viitanen, T., Berg, H., Jääskeläinen, P., Multanen, J., Kokkonen, M., Raiskila, K., Zetterman, T., Takala, J.
Pages: 1029-1042
Publication date: 26 Feb 2019
Peer-reviewed: Yes

Publication information

Journal: IEEE Transactions on Very Large Scale Integration (VLSI) Systems
Volume: 27
Issue number: 5
ISSN (Print): 1063-8210
Ratings:
Scopus rating (2019): CiteScore 4.9 SJR 0.561 SNIP 1.633
Original language: English
ASJC Scopus subject areas: Hardware and Architecture
Keywords: SIMD, OpenCL, MIMO, processor
DOIs:
10.1109/TVLSI.2019.2897508

Bibliographical note

EXT="Viitanen, Timo"
Research output: Contribution to journal › Article › Scientific › peer-review

ALMARVI System Solution for Image and Video Processing in Healthcare, Surveillance and Mobile Applications

ALMARVI is a collaborative European research project funded by Artemis involving 16 industrial as well as academic partners across 4 countries, working together to address various computational challenges in image and video processing in 3 application domains: healthcare, surveillance and mobile. This paper is an editorial for a special issue discussing the integrated system created by the partners to serve as a cross-domain solution for the project. The paper also introduces the partner articles published in this special issue to discuss the various technological developments achieved within ALMARVI spanning all system layers, from hardware to applications. We illustrate the challenges faced within the project based on use cases from the three targeted application domains, and how these can address the 4 main project objectives addressing 4 challenges faced by high performance image and video processing systems: massive data rate, low power consumption, composability and robustness. We present a system stack composed of algorithms, design frameworks and platforms as a solution to these challenges. Finally, the use cases from the three different application domains are mapped on the system stack solution and are evaluated based on their performance for each of the 4 ALMARVI objectives.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Pervasive Computing, Delft University of Technology, Philips Healthcare Nederland
Contributors: Al-Ars, Z., van der Vlugt, S., Jääskeläinen, P., van der Linden, F.

Pages: 1-7
Publication date: Jan 2019
Peer-reviewed: Yes
Early online date: 2018

Publication information
Journal: Journal of Signal Processing Systems
Volume: 91
Issue number: 1
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2019): CiteScore 2.4 SJR 0.298 SNIP 0.833
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
DOIs:

10.1007/s11265-018-1423-2
Source: Scopus
Source ID: 85057058836
Research output: Contribution to journal › Article › Scientific › peer-review

Digital Predistortion for 5G Small Cell: GPU Implementation and RF Measurements
In this paper, we present a high data rate implementation of a digital predistortion (DPD) algorithm on a modern mobile multicore CPU containing an on-chip GPU. The proposed implementation is capable of running in real-time, thanks to the execution of the predistortion stage inside the GPU, and the execution of the learning stage on a separate CPU core. This configuration, combined with the low complexity DPD design, allows for more than 400 Msamples/s sample rates. This is sufficient for satisfying 5G new radio (NR) base station radio transmission specifications in the sub-6 GHz bands, where signal bandwidths up to 100 MHz are specified. The linearization performance is validated with RF measurements on two base station power amplifiers at 3.7 GHz, showing that the 5G NR downlink emission requirements are satisfied.

General information
Publication status: E-pub ahead of print
MoE publication type: A1 Journal article-refereed
Organisations: Electrical Engineering, Computing Sciences, Research area: Computer engineering, Research group: Wireless Communications and Positioning, University of Vaasa (UVA), Tampere University
Contributors: Pascual Campo, P., Lampu, V., Meirhaeghe, A., Boutellier, J., Anttila, L., Valkama, M.
Number of pages: 12
Publication date: 2019
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2019): CiteScore 2.4 SJR 0.298 SNIP 0.833
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: 5G, Digital predistortion (DPD), GPU, High data rate, Real-time
Electronic versions:

PascualCampo2019_Article_DigitalPredistortionFor5GSmall
DOIs:

10.1007/s11265-019-01502-4
URLs:

http://urn.fi/URN:NBN:fi:tuni-202001171372

Bibliographical note
INT=comp,"Meirhaeghe, Alexandre"
Source: Scopus
Source ID: 85077054281
Research output: Contribution to journal › Article › Scientific › peer-review

Farm detection based on deep convolutional neural nets and semi-supervised green texture detection using VIS-NIR satellite image

Farm detection using low resolution satellite images is an important topic in digital agriculture. However, it has not received enough attention compared to high-resolution images. Although high resolution images are more efficient for detection of land cover components, the analysis of low-resolution images are yet important due to the low-resolution repositories of the past satellite images used for timeseries analysis, free availability and economic concerns. The current paper addresses the problem of farm detection using low resolution satellite images. In digital agriculture, farm detection has significant role for key applications such as crop yield monitoring. Two main categories of object detection strategies are studied and compared in this paper; First, a two-step semi-supervised methodology is developed using traditional manual feature extraction and modelling techniques; the developed methodology uses the Normalized Difference Moisture Index (NDMI), Grey Level Co-occurrence Matrix (GLCM), 2-D Discrete Cosine Transform (DCT) and morphological features and Support Vector Machine (SVM) for classifier modelling. In the second strategy, high-level features learnt from the massive filter banks of deep Convolutional Neural Networks (CNNs) are utilised. Transfer learning strategies are employed for pretrained Visual Geometry Group Network (VGG-16) networks. Results show the superiority of the high-level features for classification of farm regions.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electrical Engineering, Coventry University
Contributors: Sharifzadeh, S., Tata, J., Tan, B.
Number of pages: 9
Pages: 100-108
Publication date: 2019

Host publication information

Title of host publication: DATA 2019 - Proceedings of the 8th International Conference on Data Science, Technology and Applications
Publisher: SCITEPRESS
Editors: Hammoudi, S., Quix, C., Bernardino, J.
ISBN (Electronic): 9789897583773
ASJC Scopus subject areas: Hardware and Architecture, Information Systems, Software, Computer Networks and Communications
Keywords: Classification, Convolutional Neural Nets (CNNs), Digital Agriculture, Satellite Image, Supervised Feature Extraction
Electronic versions:

DATA_2019_68
DOIs:

10.5220/0007954901000108
URLs:

http://urn.fi/URN:NBN:fi:tuni-201910234035
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

On the Secrecy Capacity of Fisher-Snedecor F Fading Channels

The performance of physical-layer security of the classic Wyner's wiretap model over Fisher-Snedecor composite fading channels is considered in this work. Specifically, F the main channel (i.e., between the source and the legitimate destination) and the eavesdropper's channel (i.e., between the source and the illegitimate destination) are assumed to experience independent quasi-static Fisher-Snedecor fading conditions, which have been shown to be encountered in realistic wireless transmission scenarios in conventional and emerging communication systems. In this context, exact closed-form expressions for the average secrecy capacity (ASC) and the probability of non-zero secrecy capacity (PNSC) are derived. Additionally, an asymptotic analytical expression for the ASC is presented. The impact of shadowing and multipath fading on the secrecy performance is investigated. Our results show that increasing the fading parameter of the main channel and/or the shadowing parameter of the eavesdropper's channel improves the secrecy performance. The analytical results are compared with Monte-Carlo simulations to validate the analysis.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research group: Wireless Communications and Positioning, Electrical Engineering, German Jordanian University, Khalifa University, University of Surrey, Queen's University, Belfast, Northern Ireland, Manchester Metropolitan University, Universidade Federal do Ceara
Contributors: Badarneh, O. S., Sofotasios, P. C., Muhaidat, S., Cotton, S. L., Rabie, K., Al-Dhahir, N.
Number of pages: 6
Pages: 102-107
Publication date: 26 Dec 2018

Host publication information

Title of host publication: 2018 14th International Conference on Wireless and Mobile Computing, Networking and Communications, WiMob 2018
Publisher: IEEE
ISBN (Electronic): 9781538668764
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Software
DOIs:

10.1109/WiMOB.2018.8589137
Source: Scopus
Source ID: 85060830976
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

The N*Fisher-Snedecor F Cascaded Fading Model

The Fisher-Snedecor F distribution was recently proposed as an accurate and tractable composite fading model in the context of device-to-device communications. The present work derives the product of the Fisher-Snedecor F composite fading model, which is useful in characterizing fading effects in numerous realistic communication scenarios. To this end, novel analytic expressions are first derived for the probability density function, the cumulative distribution function and the moment of the product of N statistically independent, but not necessarily identically distributed, Fisher-Snedecor F random variables. Capitalizing on these expressions, we derive tractable closed-form expressions for channel quality estimation of the proposed model as well as the corresponding outage probability and average bit error probability for binary modulations. The offered results are corroborated by extensive Monte-Carlo simulation results, which verify the validity of the derived expressions. It is shown that the number of cascaded channels affects considerably the corresponding performance, as a variation of over an order of magnitude is observed across all signal-to-noise ratio regimes.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research group: Wireless Communications and Positioning, Electrical Engineering, German Jordanian University, Khalifa University, University of Surrey, Queen's University, Belfast, Northern Ireland, Manchester Metropolitan University, Universidade Federal do Ceara
Contributors: Badarneh, O. S., Muhaidat, S., Sofotasios, P. C., Cotton, S. L., Rabie, K., Da Costa, D. B.
Publication date: 26 Dec 2018

Host publication information

Title of host publication: 2018 14th International Conference on Wireless and Mobile Computing, Networking and Communications, WiMob 2018
Publisher: IEEE
ISBN (Electronic): 9781538668764
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Software
DOIs:

10.1109/WiMOB.2018.8589124
Source: Scopus
Source ID: 85060794044
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Efficient Solving of Markov Decision Processes on GPUs Using Parallelized Sparse Matrices

Markov Decision Processes (MDPs) provide important capabilities for facilitating the dynamic adaptation of hardware and software configurations to the environments in which they operate. However, the use of MDPs in embedded signal processing systems is limited because of the large computational demands for solving this class of system models. This paper presents Sparse Parallel Value Iteration (SPVI), a new algorithm for solving large MDPs on resource-constrained embedded systems that are equipped with mobile GPUs. SPVI leverages recent advances in parallel solving of MDPs and adds sparse linear algebra techniques to significantly outperform the state-of-the-art. The method and its application are described in detail, and demonstrated with case studies that are implemented on an NVIDIA Tegra K1 System On Chip (SoC). The experimental results show execution time improvements in the range of 65 % -78% for several applications. SPVI also lifts restrictions required by other MDP solver approaches, making it more widely compatible with large classes of optimization problems.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research area: Computer engineering, Computing Sciences, University of Maryland, Department of Electrical and Computer Engineering, Georgia Institute of Technology
Contributors: Sapio, A., Bhattacharyya, S. S., Wolf, M.
Number of pages: 6

Pages: 13-18
Publication date: Dec 2018

Host publication information
Title of host publication: 2018 Conference on Design and Architectures for Signal and Image Processing, DASIP 2018
Publisher: IEEE COMPUTER SOCIETY PRESS
ISBN (Electronic): 9781538682371

Publication series
Name: Conference on Design and Architectures for Signal and Image Processing, DASIP
ISSN (Print): 2164-9766
ASJC Scopus subject areas: Computer Graphics and Computer-Aided Design, Computer Vision and Pattern Recognition, Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
Keywords: CUDA, GPU, Markov decision processes, MDP, Sparsity, Value iteration
DOIs:

10.1109/DASIP.2018.8596969

Bibliographical note
jufoid=71852
Source: Scopus
Source ID: 85061388518
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Power mitigation of a heterogeneous multicore architecture on FPGA/ASIC by DFS/DVFS techniques
This article presents an integrated self-aware computing model in a Heterogeneous Multicore Architecture (HMA) to mitigate the power dissipation of an Orthogonal Frequency-Division Multiplexing (OFDM) receiver. The proposed platform consists of template-based Coarse-Grained Reconfigurable Array (CGRA) devices connected through a Network-on-Chip (NoC) around a few Reduced Instruction-Set Computing (RISC) cores. The self-aware computing model exploits Feedback Control System (FCS) which constantly monitors the execution-time of each core and dynamically scales the operating frequency of each node of the NoC depending on the worst execution-time. Therefore, the performance of the overall system is equalized towards a desired level besides mitigating the power dissipation. Measurement results obtained from Field-Programmable Gate Array (FPGA) synthesis show up to 20.2% dynamic power dissipation and 16.8% total power dissipation savings. Since FCS technique can be employed for scaling the frequency and the voltage and on the other hand, voltage supply cannot be scaled on the FPGA-based prototyped platform, the implementation is also estimated in 28nm Ultra-Thin Body and Buried oxide (UTBB) Fully-Depleted Silicon-On-Insulator (FD-SOI) Application-Specific Integrated Circuit (ASIC) technology to scale voltage in addition to frequency and get more benefits in terms of dynamic power dissipation reduction. Subsequent to synthesizing the whole platform on ASIC and scaling the voltage and frequency simultaneously as a Dynamic Voltage and Frequency Scaling (DVFS) method, significant dynamic power dissipation savings by 5.97X against Dynamic Frequency Scaling (DFS) method were obtained.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Electronics and Communications Engineering, Research group: System-on-Chip for GNSS, Wireless Communications and Cyber-Physical Embedded Computing, University of Bologna
Contributors: Nouri, S., Rossi, D., Nurmi, J.
Number of pages: 10
Pages: 259-268
Publication date: 1 Nov 2018
Peer-reviewed: Yes

Publication information
Journal: Microprocessors and Microsystems
Volume: 63
ISSN (Print): 0141-9331
Ratings:

Scopus rating (2018): CiteScore 2.5 SJR 0.264 SNIP 0.941
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture, Computer Networks and Communications, Artificial Intelligence
Keywords: Accelerator, ASIC, CGRA, Channel estimation, DVFS, FCS, FFT, FPGA, Frequency offset estimation, Heterogeneous, Multicore, Network-on-Chip, OFDM, Power mitigation, Receiver, Reconfigurable, Time synchronization
Electronic versions:

Power mitigation of a heterogeneous multicore architecture 2018
DOIs:

10.1016/j.micpro.2018.09.010
URLs:
http://urn.fi/URN:NBN:fi:tuni-202002252335
Source: Scopus
Source ID: 85054428146
Research output: Contribution to journal › Article › Scientific › peer-review

A Low-Cost High-Speed Self-Checking Carry Select Adder with Multiple-Fault Detection

Employing cost-efficient, high-speed and fault-tolerant processing units is an essential goal in the design of current processors. In this paper, the carry select adder (CSeA) as one of the fastest adders is augmented respecting multiple-fault detection, delay, power and required area. In this way, based on the concept of a self-checking full adder, an m-bit logic-optimized self-checking single-stage CSeA is designed in which at most m concurrent faults can be detected. Then, based on a delay analysis, a new grouping structure for the self-checking multi-stage CSeA apart from the conventional square-root (SQRT) grouping is proposed to optimize the overall delay for different adder sizes. The proposed grouping structure decreases the power overhead, as well. Experimental results show that as well as an acceptable multiple-fault detection capability, noticeable improvements are achieved in delay and power consumption compared to the previous self-checking CSeA designs. The proposed CSeA reaches in average 20% power reduction and 34% speed improvement in different sizes compared to the best existing design.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Electronics and Communications Engineering, Research group: Wireless Communications and Positioning , Research group: System-on-Chip for GNSS, Wireless Communications and Cyber-Physical Embedded Computing, Babol Noshirvani University of Technology
Contributors: Valinataj, M., Mohammadnejad, A., Nurmi, J.
Number of pages: 12
Pages: 16-27
Publication date: Nov 2018
Peer-reviewed: Yes
Early online date: 17 Sep 2018

Publication information

Journal: Microelectronics journal
Volume: 81
ISSN (Print): 0959-8324
Ratings:
Scopus rating (2018): CiteScore 2.7 SJR 0.264 SNIP 0.852
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
DOIs:
10.1016/j.mejo.2018.08.014
Research output: Contribution to journal › Article › Scientific › peer-review

Toward Efficient Execution of RVC-CAL Dataflow Programs on Multicore Platforms

The increasing number of cores in System on Chips (SoC) has introduced challenges in software parallelization. As an answer to this, the dataflow programming model offers a concurrent and reusability promoting approach for describing applications. In this work, a runtime for executing Dataflow Process Networks (DPN) on multicore platforms is proposed. The main difference between this work and existing methods is letting the operating system perform Central processing unit (CPU) load-balancing freely, instead of limiting thread migration between processing cores through CPU affinity. The proposed runtime is benchmarked on desktop and server multicore platforms using five different applications from video coding and telecommunication domains. The results show that the proposed method offers significant improvements over the state-of-art, in terms of performance and reliability.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Pervasive Computing, Research area: Computer engineering, Univ of Oulu
Contributors: Hautala, I., Boutellier, J., Nyländen, T., Silvén, O.
Number of pages: 11
Pages: 1507-1517
Publication date: Nov 2018
Peer-reviewed: Yes
Early online date: 9 Feb 2018

Publication information
Journal: Journal of Signal Processing Systems
Volume: 90
Issue number: 11
ISSN (Print): 1939-8018
Ratings:
Scopus rating (2018): CiteScore 1.7 SJR 0.203 SNIP 0.61
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Dataflow Process Networks, Multicore, Orcc, RVC-CAL
DOIs:
10.1007/s11265-018-1339-x
Source: Scopus
Source ID: 85041532591
Research output: Contribution to journal › Article › Scientific › peer-review

Visualization of memory map information in embedded system design
Data compression is a common requirement for displaying large amounts of information. The goal is to reduce visual clutter. The approach given in this paper uses an analysis of a data set to construct a visual representation. The visualization is compressed using the address ranges of the memory structure. This method produces a compressed version of the initial visualization, retaining the same information as the original. The presented method has been implemented as a Memory Designer tool for ASIC, FPGA and embedded systems using IP-XACT. The Memory Designer is a user-friendly tool for model based embedded system design, providing access and adjustment of the memory layout from a single view, complementing the 'programmer's view' to the system.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Human-Centered Technology (IHTE)
Contributors: Teuho, M., Pekkarinen, E., Hämäläinen, T. D.
Number of pages: 4
Pages: 163-166
Publication date: 12 Oct 2018

Host publication information
Title of host publication: Proceedings - 21st Euromicro Conference on Digital System Design, DSD 2018
Publisher: IEEE
Article number: 8491811
ISBN (Electronic): 9781538673768
ASJC Scopus subject areas: Hardware and Architecture
Keywords: Compression, Data visualization, Display space, Filtering, Memory structure
DOIs:
10.1109/DSD.2018.00040
Source: Scopus
Source ID: 85056487173
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Olfactory display prototype for presenting and sensing authentic and synthetic odors
The aim was to study if odors evaporated by an olfactory display prototype can be used to affect participants' cognitive and emotion-related responses to audio-visual stimuli, and whether the display can benefit from objective measurement of the odors. The results showed that odors and videos had significant effects on participants' responses. For instance, odors increased pleasantness ratings especially when the odor was authentic and the video was congurent with odors. The objective measurement of the odors was shown to be useful. The measurement data was classified with 100 % accuracy removing the need to speculate whether the odor presentation apparatus is working properly.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Faculty of Biomedical Sciences and Engineering, Research group: Sensor Technology and Biomeasurements (STB), Research group: Micro and Nanosystems Research Group
Contributors: Salminen, K., Rantala, J., Isokoski, P., Lehtonen, M., Müller, P., Karjalainen, M., Väliaho, J., Kontunen, A., Nieminen, V., Leivo, J., Telembeci, A. A., Lekkala, J., Kallio, P., Surakka, V.
Number of pages: 5

Pages: 73-77
Publication date: 2 Oct 2018

Host publication information
Title of host publication: ICMI 2018 - Proceedings of the 2018 International Conference on Multimodal Interaction
Publisher: ACM
ISBN (Electronic): 9781450356923
ASJC Scopus subject areas: Computer Science Applications, Computer Vision and Pattern Recognition, Hardware and Architecture, Human-Computer Interaction
Keywords: Emotions, Multimodal interaction, Olfaction
Electronic versions:

olfactory-display-prototype
DOIs:

10.1145/3242969.3242999
URLs:

http://urn.fi/URN:NBN:fi:tuni-201909233451

Bibliographical note
INT=tut-bmt,"Nieminen, Ville"
Source: Scopus
Source ID: 85056660798
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Visualization in the integrated SimPhoNy multiscale simulation framework
We describe three distinct approaches to visualization for multiscale materials modelling research. These have been developed with the framework of the SimPhoNy FP7 EU-project, and complement each other in their requirements and possibilities. All have been integrated via wrappers to one or more of the simulation approaches within the SimPhoNy project. In this manuscript we describe and contrast their features. Together they cover visualization needs from electronic to macroscopic scales and are suited to simulations made on personal computers, workstations or advanced High Performance parallel computers. Examples as well as recommendations for future calculations are presented.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Physics, Technion - Israel Institute of Technology, Natural Resources Institute Finland (Luke), Department of Physics and Nanoscience Center, Jyväskylän yliopisto, Enthought Ltd., Sgenia Solutions, IWM
Contributors: Adler, J., Kulju, S., Hyväluoma, J., Mattila, K., Choi, K., Tziakos, I., Pinte, D., García, G. A., Makushok, Y., Makushok, V., Lama, J., Román-Pérez, G., Hashibon, A., Sadeghi, M., Franklin, N., Silverman, A.
Number of pages: 17
Pages: 45-61
Publication date: 1 Oct 2018
Peer-reviewed: Yes

Publication information
Journal: Computer Physics Communications
Volume: 231
ISSN (Print): 0010-4655
Ratings:

Scopus rating (2018): CiteScore 7.7 SJR 1.262 SNIP 1.889
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Physics and Astronomy(all)
Keywords: Atomistic, Electronic charge density, Fluid, Visualization
DOIs:

10.1016/j.cpc.2018.05.005

Bibliographical note
EXT="Kulju, Sampo"
Source: Scopus
Source ID: 85047534237
Research output: Contribution to journal › Article › Scientific › peer-review

Energy-Delay Trade-offs in Instruction Register File Design
In order to decrease latency and energy consumption, processors use hierarchical memory systems to store temporally and spatially related instructions close to the core. Instruction register file (IRF) is an energy-efficient solution for the lowest level in the instruction memory hierarchy. Being compiler-controlled, it removes the area and energy overheads

involved in cache tag checking and adds flexibility in the separation of the instruction fetch and execution. In this paper, we systematically evaluate for the first time the effect of three IRF design variations on energy and delay against an unoptimized baseline IRF. Having instruction fetch and decode with IRF in the same pipeline stage allows minimal delay branching, but results in low operating clock frequency and impaired energy delay product compared to splitting them into two stages. Assuring instruction presence in IRF before execution with software reduces the area and increases maximum clock frequency compared to assurance with hardware, but requires compiler analysis. With a proposed compiler-analyzed instruction placement and co-designed hardware implementation, energy consumption with the best IRF variant is reduced by 9% on average with EEMBC Coremark and CHStone benchmaks. The energy delay product is improved by 23% when compared to the baseline IRF approach.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Research area: Computer engineering
Contributors: Multanen, J., Kultala, H., Jääskeläinen, P.
Publication date: Oct 2018

Host publication information
Title of host publication: 2018 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)
Publisher: IEEE
ISBN (Print): 978-1-5386-7657-8
ISBN (Electronic): 978-1-5386-7656-1
ASJC Scopus subject areas: Hardware and Architecture
Keywords: Energy efficiency, low power, Computer architecture, Instruction fetch
DOIs:

10.1109/NORCHIP.2018.8573504
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Guest Editorial Special Issue on Multimedia Big Data in Internet of Things

General information
Publication status: Published
MoE publication type: B1 Article in a scientific magazine
Organisations: Signal Processing, Research group: Multimedia Research Group - MRG, Beijing University of Posts and Telecommunications, University of Technology Sydney, IBM Research
Contributors: Ma, H., Yu, S., Gabbouj, M., Mueller, P.
Number of pages: 3
Pages: 3405-3407
Publication date: Oct 2018
Peer-reviewed: No

Publication information
Journal: IEEE Internet of Things Journal
Volume: 5
Issue number: 5
Article number: 8534720
ISSN (Print): 2327-4662
Ratings:

Scopus rating (2018): CiteScore 9.4 SJR 1.396 SNIP 4.174
Original language: English
ASJC Scopus subject areas: Signal Processing, Information Systems, Hardware and Architecture, Computer Science Applications, Computer Networks and Communications
DOIs:

10.1109/JIOT.2018.2875580
Source: Scopus
Source ID: 85056768996
Research output: Contribution to journal › Editorial › Scientific

LoTTA: Energy-Efficient Processor for Always-on Applications
Various use cases in the era of Internet-of-Things (IoT) demand processor devices to have low energy consumption in order to maximize the battery life. In addition to energy constraints, there is often a need to both swiftly execute control-oriented code to provide low reaction times and to occasionally perform real time signal processing tasks efficiently. As a response to these requirements, we propose LoTTA, an extremely energy-efficient exposed datapath core. Its transport-triggered programming model helps in lowering the execution latency via low cost data forwarding. Control efficiency is

achieved by an optimized control unit with zero delay slot branches and predicated execution. An instruction register file is included for frequently executed program hot spots to reduce the instruction stream energy consumption. These features allow the processor to execute CHStone and EEMBC CoreMark benchmarks on average with 19% fewer cycles compared to a 6-stage LM32, a traditional RISC core with similar datapath resources. The core consumes 53% less energy on average compared to the RISC core. When including the instruction stream overheads, in the best case, LoTTA saves 79% energy, and on average 40%.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Research area: Computer engineering
Contributors: Multanen, J., Kultala, H., Jääskeläinen, P., Viitanen, T., Tervo, A., Takala, J.
Publication date: Oct 2018

Host publication information
Title of host publication: 2018 IEEE International Workshop on Signal Processing Systems (SiPS)
Publisher: IEEE
ISBN (Print): 978-1-5386-6319-6
ISBN (Electronic): 978-1-5386-6318-9
ASJC Scopus subject areas: Computer Science(all), Hardware and Architecture, Signal Processing
Keywords: Energy efficiency, low power, Computer architecture, IoT, always-on, Processor
Electronic versions:

LoTTA: Energy-Efficient Processor 2018
DOIs:

10.1109/SiPS.2018.8598408
URLs:

http://urn.fi/URN:NBN:fi:tuni-202003102634
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

A Framework for Data Collection, Transformation and Processing in Industrial Systems
Data collection requires homogenization of the data prior to processing it. This can create a challenge to the companies since data have varicose formats and schemas. This paper discusses the implementation of data collection framework using the PLANTCockpit open source platform, which is an integration platform for business processes. The framework is extended to fetch data from heterogeneous sources and then, allow the user to select the relevant data that matches his/her needs. In addition to this, the extendable framework also makes it possible to select the output data structure based on the user's requirements. Defining such a framework can reduce company's efforts for reshaping and modifying their architectures to handle new challenges posed by the ever-changing data. The framework not only restricts one to collection and transformation, but also provides an option to perform available processing techniques on the transformed data structure. The proposed framework has been tested on a cloud-based platform provided by the Cloud Collaborative Manufacturing Networks (C2NET) project.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Automation and Hydraulic Engineering, Research group: Factory automation systems technology
Contributors: Iftikhar, U., Mohammed, W. M., Ferrer, B. R., Lastra, J. L.
Number of pages: 6
Pages: 707-712
Publication date: 24 Sep 2018

Host publication information
Title of host publication: Proceedings - IEEE 16th International Conference on Industrial Informatics, INDIN 2018
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 8471996
ISBN (Electronic): 9781538648292

Publication series
Name: IEEE International Conference on Industrial Informatics
ISSN (Electronic): 2161-2064
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems and Management, Industrial and Manufacturing Engineering
Keywords: Data acquisition, Data Processing, Enterprise resource planning, Web services
DOIs:

10.1109/INDIN.2018.8471996

Source: Scopus
Source ID: 85055516101
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

An ISA-95 based Ontology for Manufacturing Systems Knowledge Description Extended with Semantic Rules

There is a trend about the adoption of Knowledge Representation and Reasoning formalisms, such as ontologies, for industrial automation. For example, semantic models are used as knowledge bases that encapsulate different type of information of manufacturing systems, e.g., statuses and capabilities of their cyber and physical resources. Moreover, these models can be updated and accessed during runtime. In this context, models are becoming a critical part of the system infrastructure for both controlling and monitoring activities. However, models tend to be designed for specific purposes and not standardized. This is an issue because the employed formalisms, such as ontologies, emerged in order to bring an engineering tool for commonly classifying, defining, and sharing information. This article proposes the development of modular ontologies based on different parts of the ISA-95 standard for describing the product, process, and resource information of manufacturing systems. In addition, this research work demonstrates a set of semantic rules that may be used for inferring implicit knowledge of the ontology that permits the automatic checking of the required machines to manufacture different product variants.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Automation and Hydraulic Engineering, Research group: Factory automation systems technology
Contributors: Seyedamir, A., Ferrer, B. R., Lastra, J. L.
Number of pages: 7
Pages: 374-380
Publication date: 24 Sep 2018

Host publication information

Title of host publication: Proceedings - IEEE 16th International Conference on Industrial Informatics, INDIN 2018
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 8471929
ISBN (Electronic): 9781538648292

Publication series

Name: IEEE International Conference on Industrial Informatics
ISSN (Electronic): 2378-363X
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems and Management, Industrial and Manufacturing Engineering
Keywords: Industrial automation, ISA-95, Knowledge representation, Ontology, Semantic rules
DOIs:

10.1109/INDIN.2018.8471929

Bibliographical note

INT=aut,"Seyedamir, Ahmadi"
Source: Scopus
Source ID: 85055527056
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Supporting a Cloud Platform with Streams of Factory Shop Floor Data in the Context of the Intustry 4.0

Industry 4.0 is about the interconnectivity and digitalisation of industrial systems that need to be integrated in order to improve the efficiency of resources and, in turn, processes. Both research and commercial sectors are working towards addressing specific challenges, such as data modelling, collection and processing. A correct manipulation and interpretation of data is critical and, now, more difficult than ever due to the dramatic increment of the amount of data generated at different levels of enterprises. Ultimately, this research work presents a solution, integrated with an existing cloud-based platform, for collecting and processing real-time factory shop floor streams of data. Such solution is an IoT-based development, which consist on both IoT hub and gateway that permit the consumption and communication of device information. The required message exchange is done within state of the art technologies and protocols e.g., MQTT protocol and REST-based interface. The implementation of the solution is demonstrated through an industrial-based scenario.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Automation and Hydraulic Engineering, Research group: Factory automation systems technology, ATOS
Contributors: Mohammed, W. M., Ferrer, B. R., Iftikhar, U., Lastra, J. L., Simarro, J. H.
Number of pages: 6

Pages: 786-791
Publication date: 24 Sep 2018

Host publication information
Title of host publication: Proceedings - IEEE 16th International Conference on Industrial Informatics, INDIN 2018
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 8471981
ISBN (Electronic): 9781538648292

Publication series
Name: IEEE International Conference on Industrial Informatics
ISSN (Electronic): 2378-363X
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems and Management, Industrial and Manufacturing Engineering
Keywords: Cloud computing, Industrial Cyber-Physical Systems, Industrial Internet of Things, Industry 4.0, Real-time data collection
DOIs:

10.1109/INDIN.2018.8471981

Bibliographical note
INT=aut,"Iftikhar, Umer"
Source: Scopus
Source ID: 85055528763
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Towards the Adoption of Cyber-Physical Systems of Systems Paradigm in Smart Manufacturing Environments

Cyber-physical Systems (CPS) in industrial manufacturing facilities demand a continuous interaction with different and a large amount of distributed and networked computing nodes, devices and human operators. These systems are critical to ensure the quality of production and the safety of persons working at the shop floor level. Furthermore, this situation is similar in other domains, such as logistics that, in turn, are connected and affect the overall production efficiency. In this context, this article presents some key steps for integrating three pillars of CPS (production line, logistics and facilities) into the current smart manufacturing environments in order to adopt an industrial Cyber-Physical Systems of Systems (CPSoS) paradigm. The approach is focused on the integration in several digital functionalities in a cloud-based platform to allow a real time multiple devices interaction, data analytics/sharing and machine learning-based global reconfiguration to increase the management and optimization capabilities for increasing the quality of facility services, safety and energy efficiency and industrial productivity. Conceptually, isolated systems may enhance their capabilities by accessing to information of other systems. The approach introduces particular vision, main components, potential and challenges of the envisioned CPSoS. In addition, the description of one scenario for realizing the CPSoS vision is presented. The results herein presented will pave the way for the adoption of CPSoS that can be used as a pilot for further research on this emerging topic.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Automation and Hydraulic Engineering, Research group: Factory automation systems technology, Centre for Automation and Robotics (CAR-CSIC), University of Matanzas
Contributors: Ferrer, B. R., Mohammed, W. M., Martinez Lastra, J. L., Villalonga, A., Beruvides, G., Castano, F., Haber, R. E.
Number of pages: 8
Pages: 792-799
Publication date: 24 Sep 2018

Host publication information
Title of host publication: Proceedings - IEEE 16th International Conference on Industrial Informatics, INDIN 2018
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 8472061
ISBN (Electronic): 9781538648292

Publication series
Name: IEEE International Conference on Industrial Informatics
ISSN (Electronic): 2378-363X
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems and Management, Industrial and Manufacturing Engineering
Keywords: Cyber-Physical Systems, Cyber-Physical Systems of Systems, Industry 4.0, Smart Manufacturing, System of Systems
DOIs:

10.1109/INDIN.2018.8472061
Source: Scopus
Source ID: 85055511921
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Dimensional analysis conceptual modeling supporting adaptable reasoning in simulation-based training

How to measure and train for adaptability has emerged as a priority in military contexts in response to emergent threats and technologies associated with asymmetric warfare. While much research effort has attempted to characterize adaptability in terms of accuracy and response time using traditional executive function cognitive tests, it remains unclear and undefined how adaptability should be measured and thus how simulation-based training should be designed to instigate and modulate adaptable behavior and skills. Adaptable reasoning is well-exemplified in the rescue effort of Apollo 13 by NASA engineers who repurposed available materials available in the spacecraft to retrieve the astronauts safely back to earth. Military leaders have anecdotally referred to adaptability as 'improvised thinking' that repurposes 'blocks of knowledge' to device alternative solutions in response to changes in conditions affecting original tasks while maintaining end-state commander's intent. We review a previous feasibility study that explored the specification of Reusable Modeling Primitives for models and simulation systems building on Dimensional Analysis and Design Structure Matrix for Complexity Management formal methods. This Dimensional Analysis Conceptual Modeling (DACM) paradigm is rooted in science and engineering critical thinking and is consistent with the stated anecdotal premises as it facilitates the objective dimensional decomposition of a problem space to guide the corresponding dimensional composition of possible solutions. Arguably, adaptability also concerns the capability to overcome contradictions, detections, and reductions, which we present in an exemplar addressing the contradiction of increased drag due to increased velocity inherent to torpedoes. We propose that the DACM paradigm may be repurposed as a critical thinking framework for teaching the identification of relevant components in a theater of military operations and how the properties of those components may be repurposed to fashion alternative solutions to tasks involving navigation, call-for-fires, line-of-sight cover, weather and atmospheric effect responses, and others.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Mechanical Engineering and Industrial Systems, Simulated Instruments
Contributors: Coatanea, E., Roca, R.
Number of pages: 8
Pages: 245-252
Publication date: 7 Aug 2018

Host publication information

Title of host publication: 2018 13th System of Systems Engineering Conference, SoSE 2018
Publisher: IEEE
ISBN (Print): 9781538648766
ASJC Scopus subject areas: Computer Networks and Communications, Computer Science Applications, Hardware and Architecture, Control and Systems Engineering, Information Systems and Management
Keywords: Adaptable Reasoning, Conceptual Modeling, Modeling Simulation
DOIs:
10.1109/SYSOSE.2018.8428785
Source: Scopus
Source ID: 85052311344
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Low latency edge rendering scheme for interactive 360 degree virtual reality gaming

This paper describes the core functionality and a proof-of-concept demonstration setup for remote 360 degree stereo virtual reality (VR) gaming. In this end-to-end scheme, the execution of a VR game is off-loaded from an end user device to a cloud edge server in which the executed game is rendered based on user's field of view (FoV) and control actions. Headset and controller feedback is transmitted over the network to the server from which the rendered views of the game are streamed to a user in real-time as encoded HEVC video frames. This approach saves energy and computation load of the end terminals by making use of the latest advancements in network connection speed and quality. In the showcased demonstration, a VR game is run in Unity on a laptop powered by i7 7820HK processor and GTX 1070 GPU. The 360 degree spherical view of the game is rendered and converted to a rectangular frame using equirectangular projection (ERP). The ERP video is sliced vertically and only the FoV is encoded with Kvazaar HEVC encoder in real time and sent over the network in UDP packets. Another laptop is used for playback with a HTC Vive VR headset. Our system can reach an end-to-end latency of 30 ms and bit rate of 20 Mbps for stereo 1080p30 format.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication

Organisations: Pervasive Computing, Datacenter Infrastructure Modules, Nokia Technologies
Contributors: Viitanen, M., Vanne, J., Hämäläinen, T. D., Kulmala, A.
Number of pages: 4
Pages: 1557-1560
Publication date: 19 Jul 2018

Host publication information
Title of host publication: Proceedings - 2018 IEEE 38th International Conference on Distributed Computing Systems, ICDCS 2018
Publisher: IEEE
ISBN (Electronic): 9781538668719
ASJC Scopus subject areas: Software, Hardware and Architecture, Computer Networks and Communications
Keywords: 360 degree video, Edge computing, High Efficiency Video Coding (HEVC), Video coding, Virtual reality (VR)
Electronic versions:

Low Latency Edge Rendering Scheme for Interactive 360 Degree Virtual Reality Gaming
DOIs:

10.1109/ICDCS.2018.00168
URLs:

http://urn.fi/URN:NBN:fi:tty-201908211990

Bibliographical note
jufoid=58061e
Source: Scopus
Source ID: 85050973480
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Effects of blockage in deploying mmWave drone base stations for 5g networks and beyond
Due to their unconstrained mobility and capability to carry goods or equipment, unmanned aerial vehicles (UAVs) or drones are considered as a part of the fifth-generation (5G) wireless networks and become attractive candidates to carry a base station (BS). As 5G requirements apply to a broad range of uses cases, it is of particular importance to satisfy those during spontaneous and temporary events, such as a marathon or a rural fair. To be able to support these scenarios, mobile operators need to deploy significant radio access resources quickly and on demand. Accordingly, by focusing on 5G cellular networks, we investigate the use of drone-assisted communication, where a drone is equipped with a millimeter-wave (mmWave) BS. Being a key technology for 5G, mmWave is able to facilitate the provisioning of the desired per-user data rates as drones arrive at the service area whenever needed. Therefore, in order to maximize the benefits of mmWave-drone-BS utilization, this paper proposes a methodology for its optimized deployment, which delivers the optimal height, coordinates, and coverage radius of the drone-BS by taking into account the human body blockage effects over a mmWave-specific channel model. Moreover, our methodology is able to maximize the number of offloaded users by satisfying the target signal quality at the cell edge and considering the maximum service capacity of the drone-BS. It was observed that the mmWave-specific features are extremely important to consider when targeting efficient drone-BS utilization and thus should be carefully incorporated into analysis.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Carleton University
Contributors: Gapeyenko, M., Bor-Yaliniz, I., Andreev, S., Yanikomeroglu, H., Koucheryavy, Y.
Number of pages: 6
Pages: 1-6
Publication date: 3 Jul 2018

Host publication information
Title of host publication: 2018 IEEE International Conference on Communications Workshops
Publisher: IEEE
ISBN (Electronic): 9781538643280
ASJC Scopus subject areas: Computer Networks and Communications, Computer Science Applications, Hardware and Architecture
Keywords: 5G networks and beyond, Drone-cell communications, Human body blockage, MmWave, Network slicing
Electronic versions:

Effects of blockage in deploying mmWave 2018
DOIs:

10.1109/ICCW.2018.8403671
URLs:

http://urn.fi/URN:NBN:fi:tuni-202002041799

Source: Scopus
Source ID: 85050308378
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Modeling and cancellation of self-interference in full-duplex radio transceivers: Volterra series-based approach

This paper presents a novel digital self-interference canceller for inband full-duplex radio transceivers. The proposed digital canceller utilizes a Volterra series with sparse memory to model the residual SI signal, and it can thereby accurately reconstruct the self-interference even under a heavily nonlinear transmitter power amplifier. To the best of our knowledge, this is the first time such a sparse-memory Volterra series has been used to model the self-interference within an inband full-duplex device. The performance of the Volterra-based canceller is evaluated with real-life measurements that incorporate also an active analog canceller. The results show that the novel digital canceller suppresses the SI by 34 dB in the digital domain, outperforming the state- of-the-art memory polynomial-based solution by a margin of 5 dB. The total amount of cancellation is nearly 110 dB with a transmit power of +30 dBm, even though a shared transmit/receive antenna is used. To the best of our knowledge, this is the highest reported cancellation performance for a shared-antenna full-duplex device with such a high transmit power level.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering
Contributors: Korpi, D., Turunen, M., Anttila, L., Valkama, M.
Number of pages: 6
Pages: 1-6
Publication date: 3 Jul 2018

Host publication information

Title of host publication: 2018 IEEE International Conference on Communications Workshops
Publisher: IEEE
ISBN (Electronic): 9781538643280
ASJC Scopus subject areas: Computer Networks and Communications, Computer Science Applications, Hardware and Architecture
Keywords: Digital cancellation, Full-duplex, Nonlinear power amplifier, Self-interference, Volterra series
Electronic versions:

Modeling and Cancellation of Self-interference 2018
DOIs:

10.1109/ICCW.2018.8403638
URLs:

http://urn.fi/URN:NBN:fi:tuni-202002061903

Bibliographical note

INT=elt,"Turunen, Matias"
Source: Scopus
Source ID: 85050263594
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Optimizing wirelessly powered crowd sensing: Trading energy for data

To overcome the limited coverage in traditional wireless sensor networks, mobile crowd sensing (MCS) has emerged as a new sensing paradigm. To achieve longer battery lives of user devices and incentivize human involvement, this paper presents a novel approach that seamlessly integrates MCS with wireless power transfer, named wirelessly powered crowd sensing (WPCS), for supporting crowd sensing with energy consumption and offering rewards as incentives. An optimization problem is formulated to simultaneously maximize the data utility and minimize the energy consumption for service operator, by jointly controlling wireless-power allocation at the access point (AP) as well as sensing-data size, compression ratio, and sensor transmission duration at the mobile sensor (MS). Given the fixed compression ratios, the optimal power allocation policy is shown to have a threshold-based structure with respect to a defined crowd-sensing priority function for each MS. Given fixed sensing-data utilities, the compression policy achieves the optimal compression ratio. Extensive simulations are also presented to verify the efficiency of the contributed mechanisms.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, University of Hong Kong, Southern University of Science and Technology
Contributors: Li, X., You, C., Andreev, S., Gong, Y., Huang, K.
Number of pages: 6

Pages: 1-6
Publication date: 3 Jul 2018

Host publication information
Title of host publication: 2018 IEEE International Conference on Communications Workshops
Publisher: IEEE
ISBN (Electronic): 9781538643280
ASJC Scopus subject areas: Computer Networks and Communications, Computer Science Applications, Hardware and Architecture
DOIs:

10.1109/ICCW.2018.8403562
Source: Scopus
Source ID: 85050274665
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Cybersecurity Attacks and Defences for Unmanned Smart Ships
By 2020, unmanned ships such as remotely controlled boats and autonomous vessels would become operational, marking a technological revolution for the maritime industry. Such ships are expected to serve needs ranging from coastal ferries to open sea cargo handling. In this paper we detail the security vulnerabilities of such unmanned ships. The attack surface as well as motivations for attack attempts also are discussed to provide a perspective of how and why attacks are undertaken. Finally defence strategies are proposed as countermeasures.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research area: Information security, Computing Sciences, Ericsson, F-Secure
Contributors: Silverajan, B., Ocak, M., Nagel, B.
Number of pages: 6
Pages: 15-20
Publication date: 1 Jul 2018

Host publication information
Title of host publication: Proceedings - IEEE 2018 International Congress on Cybermatics : 2018 IEEE Conferences on Internet of Things, Green Computing and Communications, Cyber, Physical and Social Computing, Smart Data, Blockchain, Computer and Information Technology, iThings/GreenCom/CPSCom/SmartData/Blockchain/CIT 2018
Publisher: IEEE
ISBN (Electronic): 9781538679753
ASJC Scopus subject areas: Business, Management and Accounting (miscellaneous), Artificial Intelligence, Computer Networks and Communications, Computer Science Applications, Hardware and Architecture, Information Systems and Management, Health Informatics, Communication
Keywords: Autonomous vehicles, IoT, Security, Smart Ships
DOIs:

10.1109/Cybermatics_2018.2018.00037
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Secure Firmware Updates for IoT: A Survey
The evolution of the Internet to an ubiquitous computing environment where massive amounts of devices will be connected. Sharing, receiving and acting upon data has brought in a problem of security. There are as many firmware and software update procedures as there are manufacturers. Therefore it would be good if a common solution could be found. We looked for suitable mechanisms in the past three years, to be used in Internet of Things networks as well as an up and coming research and standardization work. Our findings show that there indeed are good options for firmware update mechanisms that use state-of-The-Art technologies to deliver updates in a secure manner. While not all the mechanisms were specifically targeting deployment scenarios found in the Internet of Things, we still believe the concept of such update mechanism is suitable also for IoT use and thus can be adapted trivially to IoT networks and devices. We also propose a generic four-element model for secure firmware updates.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research area: Information security, Computing Sciences
Contributors: Kolehmainen, A.
Number of pages: 6
Pages: 112-117
Publication date: 1 Jul 2018

Host publication information

Title of host publication: Proceedings - IEEE 2018 International Congress on Cybermatics : 2018 IEEE Conferences on Internet of Things, Green Computing and Communications, Cyber, Physical and Social Computing, Smart Data, Blockchain, Computer and Information Technology, iThings/GreenCom/CPSCom/SmartData/Blockchain/CIT 2018
Publisher: IEEE
ISBN (Electronic): 9781538679753
ASJC Scopus subject areas: Business, Management and Accounting (miscellaneous), Artificial Intelligence, Computer Networks and Communications, Computer Science Applications, Hardware and Architecture, Information Systems and Management, Health Informatics, Communication
Keywords: Firmware updates, IoT, Lifecycle Management
DOIs:

10.1109/Cybermatics_2018.2018.00051
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Adjusting university education with workspace training and self-education

Close to 100% employment of students and easy access to abundance of information on Internet has essentially changed student's learning practices and their earlier knowledge background, especially on rapidly progressing field of Software Engineering. On workplace they have to use technologies, which are used in practice of their employing enterprise, but often do not understand the scientific and/or technological principles on which these technologies are based. They seek explanations on Internet, but information on Internet is often low quality, one-sided and presented with business targets on mind - to get more users to technologies developed and sold by a business enterprise. Thus university has to explain basic principles of technologies what students already know and have used and correct some popular beliefs, which are supported by software vendors and based their business interests. Non-formal sources of knowledge - workplace training and Internet - do not reduce teacher's task, but force teachers constantly study all new which appears in this field, thus increase teachers workload. Students increasing use of non-formal sources of knowledge imply need for flipping the process - instead of teaching students are set to learn from provided detailed tutorials. Use of Internet and work has made self-study, seeking information from Internet sources very customary for current students, thus such flipping worked very well in a game programming course provided by the first author.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Research group: Software Engineering and Intelligent Systems, Tallinn University of Technology, University of Lapland
Contributors: Henno, J., Jaakkola, H., Makela, J.
Number of pages: 8
Pages: 701-708
Publication date: 28 Jun 2018

Host publication information

Title of host publication: 2018 41st International Convention on Information and Communication Technology, Electronics and Microelectronics, MIPRO 2018
Publisher: IEEE
ISBN (Electronic): 9789532330977
ASJC Scopus subject areas: Electrical and Electronic Engineering, Hardware and Architecture, Signal Processing, Computer Networks and Communications
Keywords: CSS, game programming, HTML5, Internet, IT, JavaScript, SE, university education, working students
DOIs:

10.23919/MIPRO.2018.8400131
Source: Scopus
Source ID: 85050228879
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Role of the user in information systems development

We have focused our paper on the aspects important in adapting an Information System (IS) to the user's cultural background. We are interested both in the factors related to IS development and in the use of IS. Increasingly, ISs are being developed and used in a global context. We have perceived differences in expectations of functionalities, architecture, structural properties, information search practices, web-based system properties, and user interfaces. One conclusion would be that a high quality IS reflects user behavior in its use context. In that case, the system has to model its user one way or another. Until now, the topic has been handled without meaningful effort to model user behavior. Current publications cover a wide variety of rules on how to take into account cultural differences in the IS context. In this paper, our aim is to study the current state-of-the-art of user modeling - modeling the human being as an IS user. We start with general aspects related to the role of the user in IS development and alternatives to adaptable systems. The findings are applicable in the educational context as well. More and more, the use of computers and ISs is becoming an essential part of studies: the use of MOOCs (Massively Open Online Courses) as a part or replacement for traditional face-to-face

classes; flipped learning methodology emphasizing the significance of self-learning; and blended learning, including quite often computerized study content. Our focus is on the global context, in which students represent different cultures and the IS is globally available.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Research group: Software Engineering and Intelligent Systems, Computer Science Institute, Tallinn University of Technology, University of Lapland
Contributors: Jaakkola, H., Thalheim, B., Henno, J., Mäkelä, J., Keto, H.
Number of pages: 8
Pages: 625-632
Publication date: 28 Jun 2018

Host publication information

Title of host publication: 2018 41st International Convention on Information and Communication Technology, Electronics and Microelectronics, MIPRO 2018
Publisher: IEEE
ISBN (Electronic): 9789532330977
ASJC Scopus subject areas: Electrical and Electronic Engineering, Hardware and Architecture, Signal Processing, Computer Networks and Communications
Keywords: adaption, context, human behavior modeling, information system, information systems development, requirements engineering, user, user adaptable, user modeling
Electronic versions:

2018-Mipro-hj-P4699
DOIs:

10.23919/MIPRO.2018.8400118
URLs:

http://urn.fi/URN:NBN:fi:tty-201901161102
Source: Scopus
Source ID: 85050202384
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

An approach for implementing key performance indicators of a discrete manufacturing simulator based on the ISO 22400 standard

Performance measurement tools and techniques have become very significant in today's industries for increasing the efficiency of their processes in order to face the competitive market. The first step towards performance measurement is the real-time monitoring and gathering of the data from the manufacturing system. Applying these performance measurement techniques on real-world industry in a way that is more general and efficient is the next challenge. This paper presents a methodology for implementing the key performance indicators defined in the ISO 22400 standard-Automation systems and integration, Key performance indicators (KPIs) for manufacturing operations management. The proposed methodology is implemented on a multi robot line simulator for measuring its performance at runtime. The approach implements a knowledge-based system within an ontology model which describes the environment, the system and the KPIs. In fact, the KPIs semantic descriptions are based on the data models presented in the Key Performance Indicators Markup Language (KPIML), which is an XML implementation of models developed by the Manufacturing Enterprise Solutions Association (MESA) international organization.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Automation and Hydraulic Engineering, Research group: Automation and Systems Theory
Contributors: Muhammad, U., Ferrer, B. R., Mohammed, W. M., Lastra, J. L.
Number of pages: 8
Pages: 629-636
Publication date: 15 Jun 2018

Host publication information

Title of host publication: 2018 IEEE Industrial Cyber-Physical Systems, ICPS 2018
Publisher: IEEE
ISBN (Electronic): 9781538665312
ASJC Scopus subject areas: Artificial Intelligence, Hardware and Architecture, Control and Optimization, Industrial and Manufacturing Engineering
Keywords: ISO 22400 standard, Key performance indicators, Knowledge-based system, Manufacturing systems, Ontology
DOIs:

10.1109/ICPHYS.2018.8390779

Bibliographical note
EXT="Muhammad, Usman"
Source: Scopus
Source ID: 85050127723
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Towards the deployment of cloud robotics at factory shop floors: A prototype for smart material handling
The evolution of industries and their needs towards the implementation of Industry 4.0 based systems has brought both new technological challenges and opportunities. This article proposes the adoption and deployment of cloud robotics at factories to enhance the control and monitoring of processes, such as handling materials multiple assemblies in single cells. The ultimate research objective of this research is the offloading computation and integrating cloud robotics into an industrial scenario. However, the investigation of state of the art techniques, tools and technologies, and the development of functional prototypes is beforehand required. Then, this article presents a small-scale system as a prototype that employs the Google cloud vision API as a resource that, in turn, is used by networked agents for supporting the decision-making in the process of handling material commodities at factory shop floor. The overall concept as well as the interaction between the main actors of the prototype is detailed. Finally, further research directions are discussed.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Automation and Hydraulic Engineering, Research group: Automation and Systems Theory
Contributors: Hussnain, A., Ferrer, B. R., Lastra, J. L.
Number of pages: 7
Pages: 44-50
Publication date: 15 Jun 2018

Host publication information
Title of host publication: 2018 IEEE Industrial Cyber-Physical Systems, ICPS 2018
Publisher: IEEE
ISBN (Electronic): 9781538665312
ASJC Scopus subject areas: Artificial Intelligence, Hardware and Architecture, Control and Optimization, Industrial and Manufacturing Engineering
Keywords: Cloud Robotics, Industrial Cyber-Physical Systems, Industry 4.0, Multi-Agent Systems, SOA
DOIs:
10.1109/ICPHYS.2018.8387635

Bibliographical note
INT=aut,"Hussnain, Ali"
Source: Scopus
Source ID: 85050146182
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Toward efficient many-core scheduling of partial expansion graphs
Transformation of synchronous data flow graphs (SDF) into equivalent homogeneous SDF representations has been extensively applied as a pre-processing stage when mapping signal processing algorithms onto parallel platforms. While this transformation helps fully expose task and data parallelism, it also presents several limitations such as an exponential increase in the number of actors and excessive communication overhead. Partial expansion graphs were introduced to address these limitations for multi-core platforms. However, existing solutions are not well-suited to achieve efficient scheduling on many-core architectures. In this article, we develop a new approach that employs cyclo-static data flow techniques to provide a simple but efficient method of coordinating the data production and consumption in the expanded graphs. We demonstrate the advantage of our approach through experiments on real application models.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Research area: Computer engineering, Parc Scientifique de la Haute Borne, University of Maryland
Contributors: Tran, H. N., Bhattacharyya, S. S., Talpin, J. P., Gautier, T.
Number of pages: 4
Pages: 100-103
Publication date: 28 May 2018

Host publication information
Title of host publication: Proceedings of the 21st International Workshop on Software and Compilers for Embedded Systems, SCOPES 2018

Publisher: Association for Computing Machinery, Inc
ISBN (Print): 9781450357807
ASJC Scopus subject areas: Hardware and Architecture, Software
DOIs:
10.1145/3207719.3207734
Source: Scopus
Source ID: 85054140820
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Analysis of differentially modulated cooperative communications over asymmetric fading channels

Differential modulation has largely re-attracted the attention of academia and industry due to its advantages relating to simple implementation and no need for knowledge of channel state information. The present work analyzes the average bit error rate performance of dual-hop cooperative systems over generalized multipath fading conditions. The considered system is differentially modulated and is assumed to operate based on the amplify-and-forward relaying protocol. Therefore, the main advantage of the considered set up is that it does not require any channel state information neither at the relay nor at the destination nodes. Novel closed-form expressions are derived for the end-to-end error rate under asymmetric generalized multipath fading conditions, which are encountered in realistic wireless communication scenarios. These expressions are subsequently employed in quantifying the effect of generalized fading conditions on the achieved bit error rate performance. It is shown that the impact of multipath fading and shadowing effects is detrimental at both high and low signal-to-noise ratio regimes as the corresponding deviations are often close to an order of magnitude. The incurred difference is also significantly different than the conventional Rayleigh fading conditions, which verifies that accurate channel characterization is of paramount importance in the effective design of conventional and emerging wireless technologies. In addition, it indicates that differential modulation can be a suitable modulation scheme for relay systems, under certain conditions, since it can provide adequate performance at a reduced implementation complexity.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research group: Wireless Communications and Positioning, Electronics and Communications Engineering , Mohammed Bin Rashid Space Centre (MBRSC), Department of Electrical and Computer Engineering, Khalifa University , Aristotle University of Thessaloniki
Contributors: Almaeeni, S., Sofotasios, P. C., Muhaidat, S., Karagiannidis, G. K.
Number of pages: 8
Pages: 1-8
Publication date: 16 May 2018

Host publication information

Title of host publication: Proceedings - 2018 International Conference on Advanced Communication Technologies and Networking, CommNet 2018
Publisher: IEEE
ISBN (Electronic): 9781538646090
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Control and Optimization
DOIs:
10.1109/COMMNET.2018.8360284
Source: Scopus
Source ID: 85048312791
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Capacity analysis under generalized composite fading conditions

Novel composite fading models were recently proposed based on inverse gamma distributed shadowing conditions. These models were extensively shown to provide remarkable modeling of the simultaneous occurrence of multipath fading and shadowing phenomena in emerging wireless scenarios such as cellular, off-body and vehicle-to-vehicle communications. Furthermore, the algebraic representation of these models is rather tractable, which renders them convenient to handle both analytically and numerically. The present contribution presents the major theoretical and practical characteristics of the η - μ / inverse gamma composite fading model, followed by a thorough ergodic capacity analysis. To this end, novel analytic expressions are derived, which are subsequently used in the evaluation of the corresponding system performance. In this context, the offered results are compared with respective results from cases assuming conventional fading conditions, which leads to the development of numerous insights on the effect of the multipath fading and shadowing severity on the achieved capacity levels. It is expected that these results will be useful in the design of timely and highly demanding wireless technologies, such as wearable, cellular and inter-vehicular communications as well in wireless power transfer based applications in the context of the Internet of Things.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research group: Wireless Communications and Positioning, Electronics and Communications Engineering , Department of Electrical and Computer Engineering, Khalifa University, Queen's University, Belfast, Northern Ireland, Aristotle University of Thessaloniki
Contributors: Sofotasios, P. C., Yoo, S. K., Bhargav, N., Muhaidat, S., Cotton, S. L., Matthaiou, M., Valkama, M., Karagiannidis, G. K.
Number of pages: 10
Pages: 1-10
Publication date: 16 May 2018

Host publication information
Title of host publication: Proceedings - 2018 International Conference on Advanced Communication Technologies and Networking, CommNet 2018
Publisher: IEEE
ISBN (Electronic): 9781538646090
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Control and Optimization
DOIs:

10.1109/COMMNET.2018.8360282
Source: Scopus
Source ID: 85048321386
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Maximum achievable throughput and interference mitigation for SUN in coexistence with WLAN
An optimum packet length selection scheme to maximize the throughput of a smart utility network (SUN) is introduced under wireless local area network (WLAN) interference system. The traditional and the investigated segmented packet collision models (PCM) are compared in terms of packet error rate (PER) and maximum achievable throughput. Furthermore, we quantify the impact of minimum mean square error (MMSE) interference mitigation for the SUN in the coexistence of WLAN interfering packets over multipath Rayleigh fading channel. The effect of the distance between the WLAN transmitter and the SUN receiver on the probability of error is also investigated.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing, Qatar University, Electrical Engineering Department, University of Texas at Dallas
Contributors: Mohamed, S., Hamila, R., Al-Dhahir, N., Gouissem, A., Benbrahim, L., Gabbouj, M.
Number of pages: 6
Pages: 1-6
Publication date: 16 May 2018

Host publication information
Title of host publication: Proceedings - 2018 International Conference on Advanced Communication Technologies and Networking, CommNet 2018
Publisher: IEEE
ISBN (Electronic): 9781538646090
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Control and Optimization
Keywords: Interference mitigation, Minimum mean square error, Packet collision model, Packet length, Smart grid, Smart utility network, Throughput
DOIs:

10.1109/COMMNET.2018.8360252

Bibliographical note
EXT="Hamila, Ridha"
Source: Scopus
Source ID: 85048343760
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Outage probability of multi-carrier NOMA systems under joint I/Q imbalance
Non-orthogonal multiple access (NOMA) has been recently proposed as a viable technology that can potentially improve the spectral efficiency of fifth generation (5G) wireless networks and beyond. However, in practical communication scenarios, transceiver architectures inevitably suffer from radio-frequency (RF) front-end related impairments that can lead to degradation of the overall system performance, with in-phase/quadrature-phase imbalance (IQI) constituting a major impairment in direct-conversion transceivers. In the present work, we quantify the effects of joint transmitter/receiver IQI

on the performance of NOMA based multi-carrier (MC) systems under multipath fading conditions. Furthermore, we derive the asymptotic diversity order of the considered MC NOMA set up. Capitalizing on these results, we demonstrate that the effects of IQI differ considerably among NOMA users and depend on the underlying system parameters. For example, it is shown that the first sorted user appears more robust to IQI, which indicates that higher order users are more sensitive to the considered non-negligible impairment.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research group: Wireless Communications and Positioning, Electronics and Communications Engineering , Khalifa University, Department of Electrical and Computer Engineering, Aristotle University of Thessaloniki, University of Texas at Dallas
Contributors: Selim, B., Muhaidat, S., Sofotasios, P. C., Sharif, B. S., Stouraitis, T., Karagiannidis, G. K., Al-Dhahir, N.
Number of pages: 7
Pages: 1-7
Publication date: 16 May 2018

Host publication information
Title of host publication: Proceedings - 2018 International Conference on Advanced Communication Technologies and Networking, CommNet 2018
Publisher: IEEE
ISBN (Electronic): 9781538646090
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Control and Optimization
DOIs:

10.1109/COMMNET.2018.8360283
Source: Scopus
Source ID: 85048327091
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Preface: Special Issue on ‘New Hydraulic Components for Tough Robots’

General information
Publication status: Published
MoE publication type: B1 Article in a scientific magazine
Organisations: Automation and Hydraulic Engineering, Research group: Innovative Hydraulic Automation, Tokyo Institute of Technology, Ritsumeikan University, Italian Institute of Technology, Okayama University
Contributors: Suzumori, K., Hyon, S. H., Semini, C., Mattila, J., Kanda, T.
Number of pages: 1
Publication date: 3 May 2018
Peer-reviewed: No

Publication information
Journal: Advanced Robotics
Volume: 32
Issue number: 9
ISSN (Print): 0169-1864
Ratings:

Scopus rating (2018): CiteScore 2.7 SJR 0.346 SNIP 0.886
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Software, Human-Computer Interaction, Hardware and Architecture, Computer Science Applications
DOIs:

10.1080/01691864.2018.1466427
Source: Scopus
Source ID: 85047515551
Research output: Contribution to journal › Editorial › Scientific

A design tool for high performance image processing on multicore platforms
Design and implementation of smart vision systems often involve the mapping of complex image processing algorithms into efficient, real-time implementations on multicore platforms. In this paper, we describe a novel design tool that is developed to address this important challenge. A key component of the tool is a new approach to hierarchical dataflow scheduling that integrates a global scheduler and multiple local schedulers. The local schedulers are lightweight modules that work independently. The global scheduler interacts with the local schedulers to optimize overall memory usage and execution time. The proposed design tool is demonstrated through a case study involving an image stitching application

for large scale microscopy images.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, University of Maryland, National Institute of Standards and Technology
Contributors: Wu, J., Blattner, T., Keyrouz, W., Bhattacharyya, S. S.
Number of pages: 6
Pages: 1304-1309
Publication date: 19 Apr 2018

Host publication information
Title of host publication: Proceedings of the 2018 Design, Automation and Test in Europe Conference and Exhibition, DATE 2018
Publisher: IEEE
ISBN (Electronic): 9783981926316
ASJC Scopus subject areas: Safety, Risk, Reliability and Quality, Hardware and Architecture, Software, Information Systems and Management
DOIs:
10.23919/DATE.2018.8342215
Source: Scopus
Source ID: 85048740891
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Memory-Constrained vectorization and scheduling of dataflow graphs for hybrid CPU-GPU platforms
The increasing use of heterogeneous embedded systems with multi-core CPUs and Graphics Processing Units (GPUs) presents important challenges in effectively exploiting pipeline, task, and data-level parallelism to meet throughput requirements of digital signal processing applications. Moreover, in the presence of system-level memory constraints, hand optimization of code to satisfy these requirements is inefficient and error prone and can therefore, greatly slow down development time or result in highly underutilized processing resources. In this article, we present vectorization and scheduling methods to effectively exploit multiple forms of parallelism for throughput optimization on hybrid CPU-GPU platforms, while conforming to system-level memory constraints. The methods operate on synchronous dataflow representations, which are widely used in the design of embedded systems for signal and information processing. We show that our novel methods can significantly improve system throughput compared to previous vectorization and scheduling approaches under the same memory constraints. In addition, we present a practical case-study of applying our methods to significantly improve the throughput of an orthogonal frequency division multiplexing receiver system for wireless communications.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Pervasive Computing, University of Maryland, Department of Electrical and Computer Engineering
Contributors: Lin, S., Wu, J., Bhattacharyya, S. S.
Publication date: 1 Feb 2018
Peer-reviewed: Yes

Publication information
Journal: ACM Transactions on Embedded Computing Systems
Volume: 17
Issue number: 2
Article number: 50
ISSN (Print): 1539-9087
Ratings:
Scopus rating (2018): CiteScore 3 SJR 0.326 SNIP 0.979
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture
Keywords: Dataflow models, Design optimization, Heterogeneous computing, Signal processing systems, Software synthesis
DOIs:
10.1145/3157669
Source: Scopus
Source ID: 85042527088
Research output: Contribution to journal › Article › Scientific › peer-review

Analyzing Effects of Directional Deafness on mmWave Channel Access in Unlicensed Bands

Directional deafness problem is one of the most important challenges in beamforming-based channel access at mmWave frequencies, which is believed to have detrimental effects on system performance in form of excessive delays and significant packet drops. In this paper, we contribute a quantitative analysis of deafness in directional random access systems operating in unlicensed bands by relying on stochastic geometry formulations. We derive a general numerical approach that captures the behavior of deafness probability as well as provide a closed-form solution for a typical sector-shaped antenna model, which is then may be extended to a more realistic two-sector pattern. Finally, employing contemporary IEEE 802.11ad modeling numerology, we illustrate our analysis revealing the importance of deafness-related considerations and their system- level impact.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Intel Corporation
Contributors: Galinina, O., Pyattaev, A., Johnsson, K., Andreev, S., Koucheryavy, Y.
Number of pages: 7
Pages: 1-7
Publication date: 24 Jan 2018

Host publication information

Title of host publication: 2017 IEEE Globecom Workshops, GC Wkshps 2017 - Proceedings
Publisher: IEEE
ISBN (Electronic): 9781538639207
ASJC Scopus subject areas: Computer Networks and Communications, Computer Science Applications, Hardware and Architecture, Safety, Risk, Reliability and Quality
Electronic versions:

Analyzing Effects of Directional Deafness 2017
DOIs:

10.1109/GLOCOMW.2017.8269183
URLs:

http://urn.fi/URN:NBN:fi:tuni-202002252341
Source: Scopus
Source ID: 85050472068
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Detailed Interference Analysis in Dense mmWave Systems Employing Dual-Polarized Antennas

The use of extremely high frequency (EHF) bands, known as millimeter-wave (mmWave) frequencies, requires densification of cells to maintain system performance at required levels. This may lead to potential increase of interference in practical mmWave networks, thus making it the limiting factor. On the other hand, attractive utilization of dual-polarized antennas may improve over this situation by mitigating some of the interfering components, which can be employed as part of interference control techniques. In this paper, an accurate two-stage ray-based characterization is conducted that models interference-related metrics while taking into account a detailed dual- polarized antenna model. In particular, we confirm that narrower pencil-beam antennas (HPBW = 13) have significant advantages as compared to antennas with relatively narrow beams (HPBW = 20 and HPBW = 50) in the environments with high levels of interference. Additionally, we demonstrate that in the Manhattan grid deployment a transition from interference- to noise-limited regime and back occurs at the cell inter-site distances of under 90 m and over 180 m, respectively.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Intel Corporation
Contributors: Solomitckii, D., Petrov, V., Nikopour, H., Akdeniz, M., Orhan, O., Himayat, N., Talwar, S., Andreev, S., Koucheryavy, Y.
Number of pages: 6
Pages: 1-6
Publication date: 24 Jan 2018

Host publication information

Title of host publication: 2017 IEEE Globecom Workshops
Publisher: IEEE
ISBN (Electronic): 9781538639207
ASJC Scopus subject areas: Computer Networks and Communications, Computer Science Applications, Hardware and Architecture, Safety, Risk, Reliability and Quality
Electronic versions:

Detailed Interference Analysis in Dense mmWave 2018

DOIs:
10.1109/GLOCOMW.2017.8269040
URLs:
http://urn.fi/URN:NBN:fi:tuni-202002041814
Source: Scopus
Source ID: 85050464132
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Modeling Three-Dimensional Interference and SIR in Highly Directional mmWave Communications

Recently, new opportunities for utilizing extremely high frequencies have become instrumental in developing fifth-generation(5G) mobile technology. The use of highly directional antennas in millimeter-wave (mmWave) bands poses an important question of whether two- dimensional modeling suffices to capture the resulting system performance. Accounting for the effects of human body blockage by mmWave transmissions, in this work we compare the performance of the conventional two-dimensional and the proposed three- dimensional modeling. With our stochastic geometry based approach, we consider the aggregate interference and signal-to- interference ratio (SIR) to be the main metrics of interest. Both counterpart models attempt to capture the inherent behavior of 5G mmWave systems by incorporating the effects of human body blockage and antenna directivity. We thus deliver a realistic numerical assessment by comparing the three-dimensional modeling with its two-dimensional projection to reveal the resulting discrepancy.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Peoples' Friendship University of Russia, Federal Research Center Computer Science and Control of the Russian Academy of Sciences
Contributors: Kovalchukov, R., Samuylov, A., Moltchanov, D., Ometov, A., Andreev, S., Koucheryavy, Y., Samouylov, K.
Number of pages: 7
Pages: 1-7
Publication date: 10 Jan 2018

Host publication information

Title of host publication: 2017 IEEE Global Communications Conference, GLOBECOM 2017
Publisher: IEEE
ISBN (Electronic): 9781509050192
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Safety, Risk, Reliability and Quality
Electronic versions:
Modeling Three-Dimensional Interference and SIR in Highly Directional mmWave Communications 2017
DOIs:
10.1109/GLOCOM.2017.8254905
URLs:
http://urn.fi/URN:NBN:fi:tuni-202001281599
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Advanced wireless m-bus platform for intensive field testing in industry 4.0-based systems

Current forecasts predict that the Industrial Internet of Things (IIoT) will comprise about 10 billion devices by 2020. Because of its unique and novel demands, the emerging concepts of Industry 4.0 and SmartGrid networks have recently been coined and are now well established in the technical speech. In this work, we propose a newly developed multi-platform software tool aimed at testing the capabilities of Wireless MBus (WM-Bus) networks via simulating sensor-like behavior in uni-directional communication with a remote data concentrator. Building on our developed machine-type communication gateway (MTCG) able to receive WM-Bus data, we extend the set of features and introduce new machine-type communication device (MTCD) capable of emulating the corresponding data transmissions. As utility companies lack these features, our software implementation and hardware design open the door to initial verification of WM-Bus-based data transmissions for them without the need for investing into expensive development and certification of smart meters, where WM-Bus is utilized for data transmissions.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Brno University of Technology, Telekom Austria Group
Contributors: Masek, P., Hudec, D., Krejci, J., Ometov, A., Hosek, J., Andreev, S., Kröpfl, F., Koucheryavy, Y.
Number of pages: 6
Pages: 150-155
Publication date: 2018

Host publication information
Title of host publication: 24th European Wireless Conference
Publisher: VDE Verlag
ISBN (Electronic): 9783800745609
ASJC Scopus subject areas: Hardware and Architecture, Computer Networks and Communications
Source: Scopus
Source ID: 85050011538
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Exposed Datapath optimizations for Loop Scheduling
Transport Triggered Architecture (TTA) processors allow unique low level compiler optimizations such as software bypassing and operand sharing. Previously, these optimizations have mostly been performed inside single basic blocks, leaving much of their potential unused. In this work, software bypassing and operand sharing are integrated with loop scheduling, allowing optimizations over loop iteration boundaries. This considerably further reduces register file accesses and immediate value transfers on tight loops – in some cases even eliminating all register file accesses from the loop body. In the benchmarked 12 small loops, compared to traditional VLIW-style processors, on average 63% of register file reads and 77% of register file writes could be eliminated. Compared to a compiler which performs these optimizations only inside a basic block, on average 58% of register file reads, 28% of register file writes could be eliminated. The additional register access reductions allow both direct energy savings from fewer register accesses and indirect energy savings by allowing the use of simpler register files with less read and write ports and a simpler interconnect network with less transport buses.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Research area: Computer engineering
Contributors: Kultala, H., Jääskeläinen, P., IJzerman, J., Lehtonen, L., Viitanen, T., Mäkitalo, M., Takala, J.
Number of pages: 8
Pages: 171-178
Publication date: 2018

Host publication information
Title of host publication: Embedded Computer Systems: Architectures, Modeling, and Simulation 2017 IEEE International Conference (IC-SAMOS 2017)
Publisher: IEEE
ISBN (Electronic): 978-1-5386-3437-0
ASJC Scopus subject areas: Hardware and Architecture
Electronic versions:

LoopOptimizationsForTTA
DOIs:

10.1109/SAMOS.2017.8344625
URLs:

http://urn.fi/URN:NBN:fi:tty-201803191384
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Federated IoT services leveraging 5G technologies at the edge
The Internet of Things (IoT) ecosystem is evolving towards the deployment of integrated environments, wherein heterogeneous devices pool their capacities together to match wide-ranging user and service requirements. As a consequence, solutions for efficient and synergistic cooperation among objects acquire great relevance. Along this line, this paper focuses on the adoption of the promising MIFaaS (Mobile-IoT-Federation-as-a-Service) paradigm to support delay-sensitive applications for high-end IoT devices in next-to-come fifth generation (5G) environments. MIFaaS fosters the provisioning of IoT services and applications with low-latency requirements by leveraging cooperation among private/public clouds of IoT objects at the edge of the network. A performance assessment of the MIFaaS paradigm in a cellular 5G environment based on both Long Term Evolution (LTE) and the recent Narrowband IoT (NB-IoT) is presented. Obtained results demonstrate that the proposed solution outperforms classic approaches, highlighting significant benefits derived from the joint use of LTE and NB-IoT bandwidths in terms of increased number of successfully delivered IoT services.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Electronics and Communications Engineering, Universita degli Studi di Reggio Calabria, Peoples' Friendship University of Russia
Contributors: Farris, I., Orsino, A., Militano, L., Iera, A., Araniti, G.

Pages: 58-69
Publication date: 2018
Peer-reviewed: Yes

Publication information
Journal: Ad Hoc Networks
Volume: 68
ISSN (Print): 1570-8705
Ratings:

Scopus rating (2018): CiteScore 7.7 SJR 0.648 SNIP 2.03
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture, Computer Networks and Communications
Keywords: 5G, IoT, Multi-access edge computing, Narrowband-IoT
DOIs:

10.1016/j.adhoc.2017.09.002

Bibliographical note
INT=ELT, "Orsino, A."
Source: Scopus
Source ID: 85030565702
Research output: Contribution to journal › Article › Scientific › peer-review

Model-Based Dynamic Scheduling for Multicore Signal Processing

This paper presents a model-based design method and a corresponding new software tool, the HTGS Model-Based Engine (HMBE), for designing and implementing dataflow-based signal processing applications on multi-core architectures. HMBE provides complementary capabilities to HTGS (Hybrid Task Graph Scheduler), a recently-introduced software tool for implementing scalable workflows for high performance computing applications on compute nodes with high core counts and multiple GPUs. HMBE integrates model-based design approaches, founded on dataflow principles, with advanced design optimization techniques provided in HTGS. This integration contributes to (a) making the application of HTGS more systematic and less time consuming, (b) incorporating additional dataflow-based optimization capabilities with HTGS optimizations, and (c) automating significant parts of the HTGS-based design process using a principled approach. In this paper, we present HMBE with an emphasis on the model-based design approaches and the novel dynamic scheduling techniques that are developed as part of the tool. We demonstrate the utility of HMBE via two case studies: an image stitching application for large microscopy images and a background subtraction application for multispectral video streams.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Pervasive Computing, Research area: Computer engineering, University of Maryland, National Institute of Standards and Technology
Contributors: Wu, J., Blattner, T., Keyrouz, W., Bhattacharyya, S. S.
Number of pages: 14
Pages: 1-14
Publication date: 2018
Peer-reviewed: Yes
Early online date: 2018

Publication information
Journal: Journal of Signal Processing Systems
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2018): CiteScore 1.7 SJR 0.203 SNIP 0.61
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Dataflow, Memory management, Multicore platforms, Scheduling
DOIs:

10.1007/s11265-018-1412-5
Source: Scopus
Source ID: 85054798661
Research output: Contribution to journal › Article › Scientific › peer-review

Outlier edge detection using random graph generation models and applications

Outliers are samples that are generated by different mechanisms from other normal data samples. Graphs, in particular social network graphs, may contain nodes and edges that are made by scammers, malicious programs or mistakenly by normal users. Detecting outlier nodes and edges is important for data mining and graph analytics. However, previous research in the field has merely focused on detecting outlier nodes. In this article, we study the properties of edges and propose effective outlier edge detection algorithm. The proposed algorithms are inspired by community structures that are very common in social networks. We found that the graph structure around an edge holds critical information for determining the authenticity of the edge. We evaluated the proposed algorithms by injecting outlier edges into some real-world graph data. Experiment results show that the proposed algorithms can effectively detect outlier edges. In particular, the algorithm based on the Preferential Attachment Random Graph Generation model consistently gives good performance regardless of the test graph data. More important, by analyzing the authenticity of the edges in a graph, we are able to reveal underlying structure and properties of a graph. Thus, the proposed algorithms are not limited in the area of outlier edge detection. We demonstrate three different applications that benefit from the proposed algorithms: (1) a preprocessing tool that improves the performance of graph clustering algorithms; (2) an outlier node detection algorithm; and (3) a novel noisy data clustering algorithm. These applications show the great potential of the proposed outlier edge detection techniques. They also address the importance of analyzing the edges in graph mining—a topic that has been mostly neglected by researchers.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing, Research group: Video, Research group: Multimedia Research Group - MRG, Qatar University
Contributors: Zhang, H., Kiranyaz, S., Gabbouj, M.
Publication date: 1 Dec 2017
Peer-reviewed: Yes

Publication information

Journal: Journal of Big Data
Volume: 4
Issue number: 1
Article number: 11
ISSN (Print): 2196-1115
Ratings:

Scopus rating (2017): CiteScore 7.3 SJR 1.143 SNIP 4.649
Original language: English
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems, Information Systems and Management
Keywords: Graph mining, Outlier detection, Outlier edge
Electronic versions:

Outlier edge detection using random graph generation models and applications
DOIs:

10.1186/s40537-017-0073-8
URLs:

http://urn.fi/URN:NBN:fi:tty-201706051584

Bibliographical note

EXT="Kiranyaz, Serkan"
Source: Scopus
Source ID: 85018865430
Research output: Contribution to journal › Article › Scientific › peer-review

Model-based dynamic scheduling for multicore implementation of image processing systems

In this paper, we present a new software tool, called HTGS Model-based Engine (HMBE), for the design and implementation of multicore signal processing applications. HMBE provides complementary capabilities to HTGS (Hybrid Task Graph Scheduler), which is a recently-introduced software tool for implementing scalable workflows for high performance computing applications. HMBE integrates advanced design optimization techniques provided in HTGS with model-based approaches that are founded on dataflow principles. Such integration contributes to (a) making the application of HTGS more systematic and less time consuming, (b) incorporating additional dataflow-based optimization capabilities with HTGS optimizations, and (c) automating significant parts of the HTGS-based design process. In this paper, we present HMBE with an emphasis on novel dynamic scheduling techniques that are developed as part of the tool. We demonstrate the utility of HMBE through a case study involving an image stitching application for large scale microscopy images.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, University of Maryland, National Institute of Standards and Technology
Contributors: Wu, J., Blattner, T., Keyrouz, W., Bhattacharyya, S. S.
Publication date: 14 Nov 2017

Host publication information

Title of host publication: 2017 IEEE International Workshop on Signal Processing Systems, SiPS 2017
Publisher: IEEE
Article number: 8110003
ISBN (Electronic): 9781538604465
ASJC Scopus subject areas: Electrical and Electronic Engineering, Signal Processing, Applied Mathematics, Hardware and Architecture
DOIs:

10.1109/SiPS.2017.8110003
Source: Scopus
Source ID: 85040564128
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Evaluation of a Heterogeneous Multicore Architecture by Design and Test of an OFDM Receiver

This paper presents an evaluation of a Heterogeneous Multicore Architecture (HMA) by implementing Orthogonal Frequency- Division Multiplexing (OFDM) receiver blocks as designs for the test of functionality. OFDM receiver consists of computationally intensive and general-purpose processing tasks that can provide maximum coverage to test and evaluate a massively-parallel as well as a general-purpose platform like the HMA. The blocks of the receiver are primarily designed by crafting template-based Coarse-Grained Reconfigurable Array (CGRA) devices and then arranging them in a sequence over a Network-on-Chip (NoC) structure along with a few RISC cores for complete OFDM processing. The OFDM blocks such as Fast Fourier Transform (FFT) and Time Synchronization are computationally intensive and require parallel processing. The OFDM receiver also contains tasks such as frequency offset estimation which require the processing of Taylor series and CORDIC algorithms that are serial in nature. Such a combination of serial and parallel algorithms can perform a thorough exploration and evaluation of almost all the design features of an HMA. The OFDM implementation has led to scale CGRAs to different dimensions, instantiate Processing Elements (PEs) as multiple arithmetic resources and to establish almost all possible ways of PE interconnections. It further explores time-multiplexed patterns for data placement in the CGRA memories. Nevertheless, the data can also be exchanged among different nodes over NoC structure simultaneously and independently by using direct memory access devices. In this experimental work, the performance of each CGRA, the collective performance of the whole platform and the NoC traffic are recorded in terms of the number of clock cycles and several high-level performance metrics. Today’s HMAs are generally over or under resourced for the applications that they are designed for and thus not an optimal choice for the end user. Apart from the interesting comparisons to the other state-of-the-art, our experimental setup has provided important insight and guidelines that the designers can use to implement near-optimal solutions for their target applications.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Electronics and Communications Engineering, Research group: System-on-Chip for GNSS, Wireless Communications and Cyber-Physical Embedded Computing, Research group: Wireless Communications and Positioning, Research group: System-on-Chip for GNSS, Wireless Communications and Cyber-Physical Embedded Computing
Contributors: Nouri, S., Hussain, W., Nurmi, J.
Number of pages: 3,187
Pages: 3171
Publication date: 1 Nov 2017
Peer-reviewed: Yes
Early online date: 22 May 2017

Publication information

Journal: IEEE Transactions on Parallel and Distributed Systems
ISSN (Print): 1045-9219
Ratings:

Scopus rating (2017): CiteScore 9.8 SJR 0.983 SNIP 2.917
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
Electronic versions:

bare_jrnl_compsoc
DOIs:

10.1109/TPDS.2017.2706691

URLs:
http://urn.fi/URN:NBN:fi:tty-201802141224
Research output: Contribution to journal › Article › Scientific › peer-review

Gamified crowdsourcing: Conceptualization, literature review, and future agenda

Two parallel phenomena are gaining attention in human–computer interaction research: gamification and crowdsourcing. Because crowdsourcing's success depends on a mass of motivated crowdsourcees, crowdsourcing platforms have increasingly been imbued with motivational design features borrowed from games; a practice often called gamification. While the body of literature and knowledge of the phenomenon have begun to accumulate, we still lack a comprehensive and systematic understanding of conceptual foundations, knowledge of how gamification is used in crowdsourcing, and whether it is effective. We first provide a conceptual framework for gamified crowdsourcing systems in order to understand and conceptualize the key aspects of the phenomenon. The paper's main contributions are derived through a systematic literature review that investigates how gamification has been examined in different types of crowdsourcing in a variety of domains. This meticulous mapping, which focuses on all aspects in our framework, enables us to infer what kinds of gamification efforts are effective in different crowdsourcing approaches as well as to point to a number of research gaps and lay out future research directions for gamified crowdsourcing systems. Overall, the results indicate that gamification has been an effective approach for increasing crowdsourcing participation and the quality of the crowdsourced work; however, differences exist between different types of crowdsourcing: the research conducted in the context of crowdsourcing of homogenous tasks has most commonly used simple gamification implementations, such as points and leaderboards, whereas crowdsourcing implementations that seek diverse and creative contributions employ gamification with a richer set of mechanics.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Research group: TUT Game Lab, Pervasive Computing, Robert Bosch GmbH, Karlsruhe Institute of Technology, Insitute for Technical Physics, Germany, Gamification Group
Contributors: Morschheuser, B., Hamari, J., Koivisto, J., Maedche, A.
Number of pages: 18
Pages: 26-43
Publication date: 1 Oct 2017
Peer-reviewed: Yes

Publication information

Journal: International Journal of Human-Computer Studies
Volume: 106
ISSN (Print): 1071-5819
Ratings:
Scopus rating (2017): CiteScore 5.9 SJR 0.605 SNIP 2.146
Original language: English
ASJC Scopus subject areas: Human Factors and Ergonomics, Software, Education, Engineering(all), Human-Computer Interaction, Hardware and Architecture
Keywords: Crowdsourcing, Gamification, Human computation, Literature review, Persuasive technology, Research agenda
DOIs:
10.1016/j.ijhcs.2017.04.005
Source: Scopus
Source ID: 85019568466
Research output: Contribution to journal › Article › Scientific › peer-review

Hardware design methodology using lightweight dataflow and its integration with low power techniques

Dataflow models of computation are capable of providing high-level descriptions for hardware and software components and systems, facilitating efficient processes for system-level design. The modularity and parallelism of dataflow representations make them suitable for key aspects of design exploration and optimization, such as efficient scheduling, task synchronization, memory and power management. The lightweight dataflow (LWDF) programming methodology provides an abstract programming model that supports dataflow-based design of signal processing hardware and software components and systems. Due to its formulation in terms of abstract application programming interfaces, the LWDF methodology can be integrated with a wide variety of simulation- and implementation-oriented languages, and can be targeted across different platforms, which allows engineers to integrate dataflow modeling approaches relatively easily into existing design processes. Previous work on LWDF techniques has emphasized their application to DSP software implementation (e.g., through integration with C and CUDA). In this paper, we efficiently integrate the LWDF methodology with hardware description languages (HDLs), and we apply this HDL-integrated form of the methodology to develop efficient methods for low power DSP hardware implementation. The effectiveness of the proposed LWDF-based hardware design methodology is demonstrated through a case study of a deep neural network application for vehicle classification.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Pervasive Computing, Signal Processing, Research group: Vision, Research area: Computer engineering, Dept. of Electrical and Electronic Engineering, University of Maryland, PolComIng - Information Engineering Unit
Contributors: Fanni, T., Li, L., Viitanen, T., Sau, C., Xie, R., Palumbo, F., Raffo, L., Huttunen, H., Takala, J., Bhattacharyya, S. S.
Number of pages: 15
Pages: 15-29
Publication date: 1 Aug 2017
Peer-reviewed: Yes

Publication information
Journal: Journal of Systems Architecture
Volume: 78
ISSN (Print): 1383-7621
Ratings:

Scopus rating (2017): CiteScore 3 SJR 0.255 SNIP 1.274
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture
Keywords: Clock gating, Dataflow, Deep neural networks, Digital systems design, Globally asynchronous locally synchronous, Low power design, Signal processing
DOIs:

10.1016/j.sysarc.2017.06.003

Bibliographical note
INT=tie,"Xie, Renjie"
Source: Scopus
Source ID: 85020917888
Research output: Contribution to journal › Article › Scientific › peer-review

Design and implementation of adaptive signal processing systems using Markov decision processes
In this paper, we propose a novel framework, called Hierarchical MDP framework for Compact System-level Modeling (HMCSM), for design and implementation of adaptive embedded signal processing systems. The HMCSM framework applies Markov decision processes (MDPs) to enable autonomous adaptation of embedded signal processing under multidimensional constraints and optimization objectives. The framework integrates automated, MDP-based generation of optimal reconfiguration policies, dataflow-based application modeling, and implementation of embedded control software that carries out the generated reconfiguration policies. HMCSM systematically decomposes a complex, monolithic MDP into a set of separate MDPs that are connected hierarchically, and that operate more efficiently through such a modularized structure. We demonstrate the effectiveness of our new MDP-based system design framework through experiments with an adaptive wireless communications receiver.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, University of Maryland, Georgia Institute of Technology
Contributors: Li, L., Sapio, A. E., Wu, J., Liu, Y., Lee, K., Wolf, M., Bhattacharyya, S. S.
Number of pages: 6
Pages: 170-175
Publication date: 28 Jul 2017

Host publication information
Title of host publication: 2017 IEEE 28th International Conference on Application-Specific Systems, Architectures and Processors, ASAP 2017
Publisher: IEEE
ISBN (Electronic): 9781509048250
ASJC Scopus subject areas: Hardware and Architecture, Computer Networks and Communications
DOIs:

10.1109/ASAP.2017.7995275
Source: Scopus
Source ID: 85028039806
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Analysis of multipath propagation for 5G system at higher frequencies in microcellular environment

The main target of this paper is to perform the multidimensional analysis of multipath propagation at higher frequencies i.e. 15 GHz and 28 GHz, using 'sAGA' a 3D ray tracing tool. A real world outdoor Line of Sight (LOS) microcellular environment from the Yokusuka city of Japan is considered for the analysis. The simulation data acquired from the 3D ray tracing tool includes the received signal strength, power angular spectrum and the power delay profile. The different propagation mechanisms were closely analyzed. The simulation results show the difference of propagation at two frequencies i.e. 15 GHz and 28 GHz and draw a special attention on the impact of diffuse scattering at 28 GHz. In a simple outdoor microcellular environment with a valid LOS link between the transmitter and a receiver, a path loss difference of around 5.7 dB was found between 15 GHz and 28 GHz frequency of operation. However, the propagation loss at higher frequency can be compensated by using the antenna with narrow beamwidth and larger gain.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Research group: Laboratory of Radio Network Planning, Research group: Wireless Communications and Positioning
Contributors: Sheikh, M. U., Lempiäinen, J.
Number of pages: 5
Pages: 1660-1664
Publication date: 19 Jul 2017

Host publication information

Title of host publication: 2017 13th International Wireless Communications and Mobile Computing Conference, IWCMC 2017
Publisher: IEEE
ISBN (Electronic): 9781509043729
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Signal Processing
Keywords: 3D ray tracing, 5G, Microcellular, Multipath propagation, System performance
DOIs:
10.1109/IWCMC.2017.7986533
Source: Scopus
Source ID: 85027853365
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Angular wall loss model and Extended Building Penetration model for outdoor to indoor propagation

The main target of this research work is to study the provision of indoor service (coverage) using outdoor base stations at higher frequencies i.e. 10 GHz in the context of a single building scenario. In an outdoor to indoor propagation, an angular wall loss model is used in the General Building Penetration (GBP) model for estimating the additional loss at the intercept point of the building exterior wall. A novel angular wall loss model based on a separate incidence angle in azimuth and elevation plane is proposed in this paper. In the second part of this study, an Extended Building Penetration (EBP) model is proposed, and the performance of EBP model is compared with the GBP model. In EBP model, the additional fifth path known as the 'Direct path' is proposed to be included in the GBP model. Based on the evaluation results, the impact of the direct path is found significant for the indoor users having the same or closed by height as that of the height of the transmitter.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Research group: Laboratory of Radio Network Planning, Research group: Wireless Communications and Positioning, Ericsson Research
Contributors: Sheikh, M. U., Hiltunen, K., Lempiäinen, J.
Number of pages: 6
Pages: 1291-1296
Publication date: 19 Jul 2017

Host publication information

Title of host publication: 2017 13th International Wireless Communications and Mobile Computing Conference, IWCMC 2017
Publisher: IEEE
ISBN (Electronic): 9781509043729
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Signal Processing
Keywords: Angular loss, Building penetration loss, Outdoor to Indoor, Propagation, Wall loss model
DOIs:
10.1109/IWCMC.2017.7986471
Source: Scopus

Source ID: 85027886696
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Feasibility of self-backhauling in full-duplex radio access systems under QoS constraints

This paper investigates the feasibility of a radio access system with a self-backhauling access node under full-duplex and half-duplex operation modes. In particular, after making certain simplifying assumptions, closed-form solutions for the feasibility conditions of such a radio access system are derived for both of the considered operation modes. Furthermore, the analysis incorporates given quality of service (QoS) constraints for the system, defined in terms of minimum data rates. The numerical results show that the full-duplex scheme outperforms the corresponding half-duplex scheme under most circumstances, both in terms of the highest achievable rates and the highest tolerable path losses, when given the same QoS target. However, this requires a certain amount of self-interference attenuation in the access node. Performing a similar feasibility analysis without any simplifications in the system model is an important future work item.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Research group: Wireless Communications and Positioning
Contributors: Korpi, D., Riihonen, T., Valkama, M.
Number of pages: 6
Pages: 749-754
Publication date: 29 Jun 2017

Host publication information

Title of host publication: 2017 IEEE International Conference on Communications Workshops, ICC Workshops 2017
Publisher: IEEE
ISBN (Electronic): 9781509015252
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture
Electronic versions:

Authors post-print version
DOIs:

10.1109/ICCW.2017.7962748
URLs:

http://urn.fi/URN:NBN:fi:tty-201805141683
Source: Scopus
Source ID: 85026274089
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

On the prospects of full-duplex military radios

In-band full-duplex (FD) operation can be regarded as one of the greatest discoveries in civilian/commercial wireless communications so far in this century. The concept is significant because it can as much as double the spectral efficiency of wireless data transmission by exploiting the new-found capability for simultaneous transmission and reception (STAR) that is facilitated by advanced self-interference cancellation (SIC) techniques. As the first of its kind, this paper surveys the prospects of exploiting the emerging FD radio technology in military communication applications as well. In addition to spectrally efficient two-way data transmission, the STAR capability could give a major technical advantage for armed forces by allowing their radio transceivers to conduct electronic warfare at the same time when they are also receiving or transmitting information signals at the same frequency band. After providing a detailed introduction to FD transceiver architectures and SIC requirements in military communications, this paper outlines and analyzes some potential defensive and offensive applications of the STAR capability.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Research group: Wireless Communications and Positioning , Aalto University
Contributors: Riihonen, T., Korpi, D., Rantula, O., Valkama, M.
Publication date: 23 Jun 2017

Host publication information

Title of host publication: 2017 International Conference on Military Communications and Information Systems, ICMCIS 2017
Publisher: IEEE
ISBN (Electronic): 9781538638583
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems
Electronic versions:

On the Prospects of Full-Duplex Military Radios 2017
DOIs:
10.1109/ICMCIS.2017.7956490
URLs:
http://urn.fi/URN:NBN:fi:tuni-202002061911
Source: Scopus
Source ID: 85025684140
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Guest Editorial: Implementation Issues in System-on-Chip

General information
Publication status: Published
MoE publication type: B1 Article in a scientific magazine
Organisations: Electronics and Communications Engineering, Research group: System-on-Chip for GNSS, Wireless Communications and Cyber-Physical Embedded Computing, Tallinn University of Technology
Contributors: Ellervee, P., Nurmi, J.
Number of pages: 2
Pages: 269-270
Publication date: 1 Jun 2017
Peer-reviewed: No

Publication information
Journal: Journal of Signal Processing Systems
Volume: 87
Issue number: 3
ISSN (Print): 1939-8018
Ratings:
Scopus rating (2017): CiteScore 1.7 SJR 0.216 SNIP 0.632
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Electronic versions:
Guest Editorial SOC2014_v1. Embargo ended: 6/04/18
DOIs:
10.1007/s11265-017-1242-x
URLs:
http://urn.fi/URN:NBN:fi:tty-201802141232. Embargo ended: 6/04/18
Source: Scopus
Source ID: 85017177298
Research output: Contribution to journal › Editorial › Scientific

Power Mitigation by Performance Equalization in a Heterogeneous Reconfigurable Multicore Architecture
This paper presents an integrated self-aware computing model mitigating the power dissipation of a heterogeneous reconfigurable multicore architecture by dynamically scaling the operating frequency of each core. The power mitigation is achieved by equalizing the performance of all the cores for an uninterrupted exchange of data. The multicore platform consists of heterogeneous Coarse-Grained Reconfigurable Arrays (CGRAs) of application-specific sizes and a Reduced Instruction-Set Computing (RISC) core. The CGRAs and the RISC core are integrated with each other over a Network-on-Chip (NoC) of six nodes arranged in a topology of two rows and three columns. The RISC core constantly monitors and controls the performance of each CGRA accelerator by adjusting the operating frequencies unless the performance of all the CGRAs is optimally balanced over the platform. The CGRA cores on the platform are processing some of the most computationally-intensive signal processing algorithms while the RISC core establishes packet based synchronization between the cores for computation and communication. All the cores can access each other's computational and memory resources while processing the kernels simultaneously and independently of each other. Besides general-purpose processing and overall platform supervision, the RISC processor manages performance equalization among all the cores which mitigates the overall dynamic power dissipation by 20.7 % for a proof-of-concept test.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Electronics and Communications Engineering, Research group: System-on-Chip for GNSS, Wireless Communications and Cyber-Physical Embedded Computing
Contributors: Hussain, W., Hoffmann, H., Ahonen, T., Nurmi, J.

Number of pages: 11
Pages: 287–297
Publication date: Jun 2017
Peer-reviewed: Yes
Early online date: 5 May 2016

Publication information
Journal: Journal of Signal Processing Systems
Volume: 87
Issue number: 3
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2017): CiteScore 1.7 SJR 0.216 SNIP 0.632
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Modelling and Simulation, Hardware and Architecture, Information Systems, Signal Processing, Theoretical Computer Science
Keywords: CGRA, Dark silicon, Heterogeneous, Multicore, Power dissipation, Reconfigurable
DOIs:

10.1007/s11265-016-1142-5
Source: Scopus
Source ID: 84965022070
Research output: Contribution to journal › Article › Scientific › peer-review

Comparing the Built-In Application Architecture Models in the Web Browser
Depending on one's viewpoint, a generic standards-compatible web browser supports three, four or five built-in application rendering and programming models. In this paper, we provide an overview of the built-in client-side web application architectures. While the dominance of the base HTML/CSS/JS technologies cannot be ignored, we foresee Web Components and WebGL gaining popularity as the world moves towards more complex and even richer web applications, including systems supporting virtual and augmented reality.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Nokia, University of Helsinki, USI Lugano
Contributors: Taivalsaari, A., Mikkonen, T., Pautasso, C., Systä, K.
Number of pages: 4
Pages: 51-54
Publication date: 16 May 2017

Host publication information
Title of host publication: 2017 IEEE International Conference on Software Architecture (ICSA)
Publisher: IEEE
Article number: 7930198
ISBN (Electronic): 9781509057290
ASJC Scopus subject areas: Software, Computer Networks and Communications, Hardware and Architecture
Keywords: web application architectures, Web development
DOIs:

10.1109/ICSA.2017.23

Bibliographical note
EXT="Taivalsaari, Antero"
EXT="Mikkonen, Tommi"
jufoid=69204
Source: Scopus
Source ID: 85021433872
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Low power design methodology for signal processing systems using lightweight dataflow techniques
Dataflow modeling techniques facilitate many aspects of design exploration and optimization for signal processing systems, such as efficient scheduling, memory management, and task synchronization. The lightweight dataflow (LWDF) programming methodology provides an abstract programming model that supports dataflow-based design and implementation of signal processing hardware and software components and systems. Previous work on LWDF techniques has emphasized their application to DSP software implementation. In this paper, we present new extensions of the LWDF methodology for effective integration with hardware description languages (HDLs), and we apply these extensions to develop efficient methods for low power DSP hardware implementation. Through a case study of a deep

neural network application for vehicle classification, we demonstrate our proposed LWDF-based hardware design methodology, and its effectiveness in low power implementation of complex signal processing systems.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Signal Processing, Research group: Vision, Research area: Computer engineering, University of Maryland, Dept. of Electrical and Electronic Engineering, PolComIng - Information Engineering Unit, Department of Electrical and Computer Engineering
Contributors: Li, L., Fanni, T., Viitanen, T., Xie, R., Palumbo, F., Raffo, L., Huttunen, H., Takala, J., Bhattacharyya, S. S.
Number of pages: 8
Pages: 82-89
Publication date: 13 Feb 2017

Host publication information
Title of host publication: DASIP 2016 - Proceedings of the 2016 Conference on Design and Architectures for Signal and Image Processing
Publisher: IEEE COMPUTER SOCIETY PRESS
ISBN (Electronic): 9791092279153
ASJC Scopus subject areas: Computer Graphics and Computer-Aided Design, Computer Vision and Pattern Recognition, Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
DOIs:

10.1109/DASIP.2016.7853801

Bibliographical note
INT=tie,"Xie, Renjie"
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Experimental evaluation of dynamic licensed shared access operation in live 3GPP LTE system
As next-generation mobile networks are rapidly taking shape driven by the target standardization requirements and initial trial implementations, a range of accompanying technologies prepare to support them with more reliable wireless access and improved service provisioning. Among these are more advanced spectrum sharing options enabled by the emerging Licensed Shared Access (LSA) regulatory framework, which aims to efficiently employ the capacity of underutilized frequency bands in a controlled manner. The concept of LSA promises to equip network operators with the much needed additional spectrum on the secondary basis and thus brings changes to the existing cellular network management. Hence, additional research is in prompt demand to determine the required levels of Quality of Service (QoS) and service provisioning reliability, especially in cases of dynamic geographical and temporal LSA sharing. Motivated by this recent urge and having at our disposal a fully-functional 3GPP LTE cellular deployment, we have committed to implement and trial the principles of dynamic LSA-compatible spectrum management. This paper is our first disclosure on the comprehensive experimental evaluation of this promising technology. We expect that these unprecedented practical results together with the key lessons learned will become a valuable reference point for the subsequent integration of flexible LSA-based services, suitable for inter-operator and multi-tenant spectrum sharing.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Research group: Emerging Technologies for Nano-Bio-Info-Cogno, Brno University of Technology, Peoples' Friendship University of Russia, Department of Applied Probability and Informatics
Contributors: Masek, P., Mokrov, E., Pyattaev, A., Zeman, K., Ponomarenko-Timofeev, A., Samuylov, A., Sopin, E., Hosek, J., Gudkova, I. A., Andreev, S., Novotny, V., Koucheryavy, Y., Samouylov, K.
Publication date: 2 Feb 2017

Host publication information
Title of host publication: 2016 IEEE Global Communications Conference (GLOBECOM)
Publisher: IEEE
ISBN (Electronic): 9781509013289
ASJC Scopus subject areas: Computational Theory and Mathematics, Computer Networks and Communications, Hardware and Architecture, Safety, Risk, Reliability and Quality
DOIs:

10.1109/GLOCOM.2016.7841826
Source: Scopus
Source ID: 85015456087
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Stop it, and be stubborn!

This publication discusses how automatic verification of concurrent systems can be made more efficient by focusing on always may-terminating systems. First, making a system always may-terminating is a method formeeting a modelling need that exists independently of this publication. It is illustrated that without doing so, non-progress errors may be lost. Second, state explosion is often alleviated with stubborn, ample, and persistent set methods. They use expensive cycle or terminal strong component conditions in many cases. It is proven that for many important classes of properties, if the systems are always may-terminating, then these conditions can be left out.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Mathematics, Research group: MAT Computer Science and Applied Logics
Contributors: Valmari, A.
Publication date: 1 Jan 2017
Peer-reviewed: Yes

Publication information

Journal: ACM Transactions on Embedded Computing Systems
Volume: 16
Issue number: 2
Article number: 46
ISSN (Print): 1539-9087
Ratings:

Scopus rating (2017): CiteScore 2.5 SJR 0.32 SNIP 1.093
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture
Keywords: Ignoring problem, Safety/progress/liveness properties, Stubborn set/ample set/persistent set/partial order methods
DOIs:

10.1145/3012279
Source: Scopus
Source ID: 85011350059
Research output: Contribution to journal › Article › Scientific › peer-review

A Hybrid Task Graph Scheduler for High Performance Image Processing Workflows

Designing applications for scalability is key to improving their performance in hybrid and cluster computing. Scheduling code to utilize parallelism is difficult, particularly when dealing with data dependencies, memory management, data motion, and processor occupancy. The Hybrid Task Graph Scheduler (HTGS) improves programmer productivity when implementing hybrid workflows for multi-core and multi-GPU systems. The Hybrid Task Graph Scheduler (HTGS) is an abstract execution model, framework, and API that increases programmer productivity when implementing hybrid workflows for such systems. HTGS manages dependencies between tasks, represents CPU and GPU memories independently, overlaps computations with disk I/O and memory transfers, keeps multiple GPUs occupied, and uses all available compute resources. Through these abstractions, data motion and memory are explicit; this makes data locality decisions more accessible. To demonstrate the HTGS application program interface (API), we present implementations of two example algorithms: (1) a matrix multiplication that shows how easily task graphs can be used; and (2) a hybrid implementation of microscopy image stitching that reduces code size by ≈ 43% compared to a manually coded hybrid workflow implementation and showcases the minimal overhead of task graphs in HTGS. Both of the HTGS-based implementations show good performance. In image stitching the HTGS implementation achieves similar performance to the hybrid workflow implementation. Matrix multiplication with HTGS achieves 1.3x and 1.8x speedup over the multi-threaded OpenBLAS library for 16k × 16k and 32k × 32k size matrices, respectively.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Pervasive Computing, Research area: Computer engineering, University of Maryland Baltimore County, National Institute of Standards and Technology, Department of Electrical and Computer Engineering, University of Maryland
Contributors: Blattner, T., Keyrouz, W., Bhattacharyya, S. S., Halem, M., Brady, M.
Number of pages: 11
Pages: 457–467
Publication date: 2017
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
Volume: 89
Issue number: 3
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2017): CiteScore 1.7 SJR 0.216 SNIP 0.632
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Dataflow, Heterogeneous architectures, Hybrid workflows, Image processing, Matrix multiplication, Task graph
DOIs:

10.1007/s11265-017-1262-6
Source: Scopus
Source ID: 85025108758
Research output: Contribution to journal › Article › Scientific › peer-review

Data Flow Algorithms for Processors with Vector Extensions: Handling Actors With Internal State
Full use of the parallel computation capabilities of present and expected CPUs and GPUs requires use of vector extensions. Yet many actors in data flow systems for digital signal processing have internal state (or, equivalently, an edge that loops from the actor back to itself) that impose serial dependencies between actor invocations that make vectorizing across actor invocations impossible. Ideally, issues of inter-thread coordination required by serial data dependencies should be handled by code written by parallel programming experts that is separate from code specifying signal processing operations. The purpose of this paper is to present one approach for so doing in the case of actors that maintain state. We propose a methodology for using the parallel scan (also known as prefix sum) pattern to create algorithms for multiple simultaneous invocations of such an actor that results in vectorizable code. Two examples of applying this methodology are given: (1) infinite impulse response filters and (2) finite state machines. The correctness and performance of the resulting IIR filters and one class of FSMs are studied.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Pervasive Computing, Research area: Computer engineering, Signal Processing Research Community (SPRC), Keysight Technologies, University of Maryland
Contributors: Barford, L., Bhattacharyya, S. S., Liu, Y.
Pages: 21-31
Publication date: 2017
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
Volume: 87
Issue number: 1
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2017): CiteScore 1.7 SJR 0.216 SNIP 0.632
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Modelling and Simulation, Hardware and Architecture, Information Systems, Signal Processing, Theoretical Computer Science
Keywords: Data flow computing, Digital signal processing, Graphics processing units, Parallel algorithms, Vector processors
DOIs:

10.1007/s11265-015-1045-x
Source: Scopus
Source ID: 84946115179
Research output: Contribution to journal › Article › Scientific › peer-review

Design Flow for GPU and Multicore Execution of Dynamic Dataflow Programs
Dataflow programming has received increasing attention in the age of multicore and heterogeneous computing. Modular and concurrent dataflow program descriptions enable highly automated approaches for design space exploration, optimization and deployment of applications. A great advance in dataflow programming has been the recent introduction of the RVC-CAL language. Having been standardized by the ISO, the RVC-CAL dataflow language provides a solid basis for the development of tools, design methodologies and design flows. This paper proposes a novel design flow for mapping RVC-CAL dataflow programs to parallel and heterogeneous execution platforms. Through the proposed design flow the programmer can describe an application in the RVC-CAL language and map it to multi- and many-core platforms, as well

as GPUs, for efficient execution. The functionality and efficiency of the proposed approach is demonstrated by a parallel implementation of a video processing application and a run-time reconfigurable filter for telecommunications. Experiments are performed on GPU and multicore platforms with up to 16 cores, and the results show that for high-performance applications the proposed design flow provides up to 4 × higher throughput than the state-of-the-art approach in multicore execution of RVC-CAL programs.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Pervasive Computing, Research area: Computer engineering, Center for Machine Vision and Signal Analysis, Univ of Oulu
Contributors: Boutellier, J., Nyländen, T.
Number of pages: 10
Pages: 469–478
Publication date: 2017
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
Volume: 89
Issue number: 3
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2017): CiteScore 1.7 SJR 0.216 SNIP 0.632
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Dataflow computing, Design automation, Parallel processing, Signal processing
DOIs:

10.1007/s11265-017-1260-8
Source: Scopus
Source ID: 85021239311
Research output: Contribution to journal › Article › Scientific › peer-review

Exploiting D2D communications at the network edge for mission-critical IoT applications
The advent of the Internet of Things (IoT) is boosting a wide range of new multimedia applications driven by an ecosystems of "smart" and highly heterogeneous devices. This introduces new challenges for industries and network operators in the design of next-to-come fifth generation (5G) wireless systems, where stringent performance requirements in terms of high data rate, improved reliability, and ultra-low latency are to be met. A viable way of development is the integration of local clouds at the edge of the network as part of the recent Edge Computing paradigm. However, poor channel conditions experienced by the devices towards the serving edge node may impede the effectiveness of managing mission-critical IoT applications. In this context, Device-to-Device (D2D) communications represent a key enabling technology, which offers decisive benefits for future mobile 5G scenarios. As proposed in this paper, edgebased IoT applications may rely on D2D transmissions between the IoT devices also in the presence of mobility. In particular, a forwarding scheme is proposed showing that whenever collaborating IoT devices fall under the coverage of neighboring cellular edge nodes, D2D communications can guarantee a significant reduction in delay and traffic load across the network. The proposed solution is validated through simulations that indicate significant improvements in terms of latency, percentage of served tasks, energy efficiency, and traffic load w.r.t. the case where all communications are forwarded over the edge nodes.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Universita degli Studi di Reggio Calabria, Peoples' Friendship University of Russia
Contributors: Orsino, A., Farris, I., Militano, L., Araniti, G., Andreev, S., Gudkova, I. A., Koucheryavy, Y., Iera, A.
Publication date: 2017

Host publication information
Title of host publication: European Wireless 2017 - 23rd European Wireless Conference
Publisher: VDE
ISBN (Electronic): 9783800744268
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture
Keywords: 5G, D2D communications, Edge computing, Internet of things, Narrowband IoT
Source: Scopus

Source ID: 85030722840
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Implementation of a Multirate Resampler for Multi-carrier Systems on GPUs

Efficient sample rate conversion is of widespread importance in modern communication and signal processing systems. Although many efficient kinds of polyphase filterbank structures exist for this purpose, they are mainly geared toward serial, custom, dedicated hardware implementation for a single task. There is, therefore, a need for more flexible sample rate conversion systems that are resource-efficient, and provide high performance. To address these challenges, we present in this paper an all-software-based, fully parallel, multirate resampling method based on graphics processing units (GPUs). The proposed approach is well-suited for wireless communication systems that have simultaneous requirements on high throughput and low latency. Utilizing the multidimensional architecture of GPUs, our design allows efficient parallel processing across multiple channels and frequency bands at baseband. The resulting architecture provides flexible sample rate conversion that is designed to address modern communication requirements, including real-time processing of multiple carriers simultaneously.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Pervasive Computing, University of Maryland
Contributors: Kim, S. C., Bhattacharyya, S. S.
Number of pages: 11
Pages: 445–455
Publication date: 2017
Peer-reviewed: Yes
Early online date: 30 Mar 2017

Publication information

Journal: Journal of Signal Processing Systems
Volume: 89
Issue number: 3
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2017): CiteScore 1.7 SJR 0.216 SNIP 0.632
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Carrier aggregation, GPU-based radio, Multirate signal processing, Polyphase decimator, Polyphase interpolator, Polyphase resampler
DOIs:

10.1007/s11265-017-1239-5
Source: Scopus
Source ID: 85016560476
Research output: Contribution to journal › Article › Scientific › peer-review

Parallel Digital Predistortion Design on Mobile GPU and Embedded Multicore CPU for Mobile Transmitters

Digital predistortion (DPD) is a widely adopted baseband processing technique in current radio transmitters. While DPD can effectively suppress unwanted spurious spectrum emissions stemming from imperfections of analog RF and baseband electronics, it also introduces extra processing complexity and poses challenges on efficient and flexible implementations, especially for mobile cellular transmitters, considering their limited computing power compared to basestations. In this paper, we present high data rate implementations of broadband DPD on modern embedded processors, such as mobile GPU and multicore CPU, by taking advantage of emerging parallel computing techniques for exploiting their computing resources. We further verify the suppression effect of DPD experimentally on real radio hardware platforms. Performance evaluation results of our DPD design demonstrate the high efficacy of modern general purpose mobile processors on accelerating DPD processing for a mobile transmitter.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Electronics and Communications Engineering, Research group: Wireless Communications and Positioning , Rice University, Univ of Oulu
Contributors: Li, K., Ghazi, A., Tarver, C., Boutellier, J., Abdelaziz, M., Anttila, L., Juntti, M., Valkama, M., Cavallaro, J. R.
Number of pages: 14
Pages: 417–430
Publication date: 2017

Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
Volume: 89
Issue number: 3
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2017): CiteScore 1.7 SJR 0.216 SNIP 0.632
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: CUDA, Digital predistortion, Mobile SoC, NEON SIMD, Software-defined radio
Electronic versions:

Parallel Digital Predistortion Design on Mobile GPU 2017
DOIs:

10.1007/s11265-017-1233-y
URLs:

http://urn.fi/URN:NBN:fi:tuni-202002041822
Source: Scopus
Source ID: 85013872658
Research output: Contribution to journal › Article › Scientific › peer-review

Urban 3D segmentation and modelling from street view images and LiDAR point clouds
3D urban maps with semantic labels and metric information are not only essential for the next generation robots such autonomous vehicles and city drones, but also help to visualize and augment local environment in mobile user applications. The machine vision challenge is to generate accurate urban maps from existing data with minimal manual annotation. In this work, we propose a novel methodology that takes GPS registered LiDAR (Light Detection And Ranging) point clouds and street view images as inputs and creates semantic labels for the 3D points clouds using a hybrid of rule-based parsing and learning-based labelling that combine point cloud and photometric features. The rule-based parsing boosts segmentation of simple and large structures such as street surfaces and building facades that span almost 75% of the point cloud data. For more complex structures, such as cars, trees and pedestrians, we adopt boosted decision trees that exploit both structure (LiDAR) and photometric (street view) features. We provide qualitative examples of our methodology in 3D visualization where we construct parametric graphical models from labelled data and in 2D image segmentation where 3D labels are back projected to the street view images. In quantitative evaluation we report classification accuracy and computing times and compare results to competing methods with three popular databases: NAVTEQ True, Paris-Rue-Madame and TLS (terrestrial laser scanned) Velodyne.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing, Research group: Vision, Nokia
Contributors: Babahajiani, P., Fan, L., Kämäräinen, J., Gabbouj, M.
Number of pages: 16
Pages: 679–694
Publication date: 2017
Peer-reviewed: Yes

Publication information
Journal: Machine Vision and Applications
Volume: 28
Issue number: 7
ISSN (Print): 0932-8092
Ratings:

Scopus rating (2017): CiteScore 5.3 SJR 0.485 SNIP 1.683
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture, Computer Vision and Pattern Recognition, Computer Science Applications
Keywords: LiDAR, Point cloud, Robotics, Semantic segmentation, Street view, Urban 3D
Electronic versions:

Urban 3D segmentation and modelling from street view images and LiDAR point clouds
DOIs:

10.1007/s00138-017-0845-3
URLs:

http://urn.fi/URN:NBN:fi:tty-201706121590

Bibliographical note
EXT="Babahajiani, Pouria"
Source: Scopus
Source ID: 85019692066
Research output: Contribution to journal › Article › Scientific › peer-review

Wireless M-bus in industrial IoT: Technology overview and prototype implementation
During the past 15 years, the Internet revolution has redefined the industry landscape. The advent of the Internet of Things (IoT) is changing our lives by provisioning a wide range of novel applications that leverage the ecosystem of "smart" and highly heterogeneous devices. This is expected to dramatically transform manufacturing, energy, agriculture, transportation, and other industrial sectors. The Industrial Internet of Things (IIoT) brings along a new wave of Internet evolution and will offer unprecedented opportunities in Machine Type Communications (MTC) - intelligent industrial products, processes, and services that communicate with each other and with people over the global network. This paper delivers a technology overview of the currently utilized Wireless M-Bus communication protocol within the IIoT landscape together with describing a demonstration prototype development. In our trial implementation, the IQRF modules are utilized to be compatible with the protocol of interest. The constructed WM-Bus receiver is further integrated as part of a complex MTC Gateway, which receives the MTC data via a secure communication channel from various types of smart-metering devices.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Electronics and Communications Engineering, Brno University of Technology, Peoples' Friendship University of Russia, Telekom Austria Group
Contributors: Zeman, K., Masek, P., Krejci, J., Ometov, A., Hosek, J., Andreev, S., Kröpfl, F.
Publication date: 2017

Host publication information
Title of host publication: European Wireless 2017 - 23rd European Wireless Conference
Publisher: VDE
ISBN (Electronic): 9783800744268
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture
Source: Scopus
Source ID: 85030657944
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Xor-Masking: A Novel Statistical Method for Instruction Read Energy Reduction in Contemporary SRAM Technologies
Pervasive computing calls for ultra-low-power devices to extend the battery life enough to enable usability in everyday life. Especially in devices involving programmable processors, the energy consumption of integrated memories often plays a critical role. Consequently, contemporary memory technologies focus more on the energy-efficiency aspects with new custom CMOS SRAM cells with tailored energy consumption profiles constantly being proposed.

This paper proposes a method that exploits such contemporary low power SRAM memories that are energy optimized for storing a certain logic value to improve the energy-efficiency of instruction fetching, a major energy overhead in programmable designs. The method utilizes a low overhead xor-masking approach combined with statistical program analysis to produce optimal masks to reduce the occurrence of the more energy consuming bit values in the fetched instructions.

In comparison to the "bus invert" technique typically used with similar SRAMs, the proposed method incurs minimal area overhead while still reducing the total energy consumption of an example LatticeMico32 core up to 5%. The improvement to instruction memory energy consumption alone is up to 13% with a set of benchmarks.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Department of Pervasive Computing, Research area: Computer engineering
Contributors: Multanen, J., Viitanen, T., Jääskeläinen, P., Takala, J.
Number of pages: 6
Publication date: 12 Dec 2016

Host publication information
Title of host publication: 2016 IEEE International Workshop on Signal Processing Systems (SiPS)
Publisher: IEEE

ISBN (Electronic): 978-1-5090-3361-4
ASJC Scopus subject areas: Hardware and Architecture
Electronic versions:
Xormasking
DOIs:
10.1109/SiPS.2016.19
URLs:
http://urn.fi/URN:NBN:fi:tty-201702061097
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Models of architecture: Reproducible efficiency evaluation for signal processing systems

The current trend in high performance and embedded signal processing consists of designing increasingly complex heterogeneous hardware architectures with non-uniform communication resources. In order to take hardware and software design decisions, early evaluations of the system non-functional properties are needed. These evaluations of system efficiency require high-level information on both the algorithms and the architecture. In this paper, we define the notion of Model of Architecture (MoA) and study the combination of a Model of Computation (MoC) and an MoA to provide a design space exploration environment for the study of the algorithmic and architectural choices. A cost is computed from the mapping of an application, represented by a model conforming a MoC onto an architecture represented by a model conforming an MoA. The cost is composed of a processing-related part and a communicationrelated part. It is an abstract scalar value to be minimized and can represent any non-functional requirement of a system such as memory, energy, throughput or latency.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pervasive Computing, Research area: Computer engineering, Institut Pascal, UBL, Scuola Superiore sant'Anna, Salzburg University of Applied Sciences, University of Maryland
Contributors: Pelcat, M., Desnos, K., Maggiani, L., Liu, Y., Heulot, J., Nezan, J. F., Bhattacharyya, S. S.
Number of pages: 6
Pages: 121-126
Publication date: 9 Dec 2016

Host publication information
Title of host publication: IEEE International Workshop on Signal Processing Systems, SiPS 2016
Publisher: IEEE
Article number: 7780083
ISBN (Electronic): 9781509033614

Publication series
Name: IEEE International Workshop on Signal Processing Systems
ISSN (Electronic): 2374-7390
ASJC Scopus subject areas: Electrical and Electronic Engineering, Signal Processing, Applied Mathematics, Hardware and Architecture
DOIs:
10.1109/SiPS.2016.29
Source: Scopus
Source ID: 85013141986
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Adaptive tracking of people and vehicles using mobile platforms

Tracking algorithms have important applications in detection of humans and vehicles for border security and other areas. For large-scale deployment of such algorithms, it is critical to provide methods for their cost- and energy-efficient realization. To this end, commodity mobile devices have significant potential for use as prototyping and testing platforms due to their low cost, widespread availability, and integration of advanced communications, sensing, and processing features. Prototypes developed on mobile platforms can be tested, fine-tuned, and demonstrated in the field and then provide reference implementations for application-specific disposable sensor node implementations that are targeted for deployment. In this paper, we develop a novel, adaptive tracking system that is optimized for energy-efficient, real-time operation on off-the-shelf mobile platforms. Our tracking system applies principles of dynamic data-driven application systems (DDDAS) to periodically monitor system operating characteristics and apply these measurements to dynamically adapt the specific classifier configurations that the system employs. Our resulting adaptive approach enables powerful optimization of trade-offs among energy consumption, real-time performance, and tracking accuracy based on time-varying changes in operational characteristics. Through experiments employing an Android-based tablet platform, we demonstrate the efficiency of our proposed tracking system design for multimode detection of human and vehicle targets.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Pervasive Computing, Research area: Computer engineering, University of Maryland, U.S. Army Research Laboratory, Technische Universitat Munchen
Contributors: Ben Salem, H., Damarla, T., Sudusinghe, K., Stechele, W., Bhattacharyya, S. S.
Publication date: 1 Dec 2016
Peer-reviewed: Yes

Publication information
Journal: Eurasip Journal on Advances in Signal Processing
Volume: 2016
Issue number: 1
Article number: 65
ISSN (Print): 1687-6172
Ratings:

Scopus rating (2016): CiteScore 2.5 SJR 0.345 SNIP 1.088
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
Keywords: Acoustic sensors, Dataflow graphs, DDDAS, Mobile platforms, Signal processing systems, Target tracking
Electronic versions:

Adaptive tracking of people and vehicles using mobile platforms
DOIs:

10.1186/s13634-016-0356-9
URLs:

http://urn.fi/URN:NBN:fi:tty-201606284314
Source: Scopus
Source ID: 84971500315
Research output: Contribution to journal › Article › Scientific › peer-review

Generalized Hampel Filters
The standard median filter based on a symmetric moving window has only one tuning parameter: the window width. Despite this limitation, this filter has proven extremely useful and has motivated a number of extensions: weighted median filters, recursive median filters, and various cascade structures. The Hampel filter is a member of the class of decsion filters that replaces the central value in the data window with the median if it lies far enough from the median to be deemed an outlier. This filter depends on both the window width and an additional tuning parameter t, reducing to the median filter when t=0, so it may be regarded as another median filter extension. This paper adopts this view, defining and exploring the class of generalized Hampel filters obtained by applying the median filter extensions listed above: weighted Hampel filters, recursive Hampel filters, and their cascades. An important concept introduced here is that of an implosion sequence, a signal for which generalized Hampel filter performance is independent of the threshold parameter t. These sequences are important because the added flexibility of the generalized Hampel filters offers no practical advantage for implosion sequences. Partial characterization results are presented for these sequences, as are useful relationships between root sequences for generalized Hampel filters and their median-based counterparts. To illustrate the performance of this filter class, two examples are considered: one is simulation-based, providing a basis for quantitative evaluation of signal recovery performance as a function of t, while the other is a sequence of monthly Italian industrial production index values that exhibits glaring outliers.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Signal Processing, Research group: Video, DataRobot, Aalto University
Contributors: Pearson, R. K., Neuvo, Y., Astola, J., Gabbouj, M.
Publication date: 1 Dec 2016
Peer-reviewed: Yes

Publication information
Journal: Eurasip Journal on Advances in Signal Processing
Volume: 2016
Issue number: 1
Article number: 87
ISSN (Print): 1687-6172
Ratings:

Scopus rating (2016): CiteScore 2.5 SJR 0.345 SNIP 1.088
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering

Electronic versions:

Generalized Hampel Filters
DOIs:

10.1186/s13634-016-0383-6
URLs:

http://urn.fi/URN:NBN:fi:tty-201608254463
Source: Scopus
Source ID: 84981165367
Research output: Contribution to journal › Article › Scientific › peer-review

Optimization of Flexible Filter Banks Based on Fast Convolution

Multirate filter banks can be implemented efficiently using fast-convolution (FC) processing. The main advantage of the FC filter banks (FC-FB) compared with the conventional polyphase implementations is their increased flexibility, that is, the number of channels, their bandwidths, and the center frequencies can be independently selected. In this paper, an approach to optimize the FC-FBs is proposed. First, a subband representation of the FC-FB is derived. Then, the optimization problems are formulated with the aid of the subband model. Finally, these problems are conveniently solved with the aid of a general nonlinear optimization algorithm. Several examples are included to demonstrate the proposed overall design scheme as well as to illustrate the efficiency and the flexibility of the resulting FC-FB.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Electronics and Communications Engineering, Research group: Wireless Communications and Positioning
Contributors: Yli-Kaakinen, J., Renfors, M.
Pages: 101-111
Publication date: Aug 2016
Peer-reviewed: Yes

Publication information

Journal: Journal of Signal Processing Systems
Volume: 85
Issue number: 1
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2016): CiteScore 1.6 SJR 0.212 SNIP 0.677
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Modelling and Simulation, Hardware and Architecture, Information Systems, Signal Processing, Theoretical Computer Science
Keywords: Digital filters, Filter banks, Multirate signal processing, Optimization, Sampling rate conversion
DOIs:

10.1007/s11265-015-1004-6
Source: Scopus
Source ID: 84929682954
Research output: Contribution to journal › Article › Scientific › peer-review

SoftWater: Software-defined networking for next-generation underwater communication systems

Underwater communication systems have drawn the attention of the research community in the last 15 years. This growing interest can largely be attributed to new civil and military applications enabled by large-scale networks of underwater devices (e.g., underwater static sensors, unmanned autonomous vehicles (AUVs), and autonomous robots), which can retrieve information from the aquatic and marine environment, perform in-network processing on the extracted data, and transmit the collected information to remote locations. Currently underwater communication systems are inherently hardware-based and rely on closed and inflexible architectural design. This imposes significant challenges into adopting new underwater communication and networking technologies, prevent the provision of truly-differentiated services to highly diverse underwater applications, and induce great barriers to integrate heterogeneous underwater devices. Software-defined networking (SDN), recognized as the next-generation networking paradigm, relies on the highly flexible, programmable, and virtualizable network architecture to dramatically improve network resource utilization, simplify network management, reduce operating cost, and promote innovation and evolution. In this paper, a software-defined architecture, namely SoftWater, is first introduced to facilitate the development of the next-generation underwater communication systems. More specifically, by exploiting the network function virtualization (NFV) and network virtualization concepts, SoftWater architecture can easily incorporate new underwater communication solutions, accordingly maximize the network capacity, can achieve the network robustness and energy efficiency, as well as can provide truly differentiated and scalable networking services. Consequently, the SoftWater architecture can simultaneously support a variety of different underwater applications, and can enable the interoperability of underwater devices from different manufacturers that operate on different underwater communication technologies based on acoustic, optical, or

radio waves. Moreover, the essential network management tools of SoftWater are discussed, including reconfigurable multi-controller placement, hybrid in-band and out-of-band control traffic balancing, and utility-optimal network virtualization. Furthermore, the major benefits of SoftWater architecture are demonstrated by introducing software-defined underwater networking solutions, including the throughput-optimal underwater routing, SDN-enhanced fault recovery, and software-defined underwater mobility management. The research challenges to realize the SoftWater are also discussed in detail.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Wireless Communications and Positioning (WICO), Georgia Institute of Technology, School of Electrical and Computer Engineering, Wichita State University
Contributors: Akyildiz, I. F., Wang, P., Lin, S. C.
Publication date: Aug 2016
Peer-reviewed: Yes

Publication information
Journal: Ad Hoc Networks
Volume: 46
ISSN (Print): 1570-8705
Ratings:

Scopus rating (2016): CiteScore 6.1 SJR 0.648 SNIP 2.045
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture, Computer Networks and Communications
Keywords: SDN, Underwater communications, Virtualization
DOIs:

10.1016/j.adhoc.2016.02.016
URLs:

http://www.scopus.com/inward/record.url?scp=84992306085&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84992306085
Research output: Contribution to journal › Article › Scientific › peer-review

On the Architecture of Liquid Software: Technology Alternatives and Design Space
The liquid metaphor refers to software that operates seamlessly across multiple devices owned by one or multiple users. Liquid software architectures can dynamically deploy and redeploy stateful software components and transparently adapt them to the capabilities of heterogeneous target devices. The key design goal in liquid software development is to minimize the efforts that are related to multiple device ownership (e.g., installation, synchronization and general maintenance of personal computers, smartphones, tablets, home displays, cars and wear-able devices), while keeping the users in full control of their devices, applications and data. In this paper we present a design space for liquid software, categorizing and discussing the most important architectural issues and alternatives. These alternatives represent relevant capabilities offered by emerging technologies and deployment platforms that are then positioned and compared within the design space presented in the paper.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Department of Pervasive Computing, Research area: Software engineering, University of Lugano (USI), Nokia Technologies
Contributors: Gallidabino, A., Pautasso, C., Ilvonen, V., Mikkonen, T., Systä, K., Voutilainen, J., Taivalsaari, A.
Number of pages: 6
Pages: 122-127
Publication date: 19 Jul 2016

Host publication information
Title of host publication: Proceedings - 2016 13th Working IEEE/IFIP Conference on Software Architecture, WICSA 2016
Publisher: IEEE
ISBN (Electronic): 9781509021314
ASJC Scopus subject areas: Hardware and Architecture, Software
Keywords: design space, liquid software, Multi-device programming, multiple device owner-ship, software architecture
DOIs:

10.1109/WICSA.2016.14

Bibliographical note
EXT="Taivalsaari, Antero"

Source: Scopus
Source ID: 84983317329
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Accelerating Computation on an Android Phone with OpenCL Parallelism and Optimizing Workload Distribution between a Phone and a Cloud Service

We evaluate workload distribution optimization between an Android phone, a cloud service by considering the overall impact of both computation, data transfer. We use OpenCL parallelism on Android to obtain high computation performance. We implement an escape time algorithm to compute the Mandelbrot set with OpenCL,, with Java as a reference for comparison. In an experiment of setting the escape boundary at 256, OpenCL offers about 5.0X to 7.5X faster computation compared to Java. With a cloud service, data transfer becomes a dominant factor when the amount of computation is low. In a set of four experiments of sharing workload of computing the Mandelbrot set between a cloud service, a phone, data transfer consumes on average over 80% of processing time. In those experiments computing locally with OpenCL on an Android phone yields faster processing time. On the other hand, local computation capacity becomes a bottleneck when the amount of computation is high. With the escape boundary at 65536, requesting computation from a cloud service yields up to 7.55X speedup.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Department of Electronics and Communications Engineering, Research group: System-on-Chip for GNSS, Wireless Communications and Cyber-Physical Embedded Computing
Contributors: Wang, K., Nurmi, J., Ahonen, T.
Pages: 636-642
Publication date: 18 Jul 2016

Host publication information

Title of host publication: 2016 Intl IEEE Conferences Ubiquitous Intelligence & Computing, Advanced and Trusted Computing, Scalable Computing and Communications, Cloud and Big Data Computing, Internet of People, and Smart World Congress (UIC/ATC/ScalCom/CBDCom/IoP/SmartWorld),
Publisher: IEEE
ISBN (Electronic): 978-1-5090-2771-2
ASJC Scopus subject areas: Electrical and Electronic Engineering, Hardware and Architecture
DOIs:

10.1109/UIC-ATC-ScalCom-CBDCom-IoP-SmartWorld.2016.0106
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Investigating mid-air gestures and handhelds in motion tracked environments

Smart spaces with multiple interactive devices and motion tracking capabilities are becoming more common. However, there is little research on how interaction with one device affects the usage of other devices in the space. We investigate the effects of mobile devices and physical interactive devices on gestural interaction in motion-tracked environments. For our user study, we built a smart space consisting of a gesture-controlled large display, an NFC reader and a mobile device, to simulate a system in which users can transfer information between the space and personal devices. The study with 13 participants revealed that (1) the mobile device affects gesturing as well as passive stance; (2) users may stop moving completely when they intend to stop interacting with a display; (3) interactive devices with overlapping interaction space make unintentional interaction significantly more frequent. Our findings give implications for gestural interaction design as well as design of motion-tracked smart spaces.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Department of Pervasive Computing, Research area: User experience
Contributors: Mäkelä, V., Korhonen, H., Ojala, J., Järvi, A., Väänänen, K., Raisamo, R., Turunen, M.
Number of pages: 7
Pages: 45-51
Publication date: 20 Jun 2016

Host publication information

Title of host publication: PerDis 2016 - Proceedings of the 5th ACM International Symposium on Pervasive Displays
Publisher: ACM
ISBN (Electronic): 9781450343664
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Computer Graphics and Computer-Aided Design, Computer Science Applications
Keywords: Handhelds, Large displays, Mid-air gestures, Mobile devices, Motion-tracked environments, Smart spaces, Ubiquitous computing

Electronic versions:

Investigating_Mid_Air_Gestures_M_kel_EtAl_PerDis16

DOIs:

10.1145/2914920.2915015

URLs:

http://urn.fi/URN:NBN:fi:tty-201903291363

Bibliographical note

INT=tie,"Järvi, Antti"
Source: Scopus
Source ID: 84979742748
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

A design framework for mapping vectorized synchronous dataflow graphs onto CPU-GPU platforms

Heterogeneous computing platforms with multicore central processing units (CPUs) and graphics processing units (GPUs) are of increasing interest to designers of embedded signal processing systems since they offer the potential for significant performance boost while maintaining the flexibility of software-based design flows. Developing optimized implementations for CPU-GPU platforms is challenging due to complex, inter-related design issues, including task scheduling, interprocessor communication, memory management, and modeling and exploitation of different forms of parallelism. In this paper, we present an automated, dataflow based, design framework called DIF-GPU for application mapping and software synthesis on heterogeneous CPU-GPU platforms. DIF-GPU is based on novel extensions to the dataflow interchange format (DIF) package, which is a software environment for developing and experimenting with dataflow-based design methods and synthesis techniques for embedded signal processing systems. DIF-GPU exploits multiple forms of parallelism by deeply incorporating efficient vectorization and scheduling techniques for synchronous dataflow specifications, and incorporating techniques for streamlining interprocessor communication. DIF-GPU also provides software synthesis capabilities to help accelerate the process of moving from high-level application models to optimized implementations.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Department of Pervasive Computing, Research area: Computer engineering, University of Maryland, Fachhochschule Salzburg, College Park
Contributors: Lin, S., Liu, Y., Plishker, W., Bhattacharyya, S. S.
Number of pages: 10
Pages: 20-29
Publication date: 23 May 2016

Host publication information

Title of host publication: Proceedings of the 19th International Workshop on Software and Compilers for Embedded Systems, SCOPES 2016
Publisher: ACM
ISBN (Print): 9781450343206
ASJC Scopus subject areas: Hardware and Architecture, Software
Keywords: Dataflow, Design optimization, Heterogeneous computing, Signal processing systems, Software synthesis
DOIs:

10.1145/2906363.2906374

Source: Scopus
Source ID: 84974603317
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Extended Ewald summation technique

We present a technique to improve the accuracy and to reduce the computational labor in the calculation of long-range interactions in systems with periodic boundary conditions. We extend the well-known Ewald method by using a linear combination of screening Gaussian charge distributions instead of only one. This enables us to find faster converging real-space and reciprocal space summations. The combined simplicity and efficiency of our method is demonstrated, and the scheme is readily applicable to large-scale periodic simulations, classical as well as quantum. Moreover, apart from the required a priori optimization the method is straightforward to include in most routines based on the Ewald method within, e.g., density-functional, molecular dynamics, and quantum Monte Carlo calculations.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Physics

Contributors: Kylänpää, I., Räsänen, E.
Pages: 64–68
Publication date: 17 May 2016
Peer-reviewed: Yes

Publication information
Journal: Computer Physics Communications
Volume: 206
ISSN (Print): 0010-4655
Ratings:

Scopus rating (2016): CiteScore 7.3 SJR 1.914 SNIP 1.973
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Physics and Astronomy(all)
Keywords: Electronic structure methods, Long-range interactions, Molecular dynamics
DOIs:

10.1016/j.cpc.2016.05.005
Source: Scopus
Source ID: 84973534451
Research output: Contribution to journal › Article › Scientific › peer-review

Detection of bubbles as concentric circular arrangements
The paper proposes a method for the detection of bubble-like transparent objects in a liquid. The detection problem is non-trivial since bubble appearance varies considerably due to different lighting conditions causing contrast reversal and multiple interreflections. We formulate the problem as the detection of concentric circular arrangements (CCA). The CCAs are recovered in a hypothesize-optimize-verify framework. The hypothesis generation is based on sampling from the partially linked components of the non-maximum suppressed responses of oriented ridge filters, and is followed by the CCA parameter estimation. Parameter optimization is carried out by minimizing a novel cost-function. The performance was tested on gas dispersion images of pulp suspension and oil dispersion images. The mean error of gas/oil volume estimation was used as a performance criterion due to the fact that the main goal of the applications driving the research was the bubble volume estimation. The method achieved 28 and 13 % of gas and oil volume estimation errors correspondingly outperforming the OpenCV Circular Hough Transform in both cases and the WaldBoost detector in gas volume estimation.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Signal Processing, Research group: Vision, Research Community on Data-to-Decision (D2D), Machine Vision and Pattern Recognition Laboratory, Lappeenranta University of Technology, Computer Vision Group, Czech Technical University in Prague, Monash University Malaysia
Contributors: Strokina, N., Matas, J., Eerola, T., Lensu, L., Kälviäinen, H.
Number of pages: 10
Pages: 387-396
Publication date: Apr 2016
Peer-reviewed: Yes
Early online date: 10 Feb 2016

Publication information
Journal: Machine Vision and Applications
Volume: 27
Issue number: 3
ISSN (Print): 0932-8092
Ratings:

Scopus rating (2016): CiteScore 4.7 SJR 0.741 SNIP 1.433
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Computer Vision and Pattern Recognition, Software, Computer Science Applications
Keywords: Bubble detection, Circular arrangements, Image processing, Machine vision, Object segmentation
DOIs:

10.1007/s00138-016-0749-7
Source: Scopus
Source ID: 84957656160
Research output: Contribution to journal › Article › Scientific › peer-review

BL-LDA: Bringing bigram to supervised topic model

With the increasing amount of data being published on the Web, it is difficult to analyze their content within a short time. Topic modeling techniques can summarize textual data that contains several topics. Both the label (such as category or tag) and word co-occurrence play a significant role in understanding textual data. However, many conventional topic modeling techniques are limited to the bag-of-words assumption. In this paper, we develop a probabilistic model called Bigram Labeled Latent Dirichlet Allocation (BL-LDA), to address the limitation of the bag-of-words assumption. The proposed BL-LDA incorporates the bigram into the Labeled LDA (L-LDA) technique. Extensive experiments on Yelp data show that the proposed scheme is better than the L-LDA in terms of accuracy.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Research Community on Data-to-Decision (D2D), Korea University
Contributors: Park, Y., Alam, M. H., Ryu, W. J., Lee, S.
Number of pages: 6
Pages: 83-88
Publication date: 2 Mar 2016

Host publication information

Title of host publication: Proceedings - 2015 International Conference on Computational Science and Computational Intelligence, CSCI 2015
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 7424068
ISBN (Electronic): 9781467397957
ASJC Scopus subject areas: Computational Theory and Mathematics, Artificial Intelligence, Computer Networks and Communications, Hardware and Architecture, Signal Processing
Keywords: Data Analysis, Data Mining, Text Classification, Topic Modeling
DOIs:

10.1109/CSCI.2015.146
URLs:

http://www.scopus.com/inward/record.url?scp=84964476038&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84964476038
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Guest editorial special issue on the internet of nano things

The six papers in this special section focus on the Internet of nanotechnology things. While researchers are currently investigating these challenges to develop fully functional nano communication systems, a question remains as to whether they can represent an extended communication network that is part of the broader Internet. These papers address new solutions for the Internet of Nano Things. The Internet of Things paradigm has transformed the way we operate our personal and professional lives, it is driving our economy and will continue to enable many new opportunities in broad research areas. As this pervasive and ubiquitous interconnection of our everyday life appliances continues into the future, new types of devices enabled by nano and biotechnology promise to push engineering to previously unexplored application domains, where the exchange of information and access from/to the broader Internet for their monitoring and control are even more essential. The research on nanoscale communication and networks aims to develop systems for interconnecting these novel devices at the nanoscale, i.e., the Internet of Nano Things.

General information

Publication status: Published
MoE publication type: B1 Article in a scientific magazine
Organisations: Department of Electronics and Communications Engineering, Research group: Emerging Technologies for Nano-Bio-Info-Cogno, Nano Communication Centre, State University of New York, University of Nebraska - Lincoln
Contributors: Balasubramaniam, S., Jornet, J. M., Pierobon, M., Koucheryavy, Y.
Number of pages: 3
Pages: 1-3
Publication date: 1 Feb 2016
Peer-reviewed: No

Publication information

Journal: IEEE Internet of Things Journal
Volume: 3
Issue number: 1
ISSN (Print): 2327-4662
Ratings:

Scopus rating (2016): CiteScore 8 SJR 1.447 SNIP 6.181

Original language: English
ASJC Scopus subject areas: Computer Networks and Communications, Computer Science Applications, Hardware and Architecture, Information Systems, Signal Processing, Information Systems and Management
DOIs:
10.1109/JIOT.2016.2516838
Source: Scopus
Source ID: 84959329564
Research output: Contribution to journal › Article › Scientific

Supporting deterministic medium access control in wireless vehicular communications

The medium access is regarded as being one of the most challenging issues to solve in order to provide deterministic wireless communications in vehicular networks. It has been demonstrated that standard protocols fail to properly address this issue. The implementation of deterministic Medium Access Control (MAC) protocols is hampered by the fact that commercial devices do not allow modifications to the standard MAC mechanism, and the development of a device from scratch to implement one MAC scheme is an extremely laborious endeavor. However, over the last few years, the IT2S platform for vehicular communications has been developed and is now in a stage that allows implementation and testing of new solutions for the vehicular communications environment. This paper presents an overview of MAC mechanisms capable of providing deterministic real-time access and assesses the features a communications device should include in order to allow the implementation of these mechanisms. It then proposes an implementation of such features taking advantage of the white box access to the IT2S platform, which is not usually available in COTS devices.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Department of Signal Processing, Research group: Video, Universidade de Aveiro
Contributors: Cruz, C., Ferreira, J., Oliveira, A.
Publication date: 25 Jan 2016

Host publication information

Title of host publication: 2015 IEEE 82nd Vehicular Technology Conference, VTC Fall 2015 - Proceedings
Publisher: IEEE
ISBN (Print): 9781479980918
ASJC Scopus subject areas: Computer Networks and Communications, Automotive Engineering, Hardware and Architecture
DOIs:
10.1109/VTCFall.2015.7391160
Source: Scopus
Source ID: 84964467857
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

The influence of developer multi-homing on competition between software ecosystems

Having a large number of applications in the marketplace is considered a critical success factor for software ecosystems. The number of applications has been claimed to determine which ecosystems holds the greatest competitive advantage and will eventually dominate the market. This paper investigates the influence of developer multi-homing (i.e., participating in more than one ecosystem) in three leading mobile application ecosystems. Our results show that when regarded as a whole, mobile application ecosystems are single-homing markets. The results further show that 3% of all developers generate more than 80% of installed applications and that multi-homing is common among these developers. Finally, we demonstrate that the most installed content actually comprises only a small number of the potential value propositions. The results thus imply that attracting and maintaining developers of superstar applications is more critical for the survival of a mobile application ecosystem than the overall number of developers and applications. Hence, the mobile ecosystem is unlikely to become a monopoly. Since exclusive contracts between application developers and mobile application ecosystems are rare, multi-homing is a viable component of risk management and a publishing strategy. The study advances the theoretical understanding of the influence of multi-homing on competition in software ecosystems.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Information Technology, University of Turku, VTT Technical Research Centre of Finland
Contributors: Hyrynsalmi, S., Suominen, A., Mäntymäki, M.
Number of pages: 9
Pages: 119-127
Publication date: 1 Jan 2016
Peer-reviewed: Yes

Publication information
Journal: Journal of Systems and Software
Volume: 111
ISSN (Print): 0164-1212
Ratings:

Scopus rating (2016): CiteScore 5.3 SJR 0.617 SNIP 2.139
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Software, Information Systems
Keywords: Multi-homing, Software ecosystem, Two-sided markets
DOIs:

10.1016/j.jss.2015.08.053
Source: Scopus
Source ID: 84949783538
Research output: Contribution to journal › Article › Scientific › peer-review

Analysis of a receiver-based reliable broadcast approach for vehicular networks
The Intelligent Transportation Systems concept provides the ground to enable a wide range of applications to improve traffic safety and efficiency. Innovative communication systems must be proposed taking into account, on the one hand, unstable characteristics of vehicular communications and, on the other hand, different requirements of applications. In this paper a reliable (geo-)broadcasting scheme for vehicular ad-hoc networks is proposed and analyzed. This receiver-based technique aims at fulfilling the received message integrity yet keeping the overhead at a reasonably low level. The results are compared to simulation studies carried out in the Network Simulator-3 (NS-3) simulation environment demonstrating good agreement with each other. The analysis shows that in a single-hop scenario, receiver-based reliable broadcasting can provide good reliability, while giving very little overhead for high number of receivers.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Electronics and Communications Engineering, Research group: Emerging Technologies for Nano-Bio-Info-Cogno, University of Twente
Contributors: Gholibeigi, M., Heijenk, G., Moltchanov, D., Koucheryavy, Y.
Number of pages: 13
Pages: 63-75
Publication date: 2016
Peer-reviewed: Yes

Publication information
Journal: Ad Hoc Networks
Volume: 37
ISSN (Print): 1570-8705
Ratings:

Scopus rating (2016): CiteScore 6.1 SJR 0.648 SNIP 2.045
Original language: English
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Software
Keywords: (Geo)Broadcast, Performance modeling, Reliability, Vehicular ad hoc networks
DOIs:

10.1016/j.adhoc.2015.08.003
Source: Scopus
Source ID: 84947868264
Research output: Contribution to journal › Article › Scientific › peer-review

Gravity gradient routing for information delivery in fog Wireless Sensor Networks
Fog Computing is a new paradigm that has been proposed by CISCO to take full advantage of the ever growing computational capacity of the near-user or edge devices (e.g., wireless gateways and sensors). The paradigm proposes an architecture that enables the devices to host functionality of various user-centric services. While the prospects of Fog Computing promise numerous advantages, development of Fog Services remains under-investigated. This article considers an opportunity of Fog implementation for Alert Services on top of Wireless Sensor Network (WSN) technology. In particular, we focus on targeted WSN-alert delivery based on spontaneous interaction between a WSN and hand-held devices of its users. For the alert delivery, we propose a Gravity Routing concept that prioritizes the areas of high user-presence within the network. Based on the concept, we develop a routing protocol, namely the Gradient Gravity Routing (GGR) that combines targeted delivery and resilience to potential sensor-load heterogeneity within the network. The protocol has been compared against a set of state-of-the-art solutions via a series of simulations. The evaluation has shown the ability of GGR to match the performance of the compared solutions in terms of alert delivery ratio, while minimizing the overall energy consumption of the network.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Electronics and Communications Engineering, Research group: Emerging Technologies for Nano-Bio-Info-Cogno
Contributors: Ivanov, S., Balasubramaniam, S., Botvich, D., Akan, O. B.
Pages: 61-74
Publication date: 2016
Peer-reviewed: Yes

Publication information
Journal: Ad Hoc Networks
Volume: 46
ISSN (Print): 1570-8705
Ratings:

Scopus rating (2016): CiteScore 6.1 SJR 0.648 SNIP 2.045
Original language: English
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Software
Keywords: Fog Computing, User-awareness, Wireless sensor networks
DOIs:

10.1016/j.adhoc.2016.03.011
Source: Scopus
Source ID: 84964329276
Research output: Contribution to journal › Article › Scientific › peer-review

HARP2: An X-Scale Reconfigurable Accelerator-Rich Platform for Massively-Parallel Signal Processing Algorithms

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Electronics and Communications Engineering, Research group: System-on-Chip for GNSS, Wireless Communications and Cyber-Physical Embedded Computing, University of Chicago
Contributors: Hussain, W., Airoldi, R., Hoffmann, H., Ahonen, T., Nurmi, J.
Pages: 341-353
Publication date: 2016
Peer-reviewed: Yes
Early online date: 2015

Publication information
Journal: Journal of Signal Processing Systems
Article number: 10.1007/s11265-015-1054-9
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2016): CiteScore 1.6 SJR 0.212 SNIP 0.677
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
DOIs:

10.1007/s11265-015-1054-9
URLs:

https://rdcu.be/6sAa
Research output: Contribution to journal › Article › Scientific › peer-review

IEEE 802.11ac MIMO Transceiver Baseband Processing on a VLIW Processor
Wireless standards are evolving rapidly due to the exponential growth in the number of portable devices along with the applications with high data rate requirements. Adaptable software based signal processing implementations for these devices can make the deployment of the constantly evolving standards faster and less expensive. The flagship technology from the IEEE WLAN family, the IEEE 802.11ac, aims at achieving very high throughputs in local area connectivity scenarios. This article presents a software based implementation for the Multiple Input and Multiple Output (MIMO) transmitter and receiver baseband processing conforming to the IEEE 802.11ac standard which can achieve transmission bit rates beyond 1Gbps. This work focuses on the Physical layer frequency domain processing. Various configurations, including 2×2 and 4×4 MIMO are considered for the implementation. To utilize the available data and instruction level parallelism, a DSP core with vector extensions is selected as the implementation platform. Then, the feasibility of the presented software-based solution is assessed by studying the number of clock cycles and power consumption of the different scenarios implemented on this core. Such Software Defined Radio based approaches can potentially offer more flexibility, high energy efficiency, reduced design efforts and thus shorter time-to-market cycles in comparison with the

conventional fixed-function hardware methods.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Electronics and Communications Engineering, Research group: Wireless Communications and Positioning, Department of Pervasive Computing, Research area: Computer engineering
Contributors: Aghababaeetafreshi, M., Lehtonen, L. K., Levanen, T., Valkama, M., Takala, J.
Publication date: 2016
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2016): CiteScore 1.6 SJR 0.212 SNIP 0.677
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Modelling and Simulation, Hardware and Architecture, Information Systems, Signal Processing, Theoretical Computer Science
Keywords: MIMO, OFDM, Parallel processing, Software defined radio, VLIW, WLAN
DOIs:

10.1007/s11265-015-1032-2
URLs:

http://www.scopus.com/inward/record.url?scp=84942023616&partnerID=8YFLogxK (Link to publication in Scopus)

Bibliographical note
ORG=elt,0.5
ORG=tie,0.5
Source: Scopus
Source ID: 84942023616
Research output: Contribution to journal › Article › Scientific › peer-review

Instrumentation-Driven Validation of Dataflow Applications
Dataflow modeling offers a myriad of tools for designing and optimizing signal processing systems. A designer is able to take advantage of dataflow properties to effectively tune the system in connection with functionality and different performance metrics. However, a disparity in the specification of dataflow properties and the final implementation can lead to incorrect behavior that is difficult to detect. This motivates the problem of ensuring consistency between dataflow properties that are declared or otherwise assumed as part of dataflow-based application models, and the dataflow behavior that is exhibited by implementations that are derived from the models. In this paper, we address this problem by introducing a novel dataflow validation framework (DVF) that is able to identify disparities between an application's formal dataflow representation and its implementation. DVF works by instrumenting the implementation of an application and monitoring the instrumentation data as the application executes. This monitoring process is streamlined so that DVF achieves validation without major overhead. We demonstrate the utility of our DVF through design and implementation case studies involving an automatic speech recognition application, a JPEG encoder, and an acoustic tracking application.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Pervasive Computing, Research area: Computer engineering, Signal Processing Research Community (SPRC), University of Maryland, Technische Universitat Munchen, Institute for Advanced Computer Studies
Contributors: Chukhman, I., Jiao, Y., Salem, H. B., Bhattacharyya, S. S.
Pages: 383–397
Publication date: 2016
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
Volume: 84
Issue number: 3
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2016): CiteScore 1.6 SJR 0.212 SNIP 0.677
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Modelling and Simulation, Hardware and Architecture, Information Systems, Signal Processing, Theoretical Computer Science

Keywords: Dataflow graphs, Design validation, Models of computation, Signal processing systems
DOIs:

10.1007/s11265-015-1073-6
Source: Scopus
Source ID: 84946128443
Research output: Contribution to journal › Article › Scientific › peer-review

OpenCL Programmable Exposed Datapath High Performance Low-Power Image Signal Processor

Sophisticated computational imaging algorithms require both high performance and good energy-efficiency when executed on mobile devices. Recent trend has been to exploit the abundant data-level parallelism found in general purpose programmable GPUs. However, for low-power mobile use cases, generic GPUs consume excessive amounts of power. This paper proposes a programmable computational imaging processor with 16-bit half-precision SIMD floating point vector processing capabilities combined with power efficiency of an exposed datapath. In comparison to traditional VLIW architectures with similar computational resources, the exposed datapath reduces the register file traffic and complexity. These and the specific optimizations enabled by the explicit programming model enable extremely good power-performance. When synthesized on a 28nm ASIC technology, the accelerator consumes 71mW of power while running a state-of-the-art denoising algorithm, and occupies only 0.2mm² of chip area. For the algorithm, energy usage per frame is 7mJ, which is 10x less than the best found GPU-based implementation.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Department of Pervasive Computing, Research area: Computer engineering, Noiseless Imaging Oy Ltd
Contributors: Multanen, J., Kultala, H., Koskela, M., Viitanen, T., Jääskeläinen, P., Takala, J., Danielyan, A., Cruz, C.
Number of pages: 6
Publication date: 2016

Host publication information

Title of host publication: 2016 IEEE Nordic Circuits and Systems Conference (NORCAS)
Publisher: IEEE
ISBN (Electronic): 978-1-5090-1095-0
ASJC Scopus subject areas: Hardware and Architecture, Signal Processing
Electronic versions:

OpenCLProgrammableExposedDatapath
DOIs:

10.1109/NORCHIP.2016.7792906
URLs:

http://urn.fi/URN:NBN:fi:tty-201702061098
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Still image/video frame lossy compression providing a desired visual quality

The problem of how to automatically provide a desired (required) visual quality in lossy compression of still images and video frames is considered in this paper. The quality can be measured based on different conventional and visual quality metrics. In this paper, we mainly employ human visual system (HVS) based metrics PSNR-HVS-M and MSSIM since both of them take into account several important peculiarities of HVS. To provide a desired visual quality with high accuracy, iterative image compression procedures are proposed and analyzed. An experimental study is performed for a large number of grayscale test images. We demonstrate that there exist several coders for which the number of iterations can be essentially decreased using a reasonable selection of the starting value and the variation interval for the parameter controlling compression (PCC). PCC values attained at the end of the iterative procedure may heavily depend upon the coder used and the complexity of the image. Similarly, the compression ratio also considerably depends on the above factors. We show that for some modern coders that take HVS into consideration it is possible to give practical recommendations on setting a fixed PCC to provide a desired visual quality in a non-iterative manner. The case when original images are corrupted by visible noise is also briefly studied.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Signal Processing, Research group: Computational Imaging-CI, National Aerospace University
Contributors: Zemliachenko, A., Lukin, V., Ponomarenko, N., Egiazarian, K., Astola, J.
Pages: 697-718
Publication date: 2016
Peer-reviewed: Yes

Publication information
Journal: Multidimensional Systems and Signal Processing
Volume: 27
Issue number: 3
ISSN (Print): 0923-6082
Ratings:

Scopus rating (2016): CiteScore 3.4 SJR 0.424 SNIP 1.109
Original language: English
ASJC Scopus subject areas: Computer Science Applications, Information Systems, Signal Processing, Software, Artificial Intelligence, Hardware and Architecture, Applied Mathematics
Keywords: Compression ratio, Lossy compression, Required quality, Visual quality metrics
DOIs:

10.1007/s11045-015-0333-8
URLs:

http://www.scopus.com/inward/record.url?scp=84930357751&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84930357751
Research output: Contribution to journal › Article › Scientific › peer-review

BM3D image denoising using heterogeneous computing platforms
Noise reduction is often performed at an early stage of the image processing path. In order to keep the processing delays small in different computing platforms, it is important that the noise reduction is performed swiftly. In this paper, the block-matching and three-dimensional filtering (BM3D) denoising algorithm is implemented on heterogeneous computing platforms using OpenCL and CUDA frameworks. To our knowledge, these implementations are the first successful open source attempts to use GPU computation for BM3D denoising. The presented GPU implementations are up to 7.5 times faster than their respective CPU implementations. At the same time, the experiments illustrate general design challenges in using massively parallel processing platforms for the calculation of complex imaging algorithms.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), Univ of Oulu, Center for Machine Vision Research
Contributors: Sarjanoja, S., Boutellier, J., Hannuksela, J.
Publication date: 28 Dec 2015

Host publication information
Title of host publication: DASIP 2015 - Proceedings of the 2015 Conference on Design and Architectures for Signal and Image Processing
Volume: 2015-December
Publisher: IEEE COMPUTER SOCIETY PRESS
Article number: 7367257
ISBN (Electronic): 9791092279108
ASJC Scopus subject areas: Computer Graphics and Computer-Aided Design, Computer Vision and Pattern Recognition, Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
Keywords: Image denoising, Mobile computing, Parallel algorithms, Parallel processing
DOIs:

10.1109/DASIP.2015.7367257
URLs:

http://www.scopus.com/inward/record.url?scp=84959887479&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84959887479
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Reconfigurable computing for future vision-capable devices
Mobile devices have been identified as promising platforms for interactive vision-based applications. However, this type of applications still pose significant challenges in terms of latency, throughput and energy-efficiency. In this context, the integration of reconfigurable architectures on mobile devices allows dynamic reconfiguration to match the computation and data flow of interactive applications, demonstrating significant performance benefits compared to general purpose architectures. This paper presents concepts laying on platform level adaptability, exploring the acceleration of vision-based interactive applications through the utilization of three reconfigurable architectures: A low-power EnCore processor with a Configurable Flow Accelerator co-processor, a hybrid reconfigurable SIMD/MIMD platform and Transport-Triggered Architecture-based processors. The architectures are evaluated and compared with current processors, analyzing their advantages and weaknesses in terms of performance and energy-efficiency when implementing highly interactive vision-based applications. The results show that the inclusion of reconfigurable platforms on mobile devices can enable the computation of several computationally heavy tasks with high performance and small energy consumption while providing

enough flexibility.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), Univ of Oulu, University of Santiago de Compostela (USC)
Contributors: López, M. B., Nieto, A., Silvén, O., Bóutellier, J., Vilariño, D. L.
Number of pages: 8
Pages: 34-41
Publication date: 22 Dec 2015

Host publication information
Title of host publication: Proceedings - 2015 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, SAMOS 2015
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 7363657
ISBN (Electronic): 9781467373111
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Modelling and Simulation
DOIs:

10.1109/SAMOS.2015.7363657
URLs:

http://www.scopus.com/inward/record.url?scp=84963704173&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84963704173
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Binomial Gaussian mixture filter
In this work, we present a novel method for approximating a normal distribution with a weighted sum of normal distributions. The approximation is used for splitting normally distributed components in a Gaussian mixture filter, such that components have smaller covariances and cause smaller linearization errors when nonlinear measurements are used for the state update. Our splitting method uses weights from the binomial distribution as component weights. The method preserves the mean and covariance of the original normal distribution, and in addition, the resulting probability density and cumulative distribution functions converge to the original normal distribution when the number of components is increased. Furthermore, an algorithm is presented to do the splitting such as to keep the linearization error below a given threshold with a minimum number of components. The accuracy of the estimate provided by the proposed method is evaluated in four simulated single-update cases and one time series tracking case. In these tests, it is found that the proposed method is more accurate than other Gaussian mixture filters found in the literature when the same number of components is used and that the proposed method is faster and more accurate than particle filters.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Automation Science and Engineering, Department of Mathematics, Research group: MAT Positioning, Research group: Positioning, Wireless Communications and Positioning (WICO)
Contributors: Raitoharju, M., Ali-Löytty, S., Piché, R.
Publication date: 2 Dec 2015
Peer-reviewed: Yes

Publication information
Journal: Eurasip Journal on Advances in Signal Processing
Volume: 2015
Issue number: 1
Article number: 36
ISSN (Print): 1687-6172
Ratings:

Scopus rating (2015): CiteScore 2.5 SJR 0.351 SNIP 0.942
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
Keywords: Estimation, Gaussian mixture filter, Nonlinear filtering
Electronic versions:

s13634-015-0221-2
DOIs:

10.1186/s13634-015-0221-2

URLs:
http://urn.fi/URN:NBN:fi:tty-201706051582
URLs:
http://www.scopus.com/inward/record.url?scp=84934283964&partnerID=8YFLogxK (Link to publication in Scopus)

Bibliographical note
ORG=ase,0.75
ORG=mat,0.25
Source: Scopus
Source ID: 84934283964
Research output: Contribution to journal › Article › Scientific › peer-review

Programming graphics processing units in the RVC-CAL dataflow language

The interest towards programming of streaming applications using dataflow models of computation has been increasing steadily in the recent years. Among the numerous dataflow formalisms, the ISO-standardized RVC-CAL dataflow language has offered a solid basis for programming tool development and research. To this date RVC-CAL programming tools have enabled transforming dataflow programs into concurrent executables for multicore processors, as well as for generating synthesizable hardware descriptions. In this paper it is shown how the RVC-CAL dataflow language can be used for programming graphics processing units (GPUs) with high efficiency. Considering the processing architectures of recent mobile and desktop computing devices, this advance is of high importance, as most consumer devices contain a graphics processing unit nowadays. To evaluate the proposed solution, the paper presents a video processing application case study. At best, the solution is shown to provide a speedup of 42× over single-threaded CPU execution.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), Dept. of Computer Science and Engineering, Univ of Oulu
Contributors: Boutellier, J., Nyländen, T.
Publication date: 2 Dec 2015

Host publication information
Title of host publication: Electronic Proceedings of the 2015 IEEE International Workshop on Signal Processing Systems, SiPS 2015
Volume: 2015-December
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 7344994
ISBN (Electronic): 9781467396042
ASJC Scopus subject areas: Electrical and Electronic Engineering, Signal Processing, Applied Mathematics, Hardware and Architecture
Keywords: Dataflow computing, design automation, parallel processing
DOIs:
10.1109/SiPS.2015.7344994
URLs:
http://www.scopus.com/inward/record.url?scp=84958191208&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84958191208
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Kalman filter with a linear state model for PDR+WLAN positioning and its application to assisting a particle filter

Indoor positioning based on wireless local area network (WLAN) signals is often enhanced using pedestrian dead reckoning (PDR) based on an inertial measurement unit. The state evolution model in PDR is usually nonlinear. We present a new linear state evolution model for PDR. In simulated-data and real-data tests of tightly coupled WLAN-PDR positioning, the positioning accuracy with this linear model is better than with the traditional models when the initial heading is not known, which is a common situation. The proposed method is computationally light and is also suitable for smoothing. Furthermore, we present modifications to WLAN positioning based on Gaussian coverage areas and show how a Kalman filter using the proposed model can be used for integrity monitoring and (re)initialization of a particle filter.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Automation Science and Engineering, Research area: Dynamic Systems, Research group: Positioning, Wireless Communications and Positioning (WICO)
Contributors: Raitoharju, M., Nurminen, H., Piché, R.

Publication date: 1 Dec 2015
Peer-reviewed: Yes

Publication information
Journal: Eurasip Journal on Advances in Signal Processing
Volume: 2015
Issue number: 1
Article number: 33
ISSN (Print): 1687-6172
Ratings:

Scopus rating (2015): CiteScore 2.5 SJR 0.351 SNIP 0.942
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
Keywords: Computational modeling, Indoor positioning, Pedestrian dead reckoning, Wireless LAN
Electronic versions:

s13634-015-0216-z
DOIs:

10.1186/s13634-015-0216-z
URLs:

http://urn.fi/URN:NBN:fi:tty-201706051578
URLs:

http://www.scopus.com/inward/record.url?scp=84928397748&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84928397748
Research output: Contribution to journal › Article › Scientific › peer-review

Haptic feedback of gaze gestures with glasses: Localization accuracy and effectiveness
Wearable devices including smart eyewear require new interaction methods between the device and the user. In this paper, we describe our work on the combined use of eye tracking for input and haptic (touch) stimulation for output with eyewear. Input with eyes can be achieved by utilizing gaze gestures which are predefined patterns of gaze movements identified as commands. The frame of the eyeglasses offers three natural contact points with the wearer's skin for haptic stimulation. The results of two user studies reported in this paper showed that stimulation moving between the contact points was easy for users to localize, and that the stimulation has potential to make the use of gaze gestures more efficient.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Augmented Human Activities (AHA), University of Tampere
Contributors: Rantala, J., Kangas, J., Isokoski, P., Akkil, D., Špakov, O., Raisamo, R.
Number of pages: 8
Pages: 855-862
Publication date: 7 Sep 2015

Host publication information
Title of host publication: UbiComp and ISWC 2015 - Proceedings of the 2015 ACM International Joint Conference on Pervasive and Ubiquitous Computing and the Proceedings of the 2015 ACM International Symposium on Wearable Computers
Publisher: Association for Computing Machinery, Inc
ISBN (Electronic): 9781450335751
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Software
Keywords: Gaze gestures, Gaze tracking, Haptic stimulation, Haptics, Pervasive computing, Smart eyewear, Smart glasses, Wearable computing
DOIs:

10.1145/2800835.2804334
URLs:

http://www.scopus.com/inward/record.url?scp=84962523895&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84962523895
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

The extended one-dimensional discrete phase retrieval problem
It has been known for decades that the iterative methods are perhaps the most popular approaches to solve the phase retrieval problem. Unfortunately the iterative methods often stagnate. This happens also in the case of the 1-D Discrete

Phase Retrieval (1-D DPhR) problem. Recently it has been shown that some requirements in the input magnitude data might be one of the reasons why the direct method cannot solve the 1-D DPhR Problem. In this work we present some difficulties that can be encountered when one has to implement the iterative method for finding a solution of 1-D DPhR problem. We shall formulate the extended form of 1-D DPhR problem. Simulations indicate the conjecture to be true.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Department of Signal Processing, Research group: Algebraic and Algorithmic Methods in Signal Processing AAMSP, Signal Processing Research Community (SPRC), FETTI, Technical University of Cluj-NapocaUniversitatea Tehnica din Cluj-Napoca
Contributors: Rusu, C., Astola, J.
Publication date: 14 Aug 2015

Host publication information
Title of host publication: 2015 International Symposium on Signals, Circuits and Systems (ISSCS)
Publisher: IEEE
ISBN (Print): 9781467374873
ASJC Scopus subject areas: Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
DOIs:

10.1109/ISSCS.2015.7204029

Bibliographical note
EXT="Rusu, Corneliu"
Source: Scopus
Source ID: 84955586971
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Exploring the Stability of Software with Time-Series Cross-Sectional Data
The stability of software is a classical topic in software engineering. This research investigates stability of software architectures in terms of an object-oriented design principle presented by Robert C. Martin. The research approach is statistical: the design principle is evaluated with a time-series cross-sectional (TSCS) regression model. The empirical sample covers a release history from the Java library Vaadin. The empirical results establish that the design principle cannot be used to characterize the library. Besides delivering this negative empirical result, the research provides the necessary methodological background that is required to understand TSCS modeling.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Managing digital industrial transformation (mDIT), University of Turku, Department of Information Technology
Contributors: Ruohonen, J., Hyrynsalmi, S., Leppänen, V.
Number of pages: 7
Pages: 41-47
Publication date: 31 Jul 2015

Host publication information
Title of host publication: Proceedings - 2nd International Workshop on Software Architecture and Metrics, SAM 2015
Publisher: Institute of Electrical and Electronics Engineers Inc.
ISBN (Electronic): 9781479919345
ASJC Scopus subject areas: Hardware and Architecture, Software
Keywords: panel data, software metrics, software stability
DOIs:

10.1109/SAM.2015.13
Source: Scopus
Source ID: 84946921946
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Gathering useful programming data; Analysis and insights from real-time collaborative editing
Traditionally, collaborative coding has been practiced in open source communities where cooperation has mostly taken place on a coordination level. Nowadays, web technology is sufficiently advanced to enable collaborative coding in real-time as group work, which eases communication in software development. In this paper this phenomenon has been studied from a knowledge transfer and learning perspective. With the aid of two different example cases (code camps), we have examined the possibilities and challenges in learning during real-time group work. Additionally, we have evaluated the effect of the structure of log data created during software development. The research frame for this study is the utilization of log data visualization in evaluating group work and further improvement of the visualization in order to support

software development.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Pori Department, Research group: Software Engineering and Intelligent Systems, Department of Pervasive Computing, Research area: Software engineering, Managing digital industrial transformation (mDIT)
Contributors: Rantala, M., Soini, J., Kilamo, T.
Number of pages: 6
Pages: 229-234
Publication date: 15 Jul 2015

Host publication information
Title of host publication: 2015 38th International Convention on Information and Communication Technology, Electronics and Microelectronics, MIPRO 2015 - Proceedings
Publisher: The Institute of Electrical and Electronics Engineers, Inc.
Article number: 7160270
ISBN (Print): 9789532330854
ASJC Scopus subject areas: Computer Networks and Communications, Computer Science Applications, Hardware and Architecture, Electrical and Electronic Engineering
DOIs:

10.1109/MIPRO.2015.7160270
URLs:

http://www.scopus.com/inward/record.url?scp=84946129499&partnerID=8YFLogxK (Link to publication in Scopus)

Bibliographical note
ORG=pla,0.7
ORG=tie,0.3
Source: Scopus
Source ID: 84946129499
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

LTE indoor MIMO performances field measurements
Long-term evolution (LTE) and multiple input multiple output (MIMO) have earned reputations to be a cutting-edge technology, which can boost significantly wireless communication performances. The paper aims at providing LTE MIMO performances in indoor environments and, therefore, guidelines for network operators can be proposed. Medium access control throughput (MAC TP) and some system parameters in LTE network that are linked with MAC TP, such as Channel Quality Indicator (CQI), Modulation and Coding Scheme (MCS), Ranking Indicator (RI), Pre-coding Matrix Indicator (PMI), as well as MIMO utilization, are analysed. Effects of indoor propagation, Line of Sight (LoS), No-line of Sight (NLoS), strong and weak signal levels on Signal to Noise Radio (SNR) strength and MIMO utilization are clarified. In this paper, the performances of MIMO transmission mode over transmit diversity (TxDiv, Multiple Input-Single Output-MISO) and single antenna (Single Input Multiple Output-SIMO) modes are also analyzed and compared at overall manner and at channel-specific manners.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Tampere University of Technology, Department of Electronics and Communications Engineering, Department of Electronics and Communication Engineering, Electrical and Electronics Engineering Department, Department of Electric-Electronics Engineering, Ho Chi Minh City University of Technology, Industrial University of Ho Chi Minh City, Ho Chi Minh City University of Food Industry
Contributors: Nguyen-Thanh, D., Le-Tien, T., Bui-Thu, C., Le-Thanh, T.
Number of pages: 6
Pages: 84-89
Publication date: 17 Feb 2015

Host publication information
Title of host publication: International Conference on Advanced Technologies for Communications
Publisher: IEEE
ISBN (Print): 9781479969555
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Software
Keywords: Field measurements, LTE, MIMO, MISO, OFDM, Rayleigh channel, Rician channel
DOIs:

10.1109/ATC.2014.7043361

Bibliographical note
INT=elt,"Nguyen-Thanh, Duc"
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Social behavior in bacterial nanonetworks: Challenges and opportunities
Molecular communication holds the promise to enable communication between nanomachines with a view to increasing their functionalities and opening up new possible applications. Due to some of the biological properties, bacteria have been proposed as a possible information carrier for molecular communication, and the corresponding communication networks are known as bacterial nanonetworks. The biological properties include the ability for bacteria to mobilize between locations and carry the information encoded in deoxyribonucleic acid molecules. However, similar to most organisms, bacteria have complex social properties that govern their colony. These social characteristics enable the bacteria to evolve through various fluctuating environmental conditions by utilizing cooperative and non-cooperative behaviors. This article provides an overview of the different types of cooperative and non-cooperative social behavior of bacteria. The challenges (due to non-cooperation) and the opportunities (due to cooperation) these behaviors can bring to the reliability of communication in bacterial nanonetworks are also discussed. Finally, simulation results on the impact of bacterial cooperative social behavior on the end-to-end reliability of a single-link bacterial nanonetwork are presented. The article concludes by highlighting the potential future research opportunities in this emerging field.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Electronics and Communications Engineering, Research group: Emerging Technologies for Nano-Bio-Info-Cogno, Wireless Communications and Positioning (WICO), University of Manitoba
Contributors: Hasan, M., Hossain, E., Balasubramaniam, S., Koucheryavy, Y.
Number of pages: 9
Pages: 26-34
Publication date: 1 Jan 2015
Peer-reviewed: Yes

Publication information
Journal: IEEE Network
Volume: 29
Issue number: 1
Article number: 7018200
ISSN (Print): 0890-8044
Ratings:

Scopus rating (2015): CiteScore 7.9 SJR 1.107 SNIP 2.903
Original language: English
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Information Systems, Software
DOIs:

10.1109/MNET.2015.7018200
Source: Scopus
Source ID: 84921862364
Research output: Contribution to journal › Article › Scientific › peer-review

Towards Trusted eHealth Services in the Cloud
As adoption of eHealth solutions advances, new computing paradigms - such as cloud computing - bring the potential to improve efficiency in managing medical health records and help reduce costs. However, these opportunities introduce new security risks which can not be ignored. In this paper, we present a forward-looking design for a privacy-preserving eHealth cloud system. The proposed solution, is based on a Symmetric Searchable Encryption scheme that allows patients of an electronic healthcare system to securely store encrypted versions of their medical data and search directly on them without having to decrypt them first. As a result, the proposed protocol offers better protection than the current available solutions and paves the way for the next generation of eHealth systems.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Security Lab, SICS, Karlsruhe Institute of Technology, Insitute for Technical Physics, Germany
Contributors: Michalas, A., Dowsley, R.
Number of pages: 6
Pages: 618-623
Publication date: 1 Jan 2015

Host publication information

Title of host publication: Proceedings - 2015 IEEE/ACM 8th International Conference on Utility and Cloud Computing, UCC 2015
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 7431484
ISBN (Electronic): 9780769556970
ASJC Scopus subject areas: Hardware and Architecture, Computer Networks and Communications
Keywords: Cloud Computing, eHealth, EHR Protection, Searchable Encryption, Security, Storage Protection
DOIs:

10.1109/UCC.2015.108
Source: Scopus
Source ID: 84965052600
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Digital correction of frequency response mismatches in 2-channel time-interleaved ADCs using adaptive I/Q signal processing

A novel adaptive compensation architecture for the frequency response mismatch of 2-channel time-interleaved ADC (TI-ADC) is proposed for developing high-performance self-adaptive systems. The proposed approach overcomes the existing methods in the sense that the TI-ADC mismatch identification can be performed without allocating a region where only the TI-ADC mismatch spurs are present. This is accomplished via mapping the TI-ADC problem into an I/Q mismatch problem which allows deploying complex statistical signal processing. As proof of concept, the compensation architecture is demonstrated and tested on a 16-bit TI-ADC measured hardware data.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Wireless Communications and Positioning (WICO), Department of Electronics and Communications Engineering, Research group: Wireless Communications and Positioning, Airbus Defense and Space
Contributors: Singh, S., Valkama, M., Epp, M., Anttila, L., Schlecker, W., Ingber, E.
Number of pages: 13
Pages: 543-555
Publication date: 2015
Peer-reviewed: Yes

Publication information

Journal: Analog Integrated Circuits and Signal Processing
Volume: 82
Issue number: 3
ISSN (Print): 0925-1030
Ratings:

Scopus rating (2015): CiteScore 1.2 SJR 0.197 SNIP 0.42
Original language: English
ASJC Scopus subject areas: Surfaces, Coatings and Films, Hardware and Architecture, Signal Processing
Keywords: Circularity, Complex I/Q signal processing, Digitally assisted analog (DASA), Frequency response mismatch identification, Time-interleaved ADC
DOIs:

10.1007/s10470-014-0476-9
Source: Scopus
Source ID: 84925535772
Research output: Contribution to journal › Article › Scientific › peer-review

Dynamic text presentation in print interpreting - An eye movement study of reading behaviour

Print interpreting supports people with a hearing disability by giving them access to spoken language. In print interpreting, the interpreter types the spoken text in real time for the hard-of-hearing client to read. This results in dynamic text presentation. An eye movement study was conducted to compare two types of dynamic text presentation formats in print interpreting: letter-by-letter and word-by-word. Gaze path analysis with 20 hearing participants showed different types of reading behaviour during reading of two pieces of text in these two presentation formats. Our analysis revealed that the text presentation format has a significant effect on reading behaviour. Rereading and regressions occurred significantly more often with the word-by-word format than with the letter-by-letter format. We also found a significant difference between the number of regressions starting at the words that end a sentence and that of regressions starting at all other words. The frequency of rereading was significantly higher for incorrectly typed or abbreviated words than for the other words. Analysis of the post-test questionnaire found almost equal acceptance of the word-by-word and letter-by-letter formats by the participants. A follow-up study with 18 hard-of-hearing participants showed a similar trend in results. The findings of this study highlight the importance of developing print interpreting tools that allow the interpreter and the client to choose the options that best facilitate the communication. They also bring up the need to develop new eye movement

metrics for analysing the reading of dynamic text, and provide first results on a new dynamic presentation context.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Augmented Human Activities (AHA), School of Management (JKK)
Contributors: Sharmin, S., Špakov, O., Räihä, K. J.
Number of pages: 14
Pages: 17-30
Publication date: 2015
Peer-reviewed: Yes

Publication information
Journal: International Journal of Human-Computer Studies
Volume: 78
ISSN (Print): 1071-5819
Ratings:

Scopus rating (2015): CiteScore 4.4 SJR 0.666 SNIP 1.739
Original language: English
ASJC Scopus subject areas: Human Factors and Ergonomics, Software, Education, Engineering(all), Human-Computer Interaction, Hardware and Architecture
Keywords: Dynamic text presentation, Eye movements, Print interpreting, Reading, Regressions
DOIs:

10.1016/j.ijhcs.2015.01.010
URLs:

http://www.scopus.com/inward/record.url?scp=84923618729&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84923618729
Research output: Contribution to journal › Article › Scientific › peer-review

Techno-Economical Comparison of Dynamic DAS and Legacy Macrocellular Densification: Capacity and Cost-Efficiency Analysis of Alternative Deployment Solutions for Outdoor Service Provisioning
In order to support anywhere and anytime services of Beyond 4G networks, new deployment solutions will be required that can cost-effectively address the capacity demand of the future and also offer consistently high bit rates and decent quality of service throughout the network coverage area. In this article we look into an advanced outdoor distributed antenna system (DAS) concept, dynamic DAS, that offers on-demand outdoor capacity in urban areas by dynamically configuring the remote antenna units to either act as individual small cells or distributed nodes of a common central cell. The performance of the investigated DAS solution is evaluated and compared with legacy macrocellular deployment in a dense urban environment. Furthermore, the analysis covers the performance evaluation, mainly from an outdoor perspective. The obtained results indicate superior performance of dynamic DAS concept in terms of coverage and SINR, network capacity and cost-efficiency as compared to legacy macrocellular network deployments.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Department of Electronics and Communications Engineering, Research group: Wireless Communications and Positioning, Wireless Communications and Positioning (WICO), Elisa Corporation
Contributors: Yunas, S. F., Valkama, M., Niemelä, J.
Pages: 312-326
Publication date: 2015
Peer-reviewed: Yes

Publication information
Journal: International Journal of Wireless Information Networks
Volume: 22
Issue number: 4
ISSN (Print): 1068-9605
Ratings:

Scopus rating (2015): CiteScore 2 SJR 0.207 SNIP 1.271
Original language: English
ASJC Scopus subject areas: Electrical and Electronic Engineering, Computer Networks and Communications, Hardware and Architecture
Keywords: Capacity efficiency, Cost efficiency, Dynamic DAS, Macrocellular densification, Outdoor service provisioning, Techno-economics
DOIs:

10.1007/s10776-015-0286-8

Bibliographical note
EXT="Niemelä, Jarno"
Research output: Contribution to journal › Article › Scientific › peer-review

A multi-coil wireless power transfer system utilizing dynamic matching for in-vivo and biomedical applications
Typically, single coil wireless power transfer (WPT) systems which are potential utilized for in-vivo device powering are limited by the total available power at the antenna. To overcome this limitation, a multi-coil system is presented which can greatly increase the power available to the receiver coil by as much as 80% while still remaining within the regulatory limits for total available power from an individual antenna. The effects of matching based on coil separation are presented which demonstrate the dependence of the self-resonant frequency of the WPT system, and a dynamic matching solution is proposed which allows for maximum power transfer efficiency independent of coil separation or changes in body impedance.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Sensing Systems for Wireless Medicine (MediSense), Georgia Institute of Technology
Contributors: Bito, J., Cook, B. S., Tentzeris, M. M.
Number of pages: 3
Pages: 680-682
Publication date: 25 Mar 2014

Host publication information
Title of host publication: 2014 Asia-Pacific Microwave Conference Proceedings, APMC 2014
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 7067912
ISBN (Electronic): 9784902339314
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Electrical and Electronic Engineering
Keywords: Biomedical systems, Dynamic matching, Implantable systems, In-vivo electronics, Wireless power transfer
URLs:

http://www.scopus.com/inward/record.url?scp=84942911542&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84942911542
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

BIM based schedule control for precast concrete supply chain
Development of the schedule control of precast concrete supply chain has been studied. Main idea was to use BIM model created by structural engineer as a user-interface for schedule control, for saving different status information of the real-time schedule situation of the propagation of structural design, element manufacture, delivery and site erection directly to the BIM model by using a cloud-based networked service. Some of the missing software applications were programmed by the software companies participated in the project. Experiments were done in a real construction project in Finland, where the information from design, prefabrication, delivery and erection phases was synchronized between the stakeholders by using the cloud service. The most important observations and results are introduced and analyzed. A future model for intelligent BIM based schedule control concept is concluded.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Life Cycle Effectiveness of the Built Environment (LCE@BE), Skanska Oy, Construction Technology Research Center, University of Oulu
Contributors: Nissilä, J., Heikkilä, R., Romo, I., Malaska, M., Aho, T.
Number of pages: 5
Pages: 667-671
Publication date: 2014

Host publication information
Title of host publication: 31st International Symposium on Automation and Robotics in Construction and Mining, ISARC 2014 - Proceedings
Publisher: University of Technology Sydney
ISBN (Print): 9780646597119
ASJC Scopus subject areas: Artificial Intelligence, Hardware and Architecture, Civil and Structural Engineering, Building and Construction

Keywords: BIM, Precast concrete, Schedule control, Supply chain
URLs:
http://www.scopus.com/inward/record.url?scp=84912527773&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84912527773
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Implementation of a high-throughput low-latency polyphase channelizer on GPUs Design and Architectures for Signal and Image Processing 2008

A channelizer is used to separate users or channels in communication systems. A polyphase channelizer is a type of channelizer that uses polyphase filtering to filter, downsample, and downconvert simultaneously. With graphics processing unit (GPU) technology, we propose a novel GPU-based polyphase channelizer architecture that delivers high throughput. This architecture has advantages of providing reduced complexity and optimized parallel processing of many channels, while being configurable via software. This makes our approach and implementation particularly attractive for using GPUs as DSP accelerators for communication systems.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), University of Maryland, Department of Electrical and Computer Engineering
Contributors: Kim, S. C., Bhattacharyya, S. S.
Publication date: 2014
Peer-reviewed: Yes

Publication information

Journal: Eurasip Journal on Advances in Signal Processing
Volume: 2014
Issue number: 1
ISSN (Print): 1687-6172
Ratings:
Scopus rating (2014): CiteScore 2.2 SJR 0.286 SNIP 0.937
Original language: English
ASJC Scopus subject areas: Signal Processing, Hardware and Architecture, Electrical and Electronic Engineering
Keywords: DSP accelerator, GPU front-end receiver, GPU-based radio, Polyphase channelizer, Polyphase filter
DOIs:
10.1186/1687-6180-2014-141
URLs:
http://www.scopus.com/inward/record.url?scp=84907545943&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84907545943
Research output: Contribution to journal › Article › Scientific › peer-review

Federation lifecycle management incorporating coordination of bio-inspired self-management processes

As it has evolved, the Internet has had to support a broadening range of networking technologies, business models and user interaction modes. Researchers and industry practitioners have realised that this trend necessitates a fundamental rethinking of approaches to network and service management. This has spurred significant research efforts towards developing autonomic network management solutions incorporating distributed self-management processes inspired by biological systems. Whilst significant advances have been made, most solutions focus on management of single network domains and the optimisation of specific management or control processes therein. In this paper we argue that a networking infrastructure providing a myriad of loosely coupled services must inherently support federation of network domains and facilitate coordination of the operation of various management processes for mutual benefit. To this end, we outline a framework for federated management that facilitates the coordination of the behaviour of bio-inspired management processes. Using a case study relating to distribution of IPTV content, we describe how Federal Relationship Managers realising our layered model of management federations can communicate to manage service provision across multiple application/storage/ network providers. We outline an illustrative example in which storage providers are dynamically added to a federation to accommodate demand spikes, with appropriate content being migrated to those providers servers under control of a bio-inspired replication process.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Wireless Communications and Positioning (WICO), Waterford Institute of Technology, Trinity College Dublin

Contributors: Meskill, B., Balasubramaniam, S., Brennan, R., Feeney, K., Jennings, B.
Number of pages: 27
Pages: 650-676
Publication date: Dec 2013
Peer-reviewed: Yes

Publication information
Journal: JOURNAL OF NETWORK AND SYSTEMS MANAGEMENT
Volume: 21
Issue number: 4
ISSN (Print): 1064-7570
Ratings:

Scopus rating (2013): CiteScore 1.5 SJR 0.237 SNIP 0.651
Original language: English
ASJC Scopus subject areas: Information Systems, Hardware and Architecture, Computer Networks and Communications, Strategy and Management
Keywords: Bio-inspired processes, Federation, IPTV content distribution, Network management
DOIs:

10.1007/s10922-013-9263-7
URLs:

http://www.scopus.com/inward/record.url?scp=84885309455&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84885309455
Research output: Contribution to journal › Article › Scientific › peer-review

Towards generic embedded multiprocessing for RVC-CAL dataflow programs
Dataflow languages enable describing signal processing applications in a platform independent fashion, which makes them attractive in today's multiprocessing era. RVC-CAL is a dynamic dataflow language that enables describing complex data-dependent programs such as video decoders. To this date, design automation toolchains for RVC-CAL have enabled creating workstation software, dedicated hardware and embedded application specific multiprocessor implementations out of RVC-CAL programs. However, no solution has been presented for executing RVC-CAL applications on generic embedded multiprocessing platforms. This paper presents a dataflow-based multiprocessor communication model, an architecture prototype that uses it and an automated toolchain for instantiating such a platform and the software for it. The complexity of the platform increases linearly as the number of processors is increased. The experiments in this paper use several instances of the proposed platform, with different numbers of processors. An MPEG-4 video decoder is mapped to the platform and executed on it. Benchmarks are performed on an FPGA board.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), Dept. of Computer Science and Engineering, Univ of Oulu
Contributors: Boutellier, J., Silvén, O.
Number of pages: 6
Pages: 137-142
Publication date: Nov 2013
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
Volume: 73
Issue number: 2
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2013): CiteScore 2.1 SJR 0.254 SNIP 0.866
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Information Systems, Signal Processing, Theoretical Computer Science, Control and Systems Engineering, Modelling and Simulation
Keywords: Data flow computing, Design automation, Multiprocessor interconnection
DOIs:

10.1007/s11265-013-0737-3
URLs:

http://www.scopus.com/inward/record.url?scp=84881476500&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus

Source ID: 84881476500
Research output: Contribution to journal › Article › Scientific › peer-review

High-performance and low-energy buffer mapping method for multiprocessor DSP systems

When implementing digital signal processing (DSP) applications onto multiprocessor systems, one significant problem in the viewpoints of performance is the memory wall. In this paper, to help alleviate the memory wall problem, we propose a novel, high-performance buffer mapping policy for SDF-represented DSP applications on bus-based multiprocessor systems that support the shared-memory programming model. The proposed policy exploits the bank concurrency of the DRAM main memory system according to the analysis of hierarchical parallelism. Energy consumption is also a critical parameter, especially in battery-based embedded computing systems. In this paper, we apply a synchronization back-off scheme on the top of the proposed high-performance buffer mapping policy to reduce energy consumption. The energy saving is attained by minimizing the number of non-essential synchronization transactions. We measure throughput and energy consumption on both synthetic and real benchmarks. The simulation results show that the proposed buffer mapping policy is very useful in terms of performance, especially in memory-intensive applications where the total execution time of computational tasks is relatively small compared to that of memory operations. In addition, the proposed synchronization back-off scheme provides a reduction in the number of synchronization transactions without degrading performance, which results in system energy saving.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), Georgia Institute of Technology, Department of ECE and Institute for Advanced Computer Studies, University of Maryland
Contributors: Lee, D., Wolf, M., Bhattacharyya, S. S.
Publication date: Mar 2013
Peer-reviewed: Yes

Publication information

Journal: ACM Transactions on Embedded Computing Systems
Volume: 12
Issue number: 3
Article number: 82
ISSN (Print): 1539-9087
Ratings:

Scopus rating (2013): CiteScore 1.7 SJR 0.307 SNIP 0.982
Original language: English
ASJC Scopus subject areas: Software, Hardware and Architecture
Keywords: Bank concurrency, DRAM main memory systems, Multiprocessor DSP systems, SDF
DOIs:

10.1145/2442116.2442132
URLs:

http://www.scopus.com/inward/record.url?scp=84878495064&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84878495064
Research output: Contribution to journal › Article › Scientific › peer-review

Integration of dataflow-based heterogeneous multiprocessor scheduling techniques in GNU radio

As the variety of off-the-shelf processors expands, traditional implementation methods of systems for digital signal processing and communication are no longer adequate to achieve design objectives in a timely manner. There is a necessity for designers to easily track the changes in computing platforms, and apply them efficiently while reusing legacy code and optimized libraries that target specialized features in single processing units. In this context, we propose an integration workflow to schedule and implement Software Defined Radio (SDR) protocols that are developed using the GNU Radio environment on heterogeneous multiprocessor platforms. We show how to utilize Single Instruction Multiple Data (SIMD) units provided in Graphics Processing Units (GPUs) along with vector accelerators implemented in General Purpose Processors (GPPs). We augment a popular SDR framework (i.e, GNU Radio) with a library that seamlessly allows offloading of algorithm kernels mapped to the GPU without changing the original protocol description. Experimental results show how our approach can be used to efficiently explore design spaces for SDR system implementation, and examine the overhead of the integrated backend (software component) library.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), University of Maryland, Department of Electrical and Computer Engineering, Virginia Tech, Laboratory for Telecommunications Sciences

Contributors: Zaki, G. F., Plishker, W., Bhattacharyya, S. S., Clancy, C., Kuykendall, J.
Number of pages: 15
Pages: 177-191
Publication date: Feb 2013
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
Volume: 70
Issue number: 2
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2013): CiteScore 2.1 SJR 0.254 SNIP 0.866
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Design methodology, GNU Radio, Graphic processor unit, Multiprocessor scheduling, Software defined radio
DOIs:

10.1007/s11265-012-0696-0
URLs:

http://www.scopus.com/inward/record.url?scp=84892800816&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84892800816
Research output: Contribution to journal › Article › Scientific › peer-review

An efficient GPU implementation of an arbitrary resampling polyphase channelizer
A channelizer is a part of a receiver front-end subsystem, commonly found in various communication systems, that separates different users or channels. A modern channelizer uses advantages of polyphase filter banks to process multiple channels at the same time, allowing down conversion, downsampling, and filtering all at the same time. However, due to limitations imposed by the structure and requirements of channelizers, their usage is limited and poses significant challenges due to inflexibility using conventional implementation techniques, which are intensively hardware-based. However, with advances in graphics processing unit (GPU) technology, we now have the potential to deliver high computational throughput along with the flexibility of software-based implementation. In this paper, we demonstrate how this potential can be exploited by presenting a novel GPU-based channelizer implementation. Our implementation incorporates methods for eliminating complex buffer managements and performing arbitrary resampling on all channels simultaneously. We also introduce the notion of simultaneously processing many channels as a high data rate parallel receiver system using blocks of threads in the GPU. The multi-channel, flexible, high-throughput, and arbitrary resampling characteristics of our GPU-based channelizer make it attractive for a variety of communication receiver applications.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), University of Maryland, Department of Electrical and Computer Engineering
Contributors: Kim, S. C., Plishker, W. L., Bhattacharyya, S. S.
Number of pages: 8
Pages: 231-238
Publication date: 2013

Host publication information
Title of host publication: DASIP 2013 - Proceedings of the 2013 Conference on Design and Architectures for Signal and Image Processing
Article number: 6661548
ISBN (Print): 9791092279016
ASJC Scopus subject areas: Computer Graphics and Computer-Aided Design, Computer Vision and Pattern Recognition, Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
Keywords: Arbitrary resampling, DSP accelerator, Front-end receiver, Polyphase channelizer, Sample rate conversion
URLs:

http://www.scopus.com/inward/record.url?scp=84892642738&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84892642738
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

An IPv6-enabled wireless shoe-mounted platform for health-monitoring

An innovative wearable, partially self-powered, health monitoring and indoor localization shoe-mounted sensor module is presented. The system's novel shoe sole serves the double role of (i) medical-grade temperature probe for human body monitoring and (ii) renewable energy scavenger, which transforms the human motion to electrical energy. Mounted on the shoe is also an NFC reader for proximity-based localization purposes. An Adidas™-logo-shaped dual-band communication antenna is fabricated that exhibits great performance despite the close proximity to the high lossy human body. The proposed platform can be extended to other sensors applications, for example by embedding into the sole normal and/or shear force sensors in order to monitor the sport performances of the athletes as well as to improve the rehabilitation techniques.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Sensing Systems for Wireless Medicine (MediSense), University of Perugia, Georgia Institute of Technology
Contributors: Mariotti, C., Lakafosis, V., Tentzeris, M. M., Roselli, L.
Number of pages: 3
Pages: 46-48
Publication date: 2013

Host publication information

Title of host publication: WiSNet 2013 - Proceedings: 2013 IEEE Topical Conference on Wireless Sensors and Sensor Networks - 2013 IEEE Radio and Wireless Week, RWW 2013
Article number: 6488629
ISBN (Print): 9781467329309
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture
Keywords: dual-band antenna, health monitoring, NFC, RFID, unobtrusive electronics, wearable electronics, WSN
DOIs:

10.1109/WiSNet.2013.6488629
URLs:

http://www.scopus.com/inward/record.url?scp=84875995118&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84875995118
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Applying the adaptive hybrid flow-Shop scheduling method to schedule a 3GPP LTE physical layer algorithm onto many-core digital signal processors

Currently, Multicore Digital Signal Processor (DSP) platforms are commonly used in telecommunications baseband processing. In the next few years, high performance DSPs are likely to combine many more DSP cores for signal processing with some General-Purpose Processor (GPP) cores for application control. As the number of cores increases in new DSP platform designs, scheduling of applications is becoming a complex operation. Meanwhile, the variability of the scheduled applications also tends to increase as applications become more sophisticated. Such variations require runtime adaptivity of application scheduling. This paper extends the previous work on adaptive scheduling by using the Hybrid Flow-Shop (HFS) scheduling method, which enables the device architecture to be modeled as a pipeline of Processing Elements (PEs) with multiple alternate PEs for each pipeline stage. HFS scheduling is applied to the scheduling of 3rd Generation Partnership Project (3GPP) Long Term Evolution (LTE) telecommunication standard Uplink Physical Layer data processing (PUSCH). The experiments, conducted on an ARM Cortex-A9 GPP, show that an HFS scheduling algorithm has an overhead that increases very slowly with the number of PEs. This makes the method suitable for executing the adaptive scheduling in less than 1 ms for the 501 actors of a LTE PUSCH dataflow description executed on a 256-core architecture.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), UBL, Univ of Oulu, Texas Instruments France S.A
Contributors: Heulot, J., Boutellier, J., Pelcat, M., Nezan, J. F., Aridhi, S.
Number of pages: 7
Pages: 123-129
Publication date: 2013

Host publication information

Title of host publication: Proceedings of the 2013 NASA/ESA Conference on Adaptive Hardware and Systems, AHS 2013
Article number: 6604235
ISBN (Print): 9781467363839
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering

DOIs:
10.1109/AHS.2013.6604235
URLs:
http://www.scopus.com/inward/record.url?scp=84885396420&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84885396420
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Automatic hierarchical discovery of quasi-static schedules of RVC-CAL dataflow programs

RVC-CAL is an actor-based dataflow language that enables concurrent, modular and portable description of signal processing algorithms. RVC-CAL programs can be compiled to implementation languages such as C/C++ and VHDL for producing software or hardware implementations. This paper presents a methodology for automatic discovery of piecewise-deterministic (quasi-static) execution schedules for RVC-CAL program software implementations. Quasi-static scheduling moves computational burden from the implementable run-time system to design-time compilation and thus enables making signal processing systems more efficient. The presented methodology divides the RVC-CAL program into segments and hierarchically detects quasi-static behavior from each segment: first at the level of actors and later at the level of the whole segment. Finally, a code generator creates a quasi-statically scheduled version of the program. The impact of segment based quasi-static scheduling is demonstrated by applying the methodology to several RVC-CAL programs that execute up to 58 % faster after applying the presented methodology.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), Dept. of Computer Science and Engineering, Univ of Oulu, UBL
Contributors: Boutellier, J., Raulet, M., Silvén, O.
Number of pages: 6
Pages: 35-40
Publication date: 2013
Peer-reviewed: Yes

Publication information

Journal: Journal of Signal Processing Systems
Volume: 71
Issue number: 1
ISSN (Print): 1939-8018
Ratings:
Scopus rating (2013): CiteScore 2.1 SJR 0.254 SNIP 0.866
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Information Systems, Signal Processing, Theoretical Computer Science, Control and Systems Engineering, Modelling and Simulation
Keywords: Dataflow analysis, Scheduling, Signal processing
DOIs:
10.1007/s11265-012-0676-4
URLs:
http://www.scopus.com/inward/record.url?scp=84873689972&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84873689972
Research output: Contribution to journal › Article › Scientific › peer-review

Design space exploration and implementation of RVC-CAL applications using the TURNUS framework

While research on the design of heterogeneous concurrent systems has a long and rich history, a unified design methodology and tool support has not emerged so far, and thus the creation of such systems remains a difficult, time-consuming and error-prone process. The absence of principled support for system evaluation and optimization at high abstraction levels makes the quality of the resulting implementation highly dependent on the experience or prejudices of the designer. In this work we present TURNUS, a unified dataflow design space exploration framework for heterogeneous parallel systems. It provides high-level modelling and simulation methods and tools for system level performances estimation and optimization. TURNUS represents the outcome of several years of research in the area of co-design exploration for multimedia stream applications. During the presentation, it will be demonstrated how the initial high-level abstraction of the design facilitates the use of different analysis and optimization heuristics. These guide the designer during validation and optimization stages without requiring low-level implementations of parts of the application. Our framework currently yields exploration and optimization results in terms of algorithmic optimization, rapid performance estimation, application throughput, buffer size dimensioning, and power optimization.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), CRPP, Lund University, Dept. of Computer Science and Engineering, Univ of Oulu
Contributors: Casale-Brunet, S., Bezati, E., Alberti, C., Roquier, G., Mattavelli, M., Janneck, J. W., Boutellier, J.
Number of pages: 2
Pages: 341-342
Publication date: 2013

Host publication information
Title of host publication: DASIP 2013 - Proceedings of the 2013 Conference on Design and Architectures for Signal and Image Processing
Article number: 6661566
ISBN (Print): 9791092279016
ASJC Scopus subject areas: Computer Graphics and Computer-Aided Design, Computer Vision and Pattern Recognition, Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
Keywords: Co-exploration, Dataflow, Design space
URLs:

http://www.scopus.com/inward/record.url?scp=84892650917&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84892650917
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Guest editorial

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Research group: System-on-Chip for GNSS, Wireless Communications and Cyber-Physical Embedded Computing, Department of Electronics and Communications Engineering
Contributors: Ellervee, P., Nurmi, J.
Number of pages: 2
Pages: 430-431
Publication date: 2013
Peer-reviewed: Yes

Publication information
Journal: Microprocessors and Microsystems
Volume: 37
Issue number: 4-5
ISSN (Print): 0141-9331
Ratings:

Scopus rating (2013): CiteScore 1.6 SJR 0.225 SNIP 1.194
Original language: English
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Software, Artificial Intelligence
DOIs:

10.1016/j.micpro.2013.05.002
Source: Scopus
Source ID: 84878614529
Research output: Contribution to journal › Article › Scientific › peer-review

High-performance programs by source-level merging of RVC-CAL dataflow actors
RVC-CAL is a dataflow language that has acquired an ecosystem of sophisticated design tools. Previous works have shown that RVC-CAL-based applications can automatically be deployed to multiprocessor platforms, as well as hardware descriptions with high efficiency. However, as RVC-CAL is a concurrent language, code generation for a single processor core requires careful application analysis and scheduling. Although much work has been done in this area, to this date no publication has reported that programs generated from RVC-CAL could rival handwritten programs on single-core processors. This paper proposes performance optimization of RVCCAL applications by actor merging at source code level. The proposed methodology is demonstrated with an IEEE 802.15.4 (ZigBee) transmitter case study. The transmitter baseband software, previously written in C, is rewritten in RVC-CAL and optimized with the proposed methodology. Experiments show that on a VLIW-flavored processor the RVC-CAL-based program achieves the performance of manually written software.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), Dept. of Computer Science and Engineering, Univ of Oulu, Abo Akad Univ, Abo Akademi University, Dept Phys
Contributors: Boutellier, J., Ghazi, A., Silvén, O., Ersfolk, J.
Number of pages: 6
Pages: 360-365
Publication date: 2013

Host publication information
Title of host publication: 2013 IEEE Workshop on Signal Processing Systems, SiPS 2013
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 6674533
ISBN (Print): 9781467362382
ASJC Scopus subject areas: Electrical and Electronic Engineering, Signal Processing, Applied Mathematics, Hardware and Architecture
Keywords: Dataflow computing, Design automation, Signal processing
URLs:

http://www.scopus.com/inward/record.url?scp=84896457580&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84896457580
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Parameterized core functional dataflow graphs and their application to design and implementation of wireless communication systems
Due to the increased complexity of dynamics in modern DSP applications, dataflow-based design methodologies require significant enhancements in modeling and scheduling techniques to provide for efficient and flexible handling of dynamic behavior. In this paper, we address this problem through a new framework that is based on integrating two complementary modeling techniques, core functional dataflow (CFDF) and parameterized synchronous dataflow (PSDF). We apply, in a systematically integrated way, the structured mode-based dynamic dataflow modeling capability of CFDF together with the features of PSDF for dynamic parameter reconfiguration and quasi-static scheduling. We refer to this integrated methodology for mode - and dynamic-parameter - based modeling and scheduling as core functional parameterized synchronous dataflow (CF-PSDF). Through a wireless communication case study involving MIMO detection, we demonstrate the utility of design and implementation using CF-PSDF graphs. Experimental results on this case study demonstrate the efficiency and flexibility of our proposed new CF-PSDF based design methodology.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), University of Maryland
Contributors: Wang, L. H., Shen, C. C., Bhattacharyya, S. S.
Number of pages: 6
Pages: 1-6
Publication date: 2013

Host publication information
Title of host publication: 2013 IEEE Workshop on Signal Processing Systems, SiPS 2013
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 6674471
ISBN (Print): 9781467362382
ASJC Scopus subject areas: Electrical and Electronic Engineering, Signal Processing, Applied Mathematics, Hardware and Architecture
Keywords: Dataflow graph, Dynamic scheduling, MIMO detector, Parameterized modeling
URLs:

http://www.scopus.com/inward/record.url?scp=84896476923&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84896476923
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Parameterized scheduling of topological patterns in signal processing dataflow graphs
In recent work, a graphical modeling construct called "topological patterns" has been shown to enable concise representation and direct analysis of repetitive dataflow graph sub-structures in the context of design methods and tools for digital signal processing systems (Sane et al. 2010). In this paper, we present a formal design method for specifying topological patterns and deriving parameterized schedules from such patterns based on a novel schedule model called

the scalable schedule tree. The approach represents an important class of parameterized schedule structures in a form that is intuitive for representation and efficient for code generation. Through application case studies involving image processing and wireless communications, we demonstrate our methods for topological pattern representation, scalable schedule tree derivation, and associated dataflow graph code generation.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), University of Maryland, Department of Electrical and Computer Engineering
Contributors: Wang, L. H., Shen, C. C., Wu, S., Bhattacharyya, S. S.
Number of pages: 12
Pages: 275-286
Publication date: 2013
Peer-reviewed: Yes

Publication information

Journal: Journal of Signal Processing Systems
Volume: 71
Issue number: 3
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2013): CiteScore 2.1 SJR 0.254 SNIP 0.866
Original language: English
ASJC Scopus subject areas: Hardware and Architecture, Information Systems, Signal Processing, Theoretical Computer Science, Control and Systems Engineering, Modelling and Simulation
Keywords: Dataflow, Image registration, Scheduling, Software tools, Turbo decoder
DOIs:

10.1007/s11265-012-0719-x
URLs:

http://www.scopus.com/inward/record.url?scp=84879696501&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84879696501
Research output: Contribution to journal › Article › Scientific › peer-review

PiMM: Parameterized and interfaced dataflow meta-model for MPSoCs runtime reconfiguration

Dataflow models of computation are widely used for the specification, analysis, and optimization of Digital Signal Processing (DSP) applications. In this paper a new meta-model called PiMM is introduced to address the important challenge of managing dynamics in DSP-oriented representations. PiMM extends a dataflow model by introducing an explicit parameter dependency tree and an interface-based hierarchical compositionality mechanism. PiMM favors the design of highly-efficient heterogeneous multicore systems, specifying algorithms with customizable trade-offs among predictability and exploitation of both static and adaptive task, data and pipeline parallelism. PiMM fosters design space exploration and reconfigurable resource allocation in a flexible dynamic dataflow context.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), UBL, University of Maryland, Texas Instruments France S.A
Contributors: Desnos, K., Pelcat, M., Nezan, J. F., Bhattacharyya, S. S., Aridhi, S.
Number of pages: 8
Pages: 41-48
Publication date: 2013

Host publication information

Title of host publication: Proceedings - 2013 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, IC-SAMOS 2013
Publisher: IEEE COMPUTER SOCIETY PRESS
Article number: 6621104
ISBN (Print): 9781479901036
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering, Modelling and Simulation
DOIs:

10.1109/SAMOS.2013.6621104
URLs:

http://www.scopus.com/inward/record.url?scp=84888883761&partnerID=8YFLogxK (Link to publication in Scopus)

Source: Scopus
Source ID: 84888883761
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Programmable implementation of zero-crossing demodulator on an application specific processor

The zero-intermediate frequency zero-crossing demodulator (ZIFZCD) is extensively used for demodulating continuous phase frequency shift keying (CPFSK) signals in low power and low cost devices. ZIFZCD has previously been implemented as hardwired circuits. Many variations have been suggested to the ZIFZCD algorithm for different modulation methods and channel conditions. To support all these variants, a programmable processor based implementation of the ZIFZCD is needed. This paper describes a programmable software implementation of ZIFZCD on an application specific processor (ASP). The ASP is based on transport triggered architecture (TTA) and provides an ideal low power platform for ZIFZCD implementation due to its simplicity. The designed processor operates at a maximum clock frequency of 250 MHz and has gate count of 134 kGE for a 32-bit TTA processor and 76 kGE for a 16-bit processor. The demodulator has been developed as a part of an open source radio implementation for wireless sensor nodes.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), Dept. of Computer Science and Engineering, Univ of Oulu
Contributors: Ghazi, A., Boutellier, J., Hannuksela, J., Shahabuddin, S., Silvén, O.
Number of pages: 6
Pages: 231-236
Publication date: 2013

Host publication information

Title of host publication: 2013 IEEE Workshop on Signal Processing Systems, SiPS 2013
Publisher: Institute of Electrical and Electronics Engineers Inc.
Article number: 6674510
ISBN (Print): 9781467362382
ASJC Scopus subject areas: Electrical and Electronic Engineering, Signal Processing, Applied Mathematics, Hardware and Architecture
Keywords: Demodulation, Signal Processing, Software radio
URLs:

http://www.scopus.com/inward/record.url?scp=84896460964&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84896460964
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Scheduling of parallelized synchronous dataflow actors

Parallelization of Digital Signal Processing (DSP) software is an important trend for Multi Processor System-on-Chip (MPSoC) implementation. The performance of DSP systems composed of parallelized computations depends on the scheduling technique, which must in general allocate computation and communication resources for competing tasks, and ensure that data dependencies are satisfied. In this paper, we formulate a new type of parallel task scheduling problem called Parallel Actor Scheduling (PAS) for MPSoC mapping of DSP systems that are represented as Synchronous DataFlow (SDF) graphs. In contrast to traditional SDF -based scheduling techniques, which focus on exploiting graph level (inter-actor) parallelism, the PAS problem targets the integrated exploitation of both intra- and inter-actor parallelism for platforms in which individual actors can be parallelized across multiple processing units. We address a special case of the PAS problem in which all of the actors in the DSP application or subsystem being optimized can be parallelized. For this special case, we develop and experimentally evaluate a two-phase scheduling framework with two work flows - particle swarm optimization with a mixed integer programming formulation, and particle swarm optimization with a fast heuristic based on list scheduling. We demonstrate that our PAS-targeted scheduling framework provides a useful range of trade-off's between synthesis time requirements and the quality of the derived solutions.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), University of Maryland, UBL, Department of Electrical and Computer Engineering
Contributors: Zhou, Z., Desnos, K., Pelcat, M., Nezan, J. F., Plishker, W., Bhattacharyya, S. S.
Publication date: 2013

Host publication information

Title of host publication: 2013 International Symposium on System-on-Chip, SoC 2013 - Proceedings
Publisher: IEEE COMPUTER SOCIETY PRESS

Article number: 6675271
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
URLs:

http://www.scopus.com/inward/record.url?scp=84896974096&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84896974096
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Touch gestures in communicating emotional intention via vibrotactile stimulation

Remote communication between people typically relies on audio and vision although current mobile devices are increasingly based on detecting different touch gestures such as swiping. These gestures could be adapted to interpersonal communication by using tactile technology capable of producing touch stimulation to a user's hand. It has been suggested that such mediated social touch would allow for new forms of emotional communication. The aim was to study whether vibrotactile stimulation that imitates human touch can convey intended emotions from one person to another. For this purpose, devices were used that converted touch gestures of squeeze and finger touch to vibrotactile stimulation. When one user squeezed his device or touched it with finger(s), another user felt corresponding vibrotactile stimulation on her device via four vibrating actuators. In an experiment, participant dyads comprising a sender and receiver were to communicate variations in the affective dimensions of valence and arousal using the devices. The sender's task was to create stimulation that would convey unpleasant, pleasant, relaxed, or aroused emotional intention to the receiver. Both the sender and receiver rated the stimulation using scales for valence and arousal so that the match between sender's intended emotions and receiver's interpretations could be measured. The results showed that squeeze was better at communicating unpleasant and aroused emotional intention, while finger touch was better at communicating pleasant and relaxed emotional intention. The results can be used in developing technology that enables people to communicate via touch by choosing touch gesture that matches the desired emotion.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Augmented Human Activities (AHA), Field robotics for efficient work sites (FIRE)
Contributors: Rantala, J., Salminen, K., Raisamo, R., Surakka, V.
Number of pages: 12
Pages: 679-690
Publication date: 2013
Peer-reviewed: Yes

Publication information

Journal: International Journal of Human-Computer Studies
Volume: 71
Issue number: 6
ISSN (Print): 1071-5819
Ratings:

Scopus rating (2013): CiteScore 4.6 SJR 0.861 SNIP 2.378
Original language: English
ASJC Scopus subject areas: Human Factors and Ergonomics, Software, Education, Engineering(all), Human-Computer Interaction, Hardware and Architecture
Keywords: Affective interaction, Emotions, Haptics, Mediated social touch, Mobile devices, Tactile communication
DOIs:

10.1016/j.ijhcs.2013.02.004
URLs:

http://www.scopus.com/inward/record.url?scp=84876589281&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84876589281
Research output: Contribution to journal › Article › Scientific › peer-review

Wireless chipless passive microfluidic temperature sensor

Autonomous wireless sensors are a key technology for Ambiant Intelligence. For several years, chipless-electromagnetics sensors are studied to overcome the limitations of other passive sensors like low interrogation distance. In this paper we present a new concept of passive temperature sensor based on the electromagnetic coupling between an RF capacitor and dielectric liquid moving inside a SU8 micro-channel. The concept is validated using water as dielectric liquid with a full scale variation of S11 versus temperature around 8dB at 29.75GHz

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication

Organisations: Sensing Systems for Wireless Medicine (MediSense), University of Toulouse, INP, LAAS-CNRS, Georgia Institute of Technology
Contributors: Rifai, A., Debourg, E., Bouaziz, S., Traille, A., Pons, P., Aubert, H., Tentzeris, M.
Number of pages: 4
Pages: 1024-1027
Publication date: 2013

Host publication information
Title of host publication: 2013 Transducers and Eurosensors XXVII: The 17th International Conference on Solid-State Sensors, Actuators and Microsystems, TRANSDUCERS and EUROSENSORS 2013
Article number: 6626944
ISBN (Print): 9781467359818
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
Keywords: Chipless sensor, Passive sensor, RF and microfluidic coupling, Wireless sensor
DOIs:

10.1109/Transducers.2013.6626944
URLs:

http://www.scopus.com/inward/record.url?scp=84891687523&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84891687523
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Application-specific instruction processor for extracting local binary patterns
Local Binary Pattern (LBP) is texture operator used in preprocessing for object detection, tracking, face recognition and fingerprint matching. Many of these applications are performed on embedded devices, which poses limitations on the implementation complexity and power consumption. As LBP features are computed pixelwise, high performance is required for real time extraction of LBP features from high resolution video. This paper presents an application-specific instruction processor for LBP extraction. The compact, yet powerful processor is capable of extracting LBP features from 1280 × 720p (30 fps) video with a reasonable 304 MHz clock rate. With a low power consumption and an area of less than 16k gates the processor is suitable for embedded devices. Experiments present resource and power consumption measured on an FPGA board, along with processor synthesis results. In terms of latency, our processor requires 17.5 × less clock cycles per LBP feature than a workstation implementation and only 2.0 × more than a hardwired ASIC.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), Dept. of Computer Science and Engineering, Univ of Oulu
Contributors: Boutellier, J., Lundbom, I., Janhunen, J., Ylimainen, J., Hannuksela, J.
Number of pages: 8
Pages: 82-89
Publication date: 2012

Host publication information
Title of host publication: DASIP 2012 - Proceedings of the 2012 Conference on Design and Architectures for Signal and Image Processing
Article number: 6385363
ISBN (Print): 9782953998726
ASJC Scopus subject areas: Computer Graphics and Computer-Aided Design, Computer Vision and Pattern Recognition, Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
Keywords: Digital signal processors, Feature extraction, Image texture analysis, Video signal processing
URLs:

http://www.scopus.com/inward/record.url?scp=84872397244&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84872397244
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

fs-PGBR: A scalable and delay sensitive cloud routing protocol
This paper proposes an improved version of a fully distributed routing protocol, that is applicable for cloud computing infrastructure. Simulation results shows the protocol is ideal for discovering cloud services in a scalable manner with minimum latency.

General information
Publication status: Published

MoE publication type: A4 Article in a conference publication
Organisations: Wireless Communications and Positioning (WICO), Waterford Institute of Technology, Telecommunications Software and Systems Group (TSSG), University of Helsinki
Contributors: Mineraud, J., Balasubramaniam, S., Kangasharju, J., Donnelly, W.
Number of pages: 2
Pages: 301-302
Publication date: 2012

Host publication information
Title of host publication: SIGCOMM'12 - Proceedings of the ACM SIGCOMM 2012 Conference Applications, Technologies, Architectures, and Protocols for Computer Communication
ISBN (Print): 9781450314190
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Electrical and Electronic Engineering
Keywords: cloud computing infrastructure, scalable route discovery
DOIs:

10.1145/2342356.2342420
URLs:

http://www.scopus.com/inward/record.url?scp=84866508870&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84866508870
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

GPU-based acceleration of symbol timing recovery
This paper presents a novel implementation of graphics processing unit (GPU) based symbol timing recovery using polyphase interpolators to detect symbol timing error. Symbol timing recovery is a compute intensive procedure that detects and corrects the timing error in a coherent receiver. We provide optimal sample-time timing recovery using a maximum likelihood (ML) estimator to minimize the timing error. This is an iterative and adaptive system that relies on feedback, therefore, we present an accelerated implementation design by using a GPU for timing error detection (TED), enabling fast error detection by exploiting the 2D filter structure found in the polyphase interpolator. We present this hybrid/heterogeneous CPU and GPU architecture by computing a low complexity and low noise matched filter (MF) while simultaneously performing TED. We then compare the performance of the CPU vs. GPU based timing recovery for different interpolation rates to minimize the error and improve the detection by up to a factor of 35. We further improve the process by utilizing GPU optimization and performing block processing to improve the throughput even more, all while maintaining the lowest possible sampling rate.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), University of Maryland, Department of Electrical and Computer Engineering, Rice University
Contributors: Kim, S. C., Plishker, W. L., Bhattacharyya, S. S., Cavallaro, J. R.
Number of pages: 8
Pages: 273-280
Publication date: 2012

Host publication information
Title of host publication: DASIP 2012 - Proceedings of the 2012 Conference on Design and Architectures for Signal and Image Processing
Article number: 6385393
ISBN (Print): 9782953998726
ASJC Scopus subject areas: Computer Graphics and Computer-Aided Design, Computer Vision and Pattern Recognition, Hardware and Architecture, Signal Processing, Electrical and Electronic Engineering
Keywords: coherent receiver design, DSP accelerator, GPU, symbol timing recovery, synchronization
URLs:

http://www.scopus.com/inward/record.url?scp=84872402791&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84872402791
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Inkjet-printed monopole antennas for enhanced-range WBAN and wearable biomonitoring application
In this paper, a monopole antenna backed by an inkjet-printed electromagnetic band gap ground (EBG) plane on paper substrate is proposed for wearable applications with drastically enhanced communication range. This novel design approach for WBAN and wearable biomonitoring applications alleviates the on-body antenna's performance degradation, which may cause a significant degradation of the wireless system's performance as well. The communication range

improvement compared to conventional antenna is demonstrated by using a benchmarking commercial wireless temperature sensor module. In addition, the advantages and the integrability of the proposed wearable antenna topology into mobile wireless on-body health care systems is discussed in detail.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Sensing Systems for Wireless Medicine (MediSense), Georgia Institute of Technology, University of Tokyo
Contributors: Kim, S., Kawahara, Y., Tentzeris, M. M.
Number of pages: 6
Pages: 33-38
Publication date: 2012

Host publication information
Title of host publication: MobileHealth'12 - Proceedings of the 2nd ACM International Workshop on Pervasive Wireless Healthcare
ISBN (Print): 9781450312929
ASJC Scopus subject areas: Software, Hardware and Architecture, Computer Networks and Communications
Keywords: electromagnetic band gap (ebg) structure, inkjet printing, personal area networks (pans), system level antenna integration, wearable antenna, wireless body area networks (wbans)
DOIs:

10.1145/2248341.2248355
URLs:

http://www.scopus.com/inward/record.url?scp=84863544257&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84863544257
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Instrumentation-driven model detection for dataflow graphs
Dataflow modeling offers a myriad of tools to improve optimization and analysis of signal processing applications, and is often used by designers to help design, implement, and maintain systems on chip for signal processing. However, maintaining and upgrading legacy systems that were not originally designed using dataflow modeling can be challenging. To facilitate maintenance, designers often convert legacy code to dataflow graphs, a process that can be difficult and time consuming. We propose a method to facilitate this conversion process by automatically detecting the dataflow models of the core functions. The contribution of this work is twofold. First, we introduce a generic method for instrumenting dataflow graphs that can be used to measure various statistics and extract run-time information. Second, we use this instrumentation technique to demonstrate a method that facilitates the conversion of legacy code to dataflow-based implementations. This method operates by automatically detecting the dataflow model of the core functions being converted.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), University of Maryland, Department of Electrical and Computer Engineering
Contributors: Chukhman, I., Plishker, W., Bhattacharyya, S. S.
Publication date: 2012

Host publication information
Title of host publication: 2012 International Symposium on System on Chip, SoC 2012
Article number: 6376361
ISBN (Print): 9781467328951
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
Keywords: Dataflow graphs, models of computation, signal processing systems
DOIs:

10.1109/ISSoC.2012.6376361
URLs:

http://www.scopus.com/inward/record.url?scp=84871986955&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84871986955
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Mapping parameterized cyclo-static dataflow graphs onto configurable hardware
In recent years, parameterized dataflow has evolved as a useful framework for modeling synchronous and cyclo-static graphs in which arbitrary parameters can be changed dynamically. Parameterized dataflow has proven to have significant

expressive power for managing dynamics of DSP applications in important ways. However, efficient hardware synthesis techniques for parameterized dataflow representations are lacking. This paper addresses this void; specifically, the paper investigates efficient field programmable gate array (FPGA)-based implementation of parameterized cyclo-static dataflow (PCSDF) graphs. We develop a scheduling technique for throughput-constrained minimization of dataflow buffering requirements when mapping PCSDF representations of DSP applications onto FPGAs. The proposed scheduling technique is integrated with an existing formal schedule model, called the generalized schedule tree, to reduce schedule cost. To demonstrate our new, hardware-oriented PCSDF scheduling technique, we have designed a real-time base station emulator prototype based on a subset of long-term evolution (LTE), which is a key cellular standard.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), National Instruments, University of Maryland, Department of Electrical and Computer Engineering
Contributors: Kee, H., Shen, C. C., Bhattacharyya, S. S., Wong, I., Rao, Y., Kornerup, J.
Number of pages: 17
Pages: 285-301
Publication date: 2012
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
Volume: 66
Issue number: 3
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2012): CiteScore 2.1 SJR 0.269 SNIP 0.879
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: 4G communication systems, Dataflow modeling, FPGA implementation, Parameterized dataflow, Scheduling
DOIs:

10.1007/s11265-011-0599-5
URLs:

http://www.scopus.com/inward/record.url?scp=84888881360&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84888881360
Research output: Contribution to journal › Article › Scientific › peer-review

Multidimensional dataflow graph modeling and mapping for efficient GPU implementation
Multidimensional synchronous dataflow (MDSDF) provides an effective model of computation for a variety of multidimensional DSP systems that have static dataflow structures. In this paper, we develop new methods for optimized implementation of MDSDF graphs on embedded platforms that employ multiple levels of parallelism to enhance performance at different levels of granularity. Our approach allows designers to systematically represent and transform multi-level parallelism specifications from a common, MDSDF-based application level model. We demonstrate our methods with a case study of image histogram implementation on a graphics processing unit (GPU). Experimental results from this study show that our approach can be used to derive fast GPU implementations, and enhance trade-off analysis during design space exploration.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), University of Maryland, Air Force Research Laboratory Information Directorate, University of Missouri-Columbia, Department of Electrical and Computer Engineering
Contributors: Wang, L. H., Shen, C. C., Seetharaman, G., Palaniappan, K., Bhattacharyya, S. S.
Number of pages: 6
Pages: 300-305
Publication date: 2012

Host publication information
Title of host publication: Proceedings - 2012 IEEE Workshop on Signal Processing Systems, SiPS 2012
Article number: 6363272
ISBN (Print): 9780769548562
ASJC Scopus subject areas: Electrical and Electronic Engineering, Signal Processing, Applied Mathematics, Hardware and Architecture

Keywords: Dataflow graph, Graphics processing unit, Integral histogram, Multidimensional synchronous dataflow
DOIs:
10.1109/SiPS.2012.10
URLs:
http://www.scopus.com/inward/record.url?scp=84875330462&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84875330462
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Novel approaches to crawling important pages early

Web crawlers are essential to many Web applications, such as Web search engines, Web archives, and Web directories, which maintain Web pages in their local repositories. In this paper, we study the problem of crawl scheduling that biases crawl ordering toward important pages. We propose a set of crawling algorithms for effective and efficient crawl ordering by prioritizing important pages with the well-known PageRank as the importance metric. In order to score URLs, the proposed algorithms utilize various features, including partial link structure, inter-host links, page titles, and topic relevance. We conduct a large-scale experiment using publicly available data sets to examine the effect of each feature on crawl ordering and evaluate the performance of many algorithms. The experimental results verify the efficacy of our schemes. In particular, compared with the representative RankMass crawler, the FPR-title-host algorithm reduces computational overhead by a factor as great as three in running time while improving effectiveness by 5% in cumulative PageRank.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Research Community on Data-to-Decision (D2D), Korea University
Contributors: Alam, M. H., Ha, J. W., Lee, S. K.
Number of pages: 28
Pages: 707-734
Publication date: 2012
Peer-reviewed: Yes

Publication information

Journal: Knowledge and Information Systems
Volume: 33
Issue number: 3
ISSN (Print): 0219-1377
Ratings:
Scopus rating (2012): CiteScore 4.2 SJR 1.111 SNIP 2.008
Original language: English
ASJC Scopus subject areas: Software, Information Systems, Human-Computer Interaction, Hardware and Architecture, Artificial Intelligence
Keywords: Crawl ordering, Fractional PageRank, PageRank, Web crawler
DOIs:
10.1007/s10115-012-0535-4
URLs:
http://www.scopus.com/inward/record.url?scp=84869092092&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84869092092
Research output: Contribution to journal › Article › Scientific › peer-review

Partial expansion graphs: Exposing parallelism and dynamic scheduling opportunities for DSP applications

Emerging Digital Signal Processing (DSP) algorithms and wireless communications protocols require dynamicadaptation and online reconfiguration for the implementedsystems at runtime. In this paper, we introduce the conceptof Partial Expansion Graphs (PEGs) as an implementationmodel and associated class of scheduling strategies. PEGsare designed to help realize DSP systems in terms of formsand granularities of parallelism that are well matched to thegiven applications and targeted platforms. PEGs also facilitatederivation of both static and dynamic scheduling techniques,depending on the amount of variability in task execution timesand other operating conditions. We show how to implementefficient PEG-based scheduling methods using real time operating systems, and to re-use pre-optimized libraries of DSPcomponents within such implementations. Empirical resultsshow that the PEG strategy can 1) achieve significant speedupson a state of the art multicore signal processor platform forstatic dataflow applications with predictable execution times,and 2) exceed classical scheduling speedups for applicationshaving execution times that can vary dynamically. This abilityto handle variable execution times is especially useful as DSPapplications and platforms increase in complexity and adaptive behavior, thereby reducing execution time predictability.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), University of Maryland, Department of Electrical and Computer Engineering, Texas Instruments
Contributors: Zaki, G. F., Plishker, W., Bhattacharyya, S. S., Fruth, F.
Number of pages: 8
Pages: 86-93
Publication date: 2012

Host publication information
Title of host publication: Proceedings - 2012 IEEE 23rd International Conference on Application-Specific Systems, Architectures and Processors, ASAP 2012
Article number: 6341457
ISBN (Print): 9780769547688
ASJC Scopus subject areas: Hardware and Architecture, Computer Networks and Communications
Keywords: Data?ow Graphs, Digital Signal Processing, Multiprocessor Dynamic Scheduling
DOIs:

10.1109/ASAP.2012.14
URLs:

http://www.scopus.com/inward/record.url?scp=84870763020&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84870763020
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Power allocation in multi-node cooperative network in Rician fading channels
Cooperative communications have been recommended to exploit the inherent spatial diversity gains in multiuser wireless systems without the need of multiple transceivers at each node. This is achieved when wireless nodes help to each other to send multiple independent transmission paths to the destination. The advantage of cooperation can be exploited significantly by allocating the power of the system optimally. Thus, in this paper we first derive the approximate symbol error rate (SER) for multi-node cooperative networks employing decode-and-forward (DF) protocol with a maximum ratio combining (MRC) at the receiving terminals in Racian fading channels. Using the approximated SER expression, optimal power allocation (OPA) scheme under different line-of-sight (LOS) scenarios is investigated. Numerical and simulation results are presented to illustrate the performance improvement due to OPA of the cooperative networks.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Wireless Communications and Positioning (WICO), Department of Computer Science, University of Vaasa (UVA)
Contributors: Fikadu, M. K., Elmusrati, M., Virrankoski, R.
Number of pages: 6
Pages: 496-501
Publication date: 2012

Host publication information
Title of host publication: 2012 IEEE 8th International Conference on Wireless and Mobile Computing, Networking and Communications, WiMob 2012
Article number: 6379119
ISBN (Print): 9781467314305
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Software
Keywords: Cooperative, decode-and-forward, multi-node, optimal power allocation, Rician fading, SER analysis
DOIs:

10.1109/WiMOB.2012.6379119
URLs:

http://www.scopus.com/inward/record.url?scp=84872085066&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84872085066
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Reconfigurable miniature sensor nodes for condition monitoring
The wireless sensor networks are being deployed at escalating rate for various application fields. The ever growing number of application areas requires a diverse set of algorithms with disparate processing needs. The wireless sensor networks also need to adapt to the prevailing energy conditions and processing requirements. The preceding reasons rule out the use of a single fixed design. Instead a general purpose design that can rapidly adapt to different conditions and

requirements is desired. In lieu of the traditional inflexible wireless sensor node consisting of a micro-controller, radio transceiver, sensor array and energy storage, we propose a rapidly reconfigurable miniature sensor node, implemented with a transport triggered architecture processor on a low-power Flash FPGA. Also power consumption and silicon area usage comparison between 16-bit fixed and floating point and 32-bit floating point implementations is presented in this paper. The implemented processors and algorithms are intended for rolling bearing condition monitoring, but can be fully extended for other applications as well.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), Univ of Oulu, Computer Science and Engineering Laboratory
Contributors: Nylanden, T., Boutellier, J., Nikunen, K., Hannuksela, J., Silven, O.
Number of pages: 7
Pages: 113-119
Publication date: 2012

Host publication information
Title of host publication: Proceedings - 2012 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, IC-SAMOS 2012
Article number: 6404164
ISBN (Print): 9781467322973
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering, Modelling and Simulation
DOIs:

10.1109/SAMOS.2012.6404164
URLs:

http://www.scopus.com/inward/record.url?scp=84873554935&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84873554935
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

The development of constructability using BIM as an intensifying technology
According to the several international research and development articles, completed building plans that take care of constructability issues, contributes the achievement of construction objectives of time, cost and quality.A good constructability improves construction performance, productivity and quality. Building information modeling (BIM) has the similar effect to construction. BIM simulates the construction project in a virtual environment. It is possible to make constructability adjustments in the model, and practice construction before it is actualized.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Life Cycle Effectiveness of the Built Environment (LCE@BE), Aalto University
Contributors: Tauriainen, M., Mero, A. K., Lemström, A., Puttonen, J., Saari, A.
Number of pages: 4
Pages: 713-716
Publication date: 2012

Host publication information
Title of host publication: eWork and eBusiness in Architecture, Engineering and Construction - Proceedings of the European Conference on Product and Process Modelling 2012, ECPPM 2012
ISBN (Print): 9780415621281
ASJC Scopus subject areas: Hardware and Architecture, Modelling and Simulation
URLs:

http://www.scopus.com/inward/record.url?scp=84863525009&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84863525009
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Overview of the MPEG reconfigurable video coding framework
Video coding technology in the last 20 years has evolved producing a variety of different and complex algorithms and coding standards. So far the specification of such standards, and of the algorithms that build them, has been done case by case providing monolithic textual and reference software specifications in different forms and programming languages. However, very little attention has been given to provide a specification formalism that explicitly presents common components between standards, and the incremental modifications of such monolithic standards. The MPEG Reconfigurable Video Coding (RVC) framework is a new ISO standard currently under its final stage of standardization,

aiming at providing video codec specifications at the level of library components instead of monolithic algorithms. The new concept is to be able to specify a decoder of an existing standard or a completely new configuration that may better satisfy application-specific constraints by selecting standard components from a library of standard coding algorithms. The possibility of dynamic configuration and reconfiguration of codecs also requires new methodologies and new tools for describing the new bitstream syntaxes and the parsers of such new codecs. The RVC framework is based on the usage of a new actor/ dataflow oriented language called CAL for the specification of the standard library and instantiation of the RVC decoder model. This language has been specifically designed for modeling complex signal processing systems. CAL dataflow models expose the intrinsic concurrency of the algorithms by employing the notions of actor programming and dataflow. The paper gives an overview of the concepts and technologies building the standard RVC framework and the non standard tools supporting the RVC model from the instantiation and simulation of the CAL model to software and/or hardware code synthesis.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), Department of Electrical and Computer Engineering, University of Maryland, Ericsson Research, Xilinx Research Labs, CRPP, UBL
Contributors: Bhattacharyya, S. S., Eker, J., Janneck, J. W., Lucarz, C., Mattavelli, M., Raulet, M.
Number of pages: 13
Pages: 251-263
Publication date: May 2011
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems
Volume: 63
Issue number: 2
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2011): CiteScore 1.8 SJR 0.248 SNIP 0.707
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: CAL actor language, Code synthesis, Dataflow programming, Reconfigurable Video Coding
DOIs:

10.1007/s11265-009-0399-3
URLs:

http://www.scopus.com/inward/record.url?scp=79954574143&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 79954574143
Research output: Contribution to journal › Article › Scientific › peer-review

Quasi-static scheduling of CAL actor networks for reconfigurable video coding
The upcoming Reconfigurable Video Coding (RVC) standard from MPEG (ISO / IEC SC29WG11) defines a library of coding tools to specify existing or new compressed video formats and decoders. The coding tool library has been written in a dataflow/actor-oriented language named CAL. Each coding tool (actor) can be represented with an extended finite state machine and the data communication between the tools are described as dataflow graphs. This paper proposes an approach to model the CAL actor network with Parameterized Synchronous Data Flow and to derive a quasi-static multiprocessor execution schedule for the system. In addition to proposing a scheduling approach for RVC, an extension to the well-known permutation flow shop scheduling problem that enables rapid run-time scheduling of RVC tasks, is introduced.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), Machine Vision Group, Univ of Oulu, CRPP, Abo Akad Univ, Abo Akademi University, Dept Phys
Contributors: Boutellier, J., Lucarz, C., Lafond, S., Gomez, V. M., Mattavelli, M.
Number of pages: 12
Pages: 191-202
Publication date: May 2011
Peer-reviewed: Yes

Publication information
Journal: Journal of Signal Processing Systems

Volume: 63
Issue number: 2
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2011): CiteScore 1.8 SJR 0.248 SNIP 0.707
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Digital signal processors, Modeling, Parallel processing, Scheduling
DOIs:

10.1007/s11265-009-0389-5
URLs:

http://www.scopus.com/inward/record.url?scp=79954614566&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 79954614566
Research output: Contribution to journal › Article › Scientific › peer-review

Exploiting statically schedulable regions in dataflow programs

Dataflow descriptions have been used in a wide range of Digital Signal Processing (DSP) applications, such as multi-media processing, and wireless communications. Among various forms of dataflow modeling, Synchronous Dataflow (SDF) is geared towards static scheduling of computational modules, which improves system performance and predictability. However, many DSP applications do not fully conform to the restrictions of SDF modeling. More general dataflow models, such as CAL (Eker and Janneck 2003), have been developed to describe dynamically-structured DSP applications. Such generalized models can express dynamically changing functionality, but lose the powerful static scheduling capabilities provided by SDF. This paper focuses on the detection of SDF-like regions in dynamic dataflow descriptions-in particular, in the generalized specification framework of CAL. This is an important step for applying static scheduling techniques within a dynamic dataflow framework. Our techniques combine the advantages of different dataflow languages and tools, including CAL (Eker and Janneck 2003), DIF (Hsu et al. 2005) and CAL2C (Roquier et al. 2008). In addition to detecting SDF-like regions, we apply existing SDF scheduling techniques to exploit the static properties of these regions within enclosing dynamic dataflow models. Furthermore, we propose an optimized approach for mapping SDF-like regions onto parallel processing platforms such as multi-core processors.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), University of Maryland, Xilinx Research Labs, UBL, Department of Electrical and Computer Engineering
Contributors: Gu, R., Janneck, J. W., Raulet, M., Bhattacharyya, S. S.
Number of pages: 14
Pages: 129-142
Publication date: Apr 2011
Peer-reviewed: Yes

Publication information

Journal: Journal of Signal Processing Systems
Volume: 63
Issue number: 1
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2011): CiteScore 1.8 SJR 0.248 SNIP 0.707
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Cal, Dataflow, DIF, Multicore processors, Quasi-static scheduling
DOIs:

10.1007/s11265-009-0445-1
URLs:

http://www.scopus.com/inward/record.url?scp=79954601701&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 79954601701
Research output: Contribution to journal › Article › Scientific › peer-review

Bit-sliced binary normal basis multiplication

The performance of many cryptographic primitives is reliant on efficient algorithms and implementation techniques for arithmetic in binary fields. While dedicated hardware support for said arithmetic is an emerging trend, the study of software-only implementation techniques remains important for legacy or non-equipped processors. One such technique is that of software-based bit-slicing. In the context of binary fields, this is an interesting option since there is extensive previous work on bit-oriented designs for arithmetic in hardware, such designs are intuitively well suited to bit-slicing in software. In this paper we harness previous work, using it to investigate bit-sliced, software-only implementation arithmetic for binary fields, over a range of practical field sizes and using a normal basis representation. We apply our results to demonstrate significant performance improvements for a stream cipher, and over the frequently employed Ning-Yin approach to normal basis implementation in software.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Intelligent dexterity for secure networked infrastructure and applications (IDSNIA), Department of Information and Computer Science, Aalto University, University of Bristol
Contributors: Brumley, B., Page, D.
Number of pages: 8
Pages: 205-212
Publication date: 2011

Host publication information

Title of host publication: Proceedings - 20th IEEE Symposium on Computer Arithmetic, ARITH-20
Article number: 5992128
ISBN (Print): 9780769543185
ASJC Scopus subject areas: Theoretical Computer Science, Software, Hardware and Architecture
Keywords: Algorithm design, analysis, Computations in finite fields, Computer arithmetic, Data encryption
DOIs:

10.1109/ARITH.2011.36
URLs:

http://www.scopus.com/inward/record.url?scp=80055027798&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 80055027798
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Design methods for wireless sensor network building energy monitoring systems

In this paper, we present a new energy analysis method for evaluating energy consumption of embedded sensor nodes at the application level and the network level. Then we apply the proposed energy analysis method to develop new energy management schemes in order to maximize lifetime for Wireless Sensor Network Building Energy Monitoring Systems (WSNBEMS). At the application level, we develop a new design approach that uses dataflow techniques to model the application-level interfacing behavior between the processor and sensors on an embedded sensor node. At the network level, we analyze the energy consumption of the IEEE 802.15.4 MAC functionality. Based on our techniques for modeling and energy analysis, we have implemented an optimized WSNBEMS for a real building, and validated our energy analysis techniques through measurements on this implementation. The performance of our implementation is also evaluated in terms of monitoring accuracy and energy consumption savings. We have demonstrated that by applying the proposed scheme, system lifetime can be improved significantly without affecting monitoring accuracy.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), University of Maryland, CoolCAD Electronics, Department of Electrical and Computer Engineering
Contributors: Cho, I., Shen, C. C., Potbhare, S., Bhattacharyya, S. S., Goldsman, N.
Number of pages: 8
Pages: 974-981
Publication date: 2011

Host publication information

Title of host publication: Proceedings of the 36th Annual IEEE Conference on Local Computer Networks, LCN 2011
Article number: 6115580
ISBN (Print): 9781612849287
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture
DOIs:

10.1109/LCN.2011.6115580
URLs:

http://www.scopus.com/inward/record.url?scp=84856182334&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84856182334
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Generation of all radix-2 fast Fourier transform algorithms using binary trees

In this work a systematic method to generate all possible fast Fourier transform (FFT) algorithms is proposed based on the relation to binary trees. The binary tree is used to represent the decomposition of a discrete Fourier transform (DFT) into sub-DFTs. The radix is adaptively changed according to compute sub-DFTs in proposed decomposition. In this work we determine the number of possible algorithms for 2^n-point FFTs with radix-2 butterfly operation and propose a simple method to determine the twiddle factor indices for each algorithm based on the binary tree representation.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Signal Processing Research Community (SPRC), Linköping University
Contributors: Qureshi, F., Gustafsson, O.
Number of pages: 4
Pages: 677-680
Publication date: 2011

Host publication information

Title of host publication: 2011 20th European Conference on Circuit Theory and Design, ECCTD 2011
Article number: 6043634
ISBN (Print): 9781457706189
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
DOIs:

10.1109/ECCTD.2011.6043634
URLs:

http://www.scopus.com/inward/record.url?scp=80355128275&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 80355128275
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Inkjet printing of UWB antennas on paper based substrates

For the first time, we demonstrate the feasibility of realizing ultra-wideband antennas through ink-jetting of conductive inks on commercially available paper sheets (paper as an RF substrate). The characterization of the conductive ink as well as of the electrical properties of the paper substrate is reported for frequencies up to 10GHz. This work is one step further towards the development of low-cost environmentfriendly conformal printed antennas/electronics for ad-hoc wireless sensor networks operating in rugged environments.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Sensing Systems for Wireless Medicine (MediSense), University of Waterloo, Georgia Institute of Technology, Fredericck Research Center
Contributors: Shaker, G., Rida, A., Safavi-Naeini, S., Tentzeris, M. M., Nikolaou, S.
Number of pages: 4
Pages: 3001-3004
Publication date: 2011

Host publication information

Title of host publication: Proceedings of the 5th European Conference on Antennas and Propagation, EUCAP 2011
Article number: 5782210
ISBN (Print): 9788882020743
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
URLs:

http://www.scopus.com/inward/record.url?scp=79959681803&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 79959681803
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Topological patterns for scalable representation and analysis of dataflow graphs

Tools for designing signal processing systems with their semantic foundation in dataflow modeling often use high-level graphical user interfaces (GUIs) or text based languages that allow specifying applications as directed graphs. Such graphical representations serve as an initial reference point for further analysis and optimizations that lead to platform-specific implementations. For large-scale applications, the underlying graphs often consist of smaller substructures that repeat multiple times. To enable more concise representation and direct analysis of such substructures in the context of high level DSP specification languages and design tools, we develop the modeling concept of topological patterns, and propose ways for supporting this concept in a high-level language. We augment the dataflow interchange format (DIF) language-a language for specifying DSP-oriented dataflow graphs-with constructs for supporting topological patterns, and we show how topological patterns can be effective in various aspects of embedded signal processing design flows using specific application examples.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Signal Processing Research Community (SPRC), University of Maryland, National Instruments, Air Force Research Laboratory Information Directorate, Department of Electrical and Computer Engineering
Contributors: Sane, N., Kee, H., Seetharaman, G., Bhattacharyya, S. S.
Number of pages: 16
Pages: 229-244
Publication date: 2011
Peer-reviewed: Yes

Publication information

Journal: Journal of Signal Processing Systems
Volume: 65
Issue number: 2
ISSN (Print): 1939-8018
Ratings:

Scopus rating (2011): CiteScore 1.8 SJR 0.248 SNIP 0.707
Original language: English
ASJC Scopus subject areas: Control and Systems Engineering, Theoretical Computer Science, Signal Processing, Information Systems, Modelling and Simulation, Hardware and Architecture
Keywords: Dataflow graphs, High-level languages, Model-based design, Signal processing systems, Topological patterns
DOIs:

10.1007/s11265-011-0610-1
URLs:

http://www.scopus.com/inward/record.url?scp=84905269801&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 84905269801
Research output: Contribution to journal › Article › Scientific › peer-review

Nonlinear robust control for dc-dc converters

This paper introduces a robust nonlinear controller for a switch mode DC-DC boost converter. This innovative controller is employed to achieve the desired dynamic performance during steady state and transient operations. Step changes are considered in the load, the input and the desired output voltages, while unknown, but bounded disturbances corrupt the output load and the supply voltage. Practical stability of the converter is assured in the presence of those disturbances provided their maximum possible variation is known. Simulation results are provided to substantiate the applicability of the proposed control scheme.

General information

Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: National Technical University of Athens, Department of Electrical Engineering and Computer Science
Contributors: Soldatos, A. G., Karamanakos, P. P., Pavlou, K. G., Manias, S. N.
Number of pages: 4
Pages: 994-997
Publication date: Dec 2010

Host publication information

Title of host publication: 2010 IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2010 - Proceedings
ISBN (Print): 9781424481576
ASJC Scopus subject areas: Hardware and Architecture, Electrical and Electronic Engineering
Keywords: DC-DC converter, Nonlinear control, Robust control

Electronic versions:

Nonlinear robust control for dc-dc converters 2010
DOIs:

10.1109/ICECS.2010.5724681
URLs:

http://urn.fi/URN:NBN:fi:tuni-202005115176
Source: Scopus
Source ID: 79953095592
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Conversion algorithms and implementations for koblitz curve cryptography

In this paper, we discuss conversions between integers and \tau-adic expansions and we provide efficient algorithms and hardware architectures for these conversions. The results have significance in elliptic curve cryptography using Koblitz curves, a family of elliptic curves offering faster computation than general elliptic curves. However, in order to enable these faster computations, scalars need to be reduced and represented using a special base-τ expansion. Hence, efficient conversion algorithms and implementations are necessary. Existing conversion algorithms require several complicated operations, such as multiprecision multiplications and computations with large rationals, resulting in slow and large implementations in hardware and microcontrollers with limited instruction sets. Our algorithms are designed to utilize only simple operations, such as additions and shifts, which are easily implementable on practically all platforms. We demonstrate the practicability of the new algorithms by implementing them on Altera Stratix ‖ FPGAs. The implementations considerably improve both computation speed and required area compared to the existing solutions.

General information

Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Pervasive Computing, Aalto University
Contributors: Brumley, B. B., Jarvinen, K. U.
Number of pages: 12
Pages: 81-92
Publication date: 4 Jan 2010
Peer-reviewed: Yes

Publication information

Journal: IEEE Transactions on Computers
Volume: 59
Issue number: 1
Article number: 5255226
ISSN (Print): 0018-9340
Ratings:

Scopus rating (2010): SJR 0.584 SNIP 1.868
Original language: English
ASJC Scopus subject areas: Software, Theoretical Computer Science, Hardware and Architecture, Computational Theory and Mathematics
Keywords: Elliptic curve cryptography, Field-programmable gate arrays, Koblitz curves, Public-key cryptosystems
DOIs:

10.1109/TC.2009.132
URLs:

http://www.scopus.com/inward/record.url?scp=72949120592&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 72949120592
Research output: Contribution to journal › Article › Scientific › peer-review

OPAS: Ontology processing for assisted synthesis of conceptual design solutions

This article focuses on a key phase of the conceptual design, the synthesis of structural concepts of solution. Several authors have described this phase of Engineering Design. The Function-Behavior-Structure (FBS) is one of these models. This study is based on the combined use of a modified version of Gero's FBS model and the latest developments of modeling languages for systems engineering. System Modeling Language (SysML) is a general-purpose graphical modeling language for specifying, analyzing, designing, and verifying complex systems. Our development shows how SysML types of diagrams match with our updated vision of the FBS model of conceptual design. The objective of this paper is to present the possibility to use artificial intelligence tools as members of the design team for supporting the synthesis process. The common point of expert systems developed during last decades for the synthesis of conceptual solutions is that their knowledge bases were application dependent. Latest research in the field of Ontology showed the possibility to build knowledge representations in a reusable and shareable manner This allows the construction of knowledge representation for engineering in a more generic manner and dynamic mapping of the ontology layers. We

present here how processing on ontology allows the synthesis of conceptual solutions.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: Tallinn University of Technology, Ecole Centrale Nantes, Aalto Univ, Aalto University, Aalto Univ Finland, Dept Engn Design & Prod, Sch Engn, Helsinki University of Technology
Contributors: Christophe, F., Sell, R., Bernard, A., Coatanéa, E.
Number of pages: 12
Pages: 249-260
Publication date: 2010

Host publication information
Title of host publication: Proceedings of the ASME International Design Engineering Technical Conferences and Computers and Information in Engineering Conference 2009, DETC2009
Volume: 5
Edition: PART A
ISBN (Print): 9780791849026
ASJC Scopus subject areas: Computer Networks and Communications, Hardware and Architecture, Electrical and Electronic Engineering
Keywords: Conceptual design, FBS model, Knowledge representation, Ontology, Semantic web standards, SysML, Systems engineering, Taxonomy
DOIs:

10.1115/DETC2009-87776
URLs:

http://www.scopus.com/inward/record.url?scp=77953689077&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 77953689077
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Cavity formation in split ring resonators
We report that it is possible to obtain a cavity structure by the deformation of a unit cell of an split ring resonator (SRR) structure. We presented the Q-factor of the cavity resonance as 192 for an SRR-based single cavity. Subsequently, we brought two and three cavities together with an intercavity distance of two metamaterial unit cells and investigated the transmission spectrum of SRR-based interacting 2-cavity and 3-cavity systems. The splitting of eigenmodes due to the interaction between the localized electromagnetic cavity modes was observed. Eventually, in taking full advantage of the effective medium theory, we modeled SRR-based cavities as 1D Fabry-Perot reflectors (FPRs) with a subwavelength cavity at the center. Finally, we observed that at the cavity resonance, the effective group velocity was reduced by a factor of 67 for an SRR-based single cavity compared to the electromagnetic waves propagating in free space.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Nanotechnology Research Center, Harvard University
Contributors: Caglayan, H., Bulu, I., Loncar, M., Ozbay, E.
Number of pages: 5
Pages: 200-204
Publication date: Dec 2008
Peer-reviewed: Yes

Publication information
Journal: Photonics and Nanostructures - Fundamentals and Applications
Volume: 6
Issue number: 3-4
ISSN (Print): 1569-4410
Ratings:

Scopus rating (2008): SJR 1.212 SNIP 1.169
Original language: English
ASJC Scopus subject areas: Electrical and Electronic Engineering, Hardware and Architecture, Condensed Matter Physics, Atomic and Molecular Physics, and Optics, Electronic, Optical and Magnetic Materials
Keywords: Cavity, Metamaterials, Split rind resonator
DOIs:

10.1016/j.photonics.2008.09.001
URLs:

http://www.scopus.com/inward/record.url?scp=56049112536&partnerID=8YFLogxK (Link to publication in Scopus)

Bibliographical note
EXT="Caglayan, Humeyra"
Source: Scopus
Source ID: 56049112536
Research output: Contribution to journal › Article › Scientific › peer-review

Dynamic and sensitivity analysis of KNTU CDRPM: A cable driven redundant parallel manipulator
KNTU CDRPM is a cable driven redundant parallel manipulator, which is under investigation for possible implementation of large workspace applications. This newly developed manipulators have several advantages compared to the conventional parable mechanisms. In this paper, the governing dynamic equation of motion of such structure is derived using the Newton-Euler formulation. Next, the dynamic equations of the system are used in simulations. It is shown that on the contrary to serial manipulators, dynamic equations of motion of cable-driven parallel manipulators can be only represented implicitly, and only special integration routines can be used for their simulations. In order to verify the accuracy and integrity of the derived dynamic equations, open-and closed-loop simulations for the system is performed and analyzed. Also, the effects of mechanical assembly tolerances on the closed-loop control performance of a cable driven parallel robot are studied in detail, and the sensitivity analysis of the precision in the construction and assembly of the system on the closed-loop behavior of the KNTU CDRPM is performed.

General information
Publication status: Published
MoE publication type: A4 Article in a conference publication
Organisations: K. N. Toosi University of Technology
Contributors: Aref, M. M., Gholami, P., Taghirad, H. D.
Number of pages: 6
Pages: 528-533
Publication date: 2008

Host publication information
Title of host publication: 2008 IEEE/ASME International Conference on Mechatronics and Embedded Systems and Applications, MESA 2008
Article number: 4735650
ISBN (Print): 9781424423682
ASJC Scopus subject areas: Artificial Intelligence, Hardware and Architecture, Electrical and Electronic Engineering
DOIs:
10.1109/MESA.2008.4735650
URLs:
http://www.scopus.com/inward/record.url?scp=60749106647&partnerID=8YFLogxK (Link to publication in Scopus)
Source: Scopus
Source ID: 60749106647
Research output: Chapter in Book/Report/Conference proceeding › Conference contribution › Scientific › peer-review

Physics and applications of photonic crystals
In this article, we investigate how the photonic band gaps and the variety of band dispersions of photonic crystals can be utilized for various applications and how they further give rise to completely novel optical phenomena. The enhancement of spontaneous emission through coupled cavity waveguides in a one-dimensional silicon nitride photonic microcrystal is investigated. We then present the highly directive radiation from sources embedded in two-dimensional photonic crystals. The manifestation of novel and intriguing optical properties of photonic crystals are exemplified experimentally by the negative refraction and the focusing of electromagnetic waves through a photonic crystal slab with subwavelength resolution.

General information
Publication status: Published
MoE publication type: A1 Journal article-refereed
Organisations: Bilkent University
Contributors: Ozbay, E., Bulu, I., Aydin, K., Caglayan, H., Guven, K.
Number of pages: 9
Pages: 87-95
Publication date: Oct 2004
Peer-reviewed: Yes

Publication information
Journal: Photonics and Nanostructures - Fundamentals and Applications
Volume: 2
Issue number: 2

ISSN (Print): 1569-4410
Ratings:

Scopus rating (2004): SJR 1.381 SNIP 1.278
Original language: English
ASJC Scopus subject areas: Electronic, Optical and Magnetic Materials, Atomic and Molecular Physics, and Optics, Condensed Matter Physics, Hardware and Architecture, Electrical and Electronic Engineering
Keywords: Coupled cavity waveguide, Left-handed material, Negative refraction, Photonic crystal, Spontaneous emission
DOIs:

10.1016/j.photonics.2004.08.001
URLs:

http://www.scopus.com/inward/record.url?scp=4544365267&partnerID=8YFLogxK (Link to publication in Scopus)

Bibliographical note

EXT="Caglayan, Humeyra"
Source: Scopus
Source ID: 4544365267
Research output: Contribution to journal › Article › Scientific › peer-review