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## Abstract

Inkjet printed metal micropillars have been developed to help meet the demands for novel and highly adaptable microelectronics fabrication processes. The digitally printed silver pillar arrays in this study have been utilized in place of wafer-level solder bump processes or chip level wire-bonded stud bumps. These 3-dimensional silver pillars were printed with a drop-on-demand piezoelectric inkjet printer utilizing silver nanoparticle ink.

The inkjet printed micropillars were found to have 22 µm diameters and a height equivalent to approximately 3 µm per droplet. In our study, we chose pillars for further use as stud bumps with 8, 10, 12 and 14 droplets, with heights of approximately 20.9 µm, 25.9 µm, 33.3 µm and 35.9 µm respectively. After printing on the bare dies the bumps were subsequently used to increase the contact reliability of flip-chip bonded samples. It was found that the bumped chips dramatically improved the reliability of the I/O connection as compared to unbumped samples. In fact nearly 88 % of the bumped pads had a resistance less than 2.5 Ω/bump (no noticeable variation between bump heights) as compared to 17 % for the unbumped bare dies.

This study clearly demonstrates the fabrication of inkjet printed silver micropillars for use in uniform stud bump arrays. With the application of inkjet printed silver stud-bumps illustrating their feasibility in flip-chip fabrication methods.

Keywords: inkjet, printed electronics, microelectronics packaging, 3D printing, printed micropillars

## 1. Introduction

The world is evolving towards the Internet of Everything and Industry 4.0. This pursuit is creating the need to develop new agile manufacturing methods for electronics, especially with the growing need for more complex sensor networks. An alternative to traditional electronics manufacturing is to incorporate traditional silicon hardware with printed components in a hybrid electronics system [1]. These hybrid architectures involve fabrication methods that not only have the potential to decrease fabrication costs, but also increase form factor,

and functionality of printed electronic systems. To utilize the best of both worlds, a silicon based ASIC with high computational power can be integrated on plastic (flexible or stretchable) substrates with printed interconnects [2].

To reduce the package size and increase the level of miniaturization, flip-chip bonding can be utilized. In general, the flip-chip attachment method has a high level of efficiency as it involves the direct placement of components on the printed substrate whilst avoiding wire-bonding or packaging of the chips. This bonding method is highly effective for attaching surface-mount components (SMC) or bare dies on various substrates. The flip-chip process normally uses solder bumps on the chip pads to provide the chip-substrate interconnection, while using the solder or alternate underfill to provide the mechanical attachment. A method to avoid the use of solder bumps is to employ an anisotropically conductive adhesive (ACA) for chip-pad interconnections and mechanical adhesion. However, depending on the conditions, this process can be unreliable and therefore bumps are added to the chip pads to increase the reliability of the interconnection when using ACAs [1]. However, unlike wafer level bumping, stud bumping is performed on the chip-level which is particularly useful for novel chip designs and research purposes. However, stud-bumps are commonly fabricated with a wire bonder and have 50-70 µm diameters, limiting the pitch size of the chips, whereas digital printing should reduce the diameters and dramatically increase the versatility of the bumping process.

Inkjet printing has been used to digitally fabricate and print conductive metal three dimensional conductive metal microstructures [3], [4] and has seen applications in the fabrication of microelectromechanical systems (MEMS) [5]. In 2012, Sadie *et al*. explained how gold nanoparticle ink can be used to fabricate micropillars with the vision to replace solder bumps [6]. In their study, they were able to print gold pillars with feature sizes appropriate for traditional solder bump replacement utilizing a custom built drop-on-demand inkjet printer. Their work was further refined by evaluating various processing conditions (e.g. sintering) and compared to traditional bulk gold alternatives [7]. The average dimensions of the gold pillars was a height of 113 µm and 63 µm diameter; with the diameter of pillar being controlled primarily from the diameter of the initial droplet. To miniaturize the pillar size, electrohydrodynamic (EHD) printing has also been used for silver and gold nanoparticle inks to fabricate single micropillars and arrays [8]–[10]. Furthermore, studies at Tampere University of Technology investigated well defined silver pillars printed with EHD printing; however, for high throughput applications this method is not appropriate and much more time consuming than piezoelectric inkjet

printing [11]. Therefore, for applications with an increased pitch density we intend to preserve a small pillar diameter (10 – 20 µm), while maintaining a highly efficient inkjet fabrication process (piezoelectric in lieu of EHD printing).

In the current study, we evaluate the agile fabrication process of inkjet printing to fabricate metallic bumps using silver nanoparticle ink on bare dies for their flip-chip integration. As discussed previously, the goal is to evaluate an alternative to the traditional wafer-level bumping process (bumping every chip), which is particularly relevant for rapid prototyping and small series production. The digital printing of conductive bumps increases the versatility in the bumping process enabling customization on the single ASIC level.

## 2. Materials and equipment

### *2.1. Materials*

In this study, dummy chips with size of 3.85×3.85 mm with 80 aluminum pads (60×60 µm) on the periphery were used as the substrate for printing the stud bumps. Figure 1 shows a schematic side view of the chip.

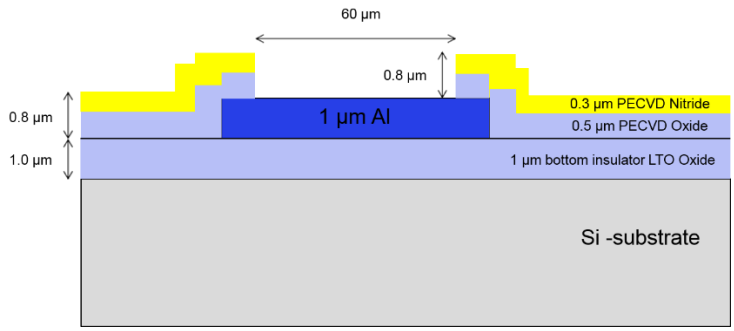


**Figure 1. Schematic side view of the chips used as the substrate.**

This work utilized symmetrical square chips with 80 I/Os (20 I/Os on each side) were selected for printing the stud-bumps on the designated pads at the top and bottom of the chips. Test chips have two daisy chains so that every second pad is connected together into the same chain. The pitch between the pads on the periphery of the chips was 200 µm. Figure 2 shows a schematic (left) and optical microscope image of the test chips (right).

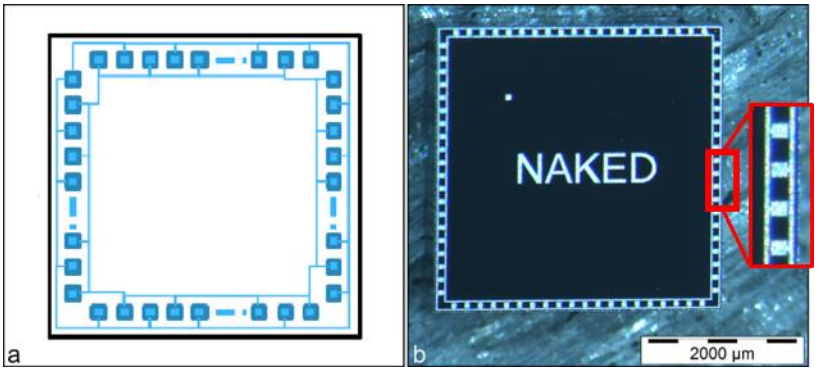


**Figure 2. Schematic (a) and optical microscope image (b) of the test chips with two daisy chains.**

Rigid printed circuit board (PCB) substrates were used for bonding to the test chips. The wiring structure shown in Figure 3 was fabricated using the lithography method on top of the FR4 PCB substrates (1.6 mm, FR4 material type DE104 from Isola) with Cu (18 µm)/Ni (4-5 µm)/Au (0.08-0.15 µm) conductors.

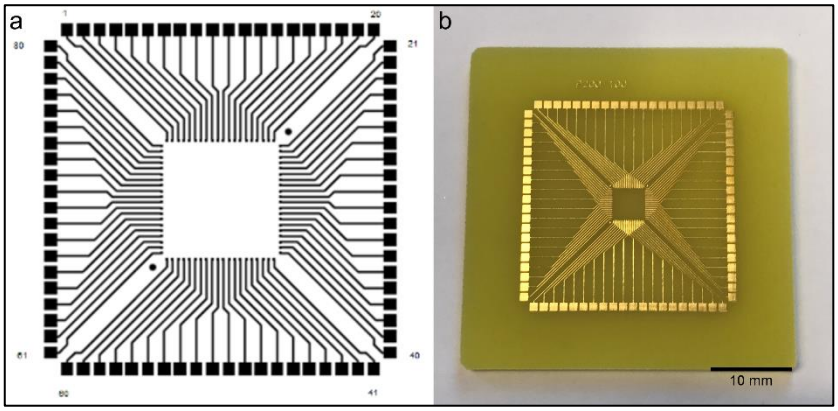


**Figure 3. (a) schematic and (b) photograph of printed wiring structure of the PCB substrates.**

An anisotropic conductive adhesive (ACF), Telephus TFA 22020 (40 µm thick), was used for bonding of the tests chips on top of the PCB substrates. The ACF contained 5 µm diameter Au/Ni coated polymer balls and has a recommended bonding temperature of 190 ℃ for 15 seconds.

NPS-J silver nanoparticle ink from Harima Chemicals, Japan was used to print the stud bumps. With Table 1 showing the reported specifications of the ink.

**Table 1. Specifications of the NPS-J silver nanoparticle ink from Harima Chemicals** [12].

| | |
|---|---|
| Particle size | Mean dia.12 nm |
| Metal contents | 63.1 wt% |
| Viscosity (Spiral viscometer/20 ℃/60 rpm) | 9 mPa·s |
| Specific gravity (g/ml at 20 ℃) | 1.93 |
| Solvent | Tetradecane |
| Curing conditions | 220 ºC (60 min) |
| Specific Resistance | 3 μΩ·cm |
| Shrinkage | 80 - 85% |

### *2.2. Fabrication equipment*

Commercial drop-on-demand Dimatix Material Printer (DMP-2831) with 10 pl cartridge was used to fabricate the 3D stud bumps. A Finetech fineplacer was used for performing the semi-automatic flip-chip bonding process with manually controlled placement and computer controlled temperature profile.

## 3. Fabrication process

In the first step, a printing pattern with the resolution of 1270 dpi (drop spacing 20 μm) was prepared to fabricate the stud bumps using the inkjet printer on two edges of the test chips. During the printing, the temperature of the printer platen was set to maximum 60 ºC in order to increase the evaporation rate of the wet droplets, which is necessary to fabricate 3D features. The temperature of 50 ºC was measured on the top of the chip. Since 50 ºC was not high enough to control the initial wetting on the pads, the surface of the test chips were treated with a thin layer of electronic grade coating (EGC) prior to printing. To achieve the appropriate concentration of EGC (2.5% 3M EGC-1720), the stock solution (3M EGC-1720; a fluorosilane polymer solution) was diluted with 3M HFE-7100 (methoxy-nonafluorobutane). This diluted EGC solution was subsequently used to decrease the wetting of the ink which enables the growing of the bumps (with a pillar-like shape) while the ink's solvent evaporates quickly. The effect of this kind of chemical surface treatment with different concentrations on the wetting and droplet diameter on the substrate is well studied in a paper by Mäntysalo and Mansikkamäki [13]. To illustrate the effectiveness of this phenomenon, Figure 4 shows that in case of not using any chemical treatment the first droplet wets the whole Al pad to a depth of 0.8 μm (see Figure 1) which is not suitable wetting to start the formation of pillars. However, with the chemical surface treatment, it is possible to have the necessary initial wetting (reduced drop diameter) to fabricate the pillars. To see the effect of the number of printed droplets on the bump height and their electrical resistance, different samples

were prepared by 8, 10, 12 and 14 droplets. Later all printed samples were sintered on top of the hot plate heated to 220 ºC for one hour as recommended by the ink manufacturer. It was experimentally determined that after sintering every droplet added approximately 3 µm in height to the bump pillars. Finally, the samples were cleaned by plasma ($O_2$ etch, 100 watt in 10 min) to remove the organic contamination from the surface of the chips as far as possible by ionized gas.

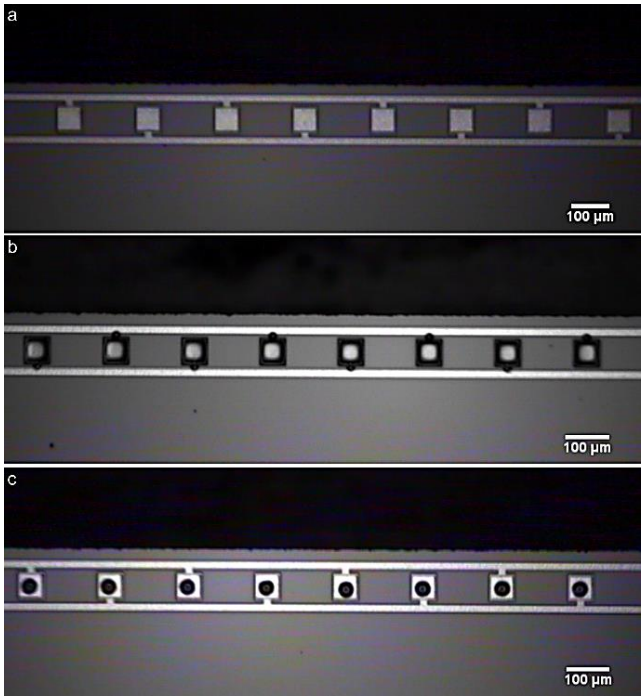


**Figure 4. Magnified images of the bare die edge with (a) Al pads before printing, (b) printed droplets on the Al pads with no surface treatment and (c) printed droplets on the Al pads with chemical surface treatment.**

After preparing the bumped test chips, a FinePlacer and ACF adhesive was used for flip-chip bonding. A portion of ACF adhesive was pre-bonded to the substrate (190 °C for 15 seconds) and then the FinePlacer was used to manually place the test chips on top of the PCB substrates (Figure 5).

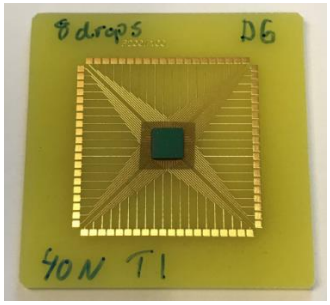

**Figure 5. Photograph of a bumped test chip bonded to the PCB substrate using flip-chip bonding.**

## 4. Results and discussion

The initial step during the optimization process of printing multiple consecutive silver bumps, was to ensure accurate alignment. Figure 6 illustrates the bumping of a complete ASIC systems

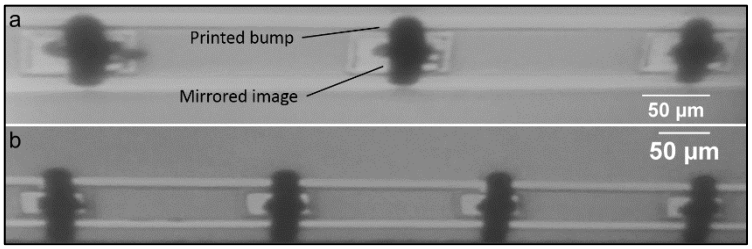


**Figure 6. Bird view images of printed bumps: (a) 10 droplets (b) 15 droplets.**

After optimizing the printing conditions and ensuring alignment accuracy, silver micropillars were digitally printed on the bare dies (to act as stud bumps). The SEM images of printed bumps with various heights are shown in Figure 7. Experimentally we found that the printed pillars all had the same average diameters of 22 µm with a height correlating to approximately 3 µm per droplet. These experimental values are in line with the theoretical pillar heights based on the ink solid content and specific gravity. To calculate the height of every droplet in theory, first, the volume of one droplet ($V$) after the solvent evaporation can be calculated by equation 1 ($m$: mass, $\rho$: density). Given the volume calculated from equation 1 (1150 µm$^3$) and radius ($r$) of 11 µm for dried pillars, the height ($h$) of dried droplets (3 µm) can be calculated. However, it must be noted that the first printed droplets just wet the substrate and do not really add to the height of the pillars. Next few droplets slowly form the base of the pillars with a smaller diameter and then next droplets add to the height of the pillars during the growth phase [7]. Therefore, in Figure 8 which shows the comparison of the theoretical and experimental pillar heights, first droplets are excluded for the calculation of theoretical pillar heights. It can be seen that the theoretical and experimental heights are almost the same except a slight difference for the pillars printed by 10 and 14 droplets, which can be attributed to the process variation that can affect the amount of solid content in the printed droplets. The nominal droplet size is 10 pl, but the actual size will vary according to used ink, waveform, temperature, and shooting voltage amplitude.

$$V = m / \rho \qquad (1)$$

$$h = V / \pi \times r^2 \qquad (2)$$

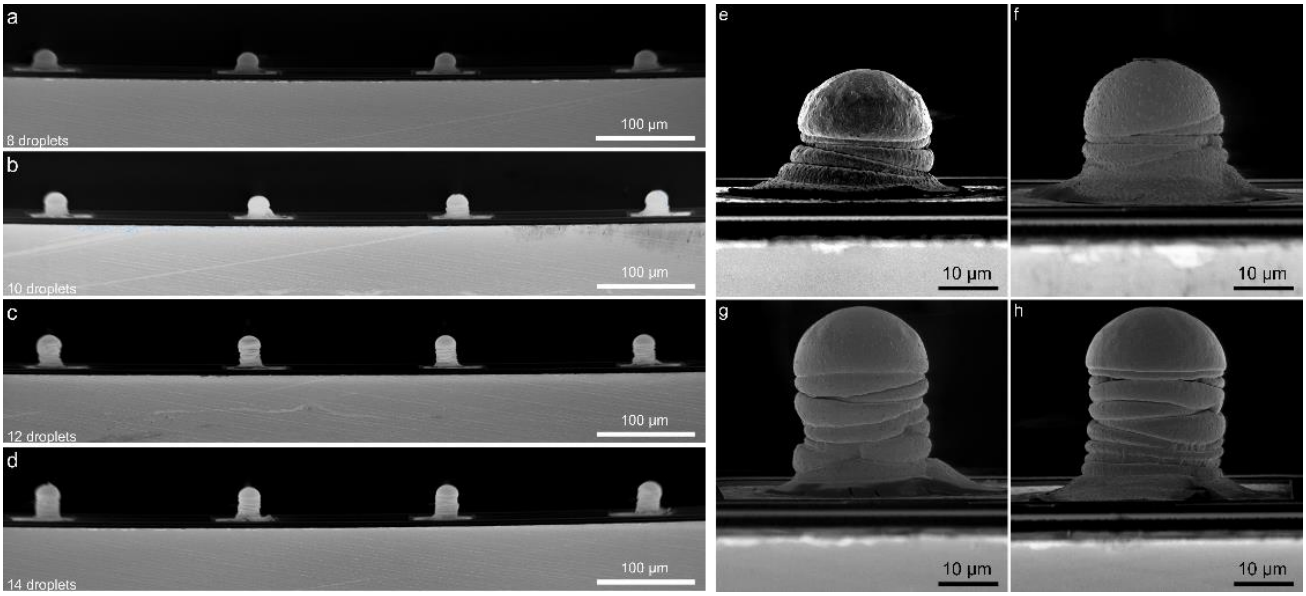


**Figure 7. SEM images of printed silver pillars on adjacent chips pads (left) with a) 8 droplets (20.9 ± 0.0 µm), b) 10 droplets (25.9 ± 0.8 µm), c) 12 droplets (33.3 ± 1.3 µm), d) 14 droplets (35.9 ± 1.1 µm), and the magnified single pillar (right) of e) 8 droplets (22.4 µm), f) 10 droplets (24.7 µm), g) 12 droplets (31.8 µm), h) 14 droplets (33.0 µm).**

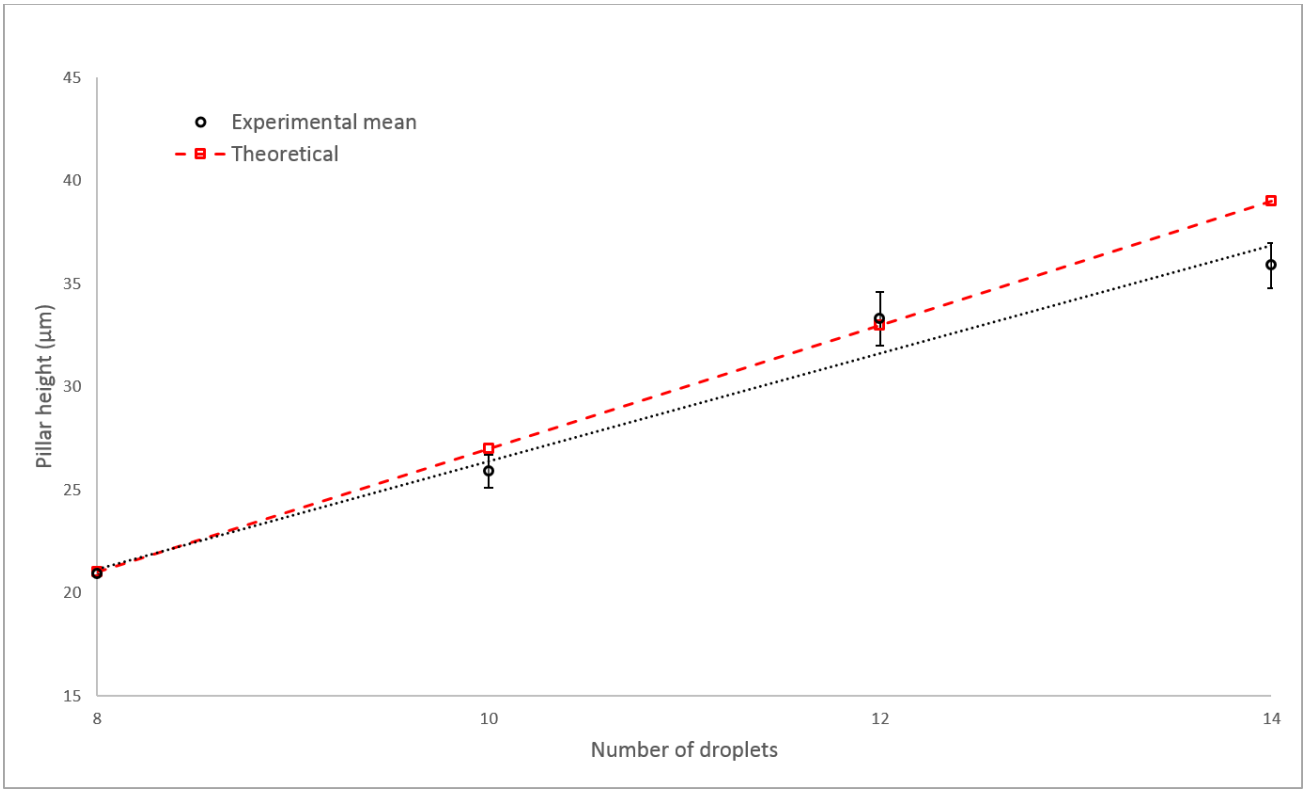


**Figure 8. Comparison of the theoretically calculated and experimental heights of the inkjet printed silver pillars.**

Following the chip-PCB bonding procedure of the bare-dies with printed bumps, resistance between the connected pad pairs on the PCB were measured (1-3, 2-4, 3-5, etc.). In addition to the bumped chips, two

reference chips with no bumps were electrically tested with the same method in order to elucidate the effect of the inkjet printed bumps. Next, the cumulative distribution of the measured resistance values for samples with and without bumps was plotted to study the results as shown in Figure 9. There is a similarity in the shape of the distribution for both bumped and un-bumped cases; however, the variation is relevant. After approximately 40 Ω both graphs are nearly flat with both bumps and un-bumped chips, this plateau eventually correlates to approximately 10 % of all chip pads having an open circuit. For the bumped case, there is a sharp distribution smaller than 5.0 Ω focused on 1.2 Ω but with no bump we see a wider range of values more equally distributed.

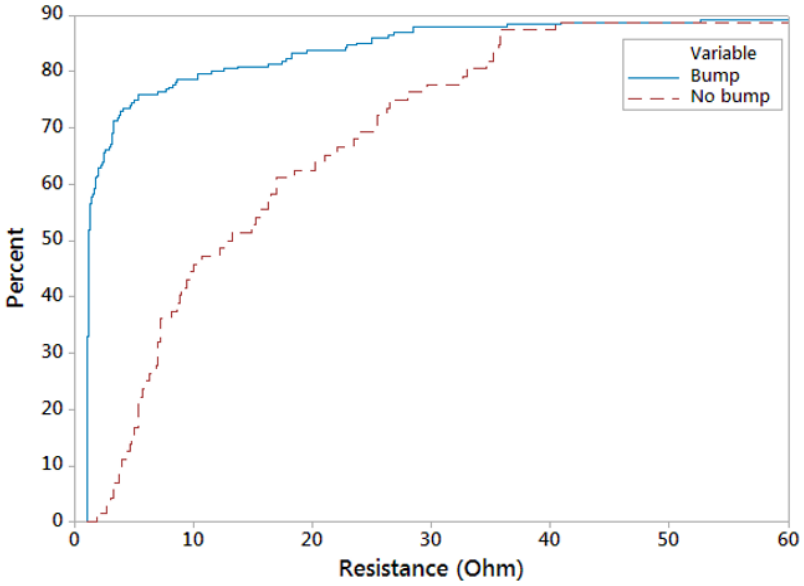


**Figure 9. Cumulative distribution of measured resistance values of the bonded samples with and without the printed bumps.**

It was noted that the data must be analyzed in more detail, since just one failed connection on one pad can show an open circuit or a very high resistance for a pair of pads. Therefore, resistance measurement for the pairs cannot be enough and a classification must be utilized. Hence, based on the graphs, it was decided to classify the performance as: 1) good (<5.0 Ω/pair; 2.5 Ω/bump + trace), 2) poor (5-60 Ω) and 3) Failure/open circuit (>60 Ω). Considering the available data, 5.0 Ω was decided by the authors to be able to do the classification presented in Figure 10. Most of the open circuits were found in the corners of the chips where the lines in the very corner cannot properly be aligned and connected to the pads on the chips. This failure comes from the PCB design, which has shorter corner lines to avoid line contact during the lithographic process (Figure 11). Therefore, the values from the corners were taken out of the data. By excluding the bumps on the corners, the

number of open circuits decreases from ~8 % to ~2 % and poor connections from ~12 % to ~10 %. In the case of the bonding with no bumps, after excluding the corner pads from the data, the number of open circuits decreases by ~3 %.

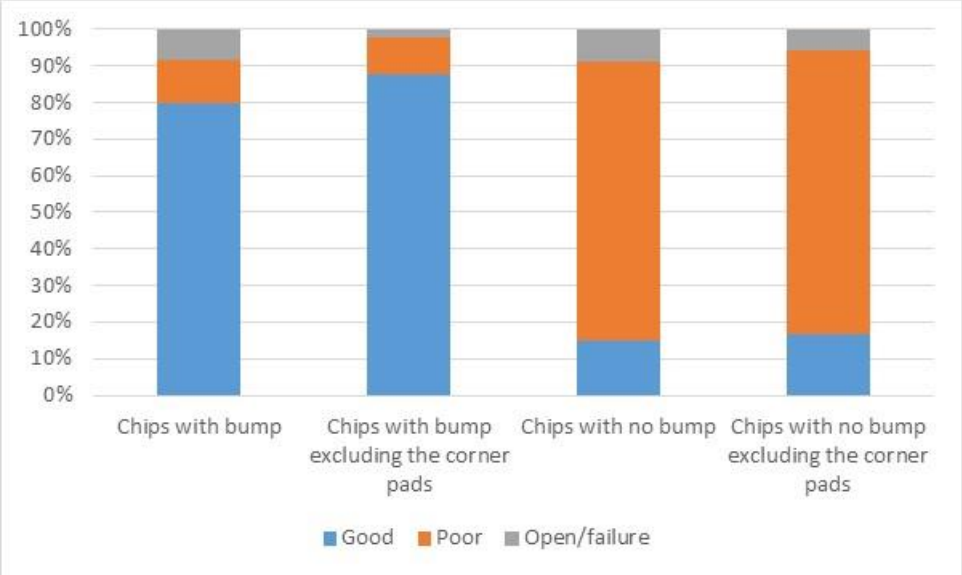


**Figure 10. Proportion of I/O connection performance [1) good (<5 Ω/pair; 2.5 Ω/bump + trace), 2) poor (5-60 Ω) and 3) Failure/open circuit (>60 Ω)] for bonded samples with or without the printed bumps.**

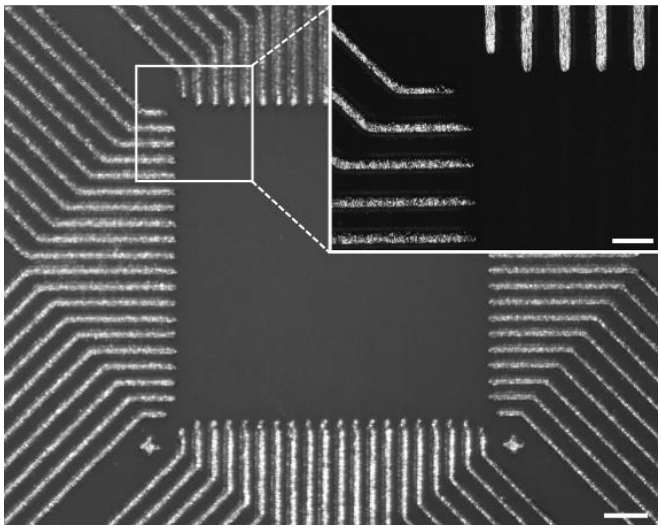

**Figure 11. Microscopic image detailing the reduced line lengths of the corner PCB paths (scale bar length = 500 µm; 200 µm for inset).**

The authors could not find any correlation between the drop count and resistance. The reason is that the height variation of the printed bumps is extremely small compared to the other factors that affect the resistance. In addition, it was noted that the bump height does not affect the failure rate.

## 5. Conclusion

This study has demonstrated the application of inkjet printed silver 3D bumps and illustrated their potential use in flip-chip fabrication methods. The inkjet printed silver pillars showed a high level of uniformity and reproducibility. Furthermore, the inkjet printed micropillars were found to have 22 µm diameters and a height equivalent to approximately 3 µm per droplet.

With the printed bumps the flip-chip bonded bare dies had a much higher contact reliability than the unbumped reference samples. Specifically, nearly 88 % of the bumped pads had a resistance <2.5 Ω/bump, with little variation between bump heights, as compared to 17 % for the unbumped bare dies.

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