Linearization of BJTs with logarithmic predistortion

Linearization of BJTs with Logarithmic Predistortion

Olli-Pekka Lundén and Timo Paldanius

Tampere University of Technology, Tampere, Finland, olli-pekka.lunden@tut.fi, +358 40 849 0098

***Abstract*— This paper proposes a novel linearization technique for bipolar junction transistors (BJT) and their derivatives, e.g., heterojunction BJTs. Since the non-linearity of BJTs is exponential by nature, analog predistortion caused by a logarithmic amplifier should linearize the response completely, in theory. This paper reports that, in practice, cascading a logarithmic amplifier in front of a simple one-transistor BJT amplifier boosted its output third-order intermodulation intercept point (OIP3) by 10 dB. The proposed linearization scheme is extremely simple and it is inherently broadbanded. To the best of our knowledge, this idea has not been reported previously.**

***Index Terms*— analogue predistortion, nonlinearity, power amplifer, linearization techniques, logarithmic amplifier, log amplifier**

I. Introduction

Needs for amplifier linearization have come about in various branches of RF and microwave electronics, such as radio transceivers and radar. Much of the recent progress has been reviewed in [1].

Both analog and digital linearization techniqus have been developed with greatly varying complexity and performance. Digital linearizers, with an (almost) real-time control by microprocessors, are superior in their ability to adapt to varying operating conditions of the nonlinear amplifier. However their practical realizations tend to be relatively complex. Also the dc power consumption of their signal processing part can be of concern, especially in low-power applications. Many analog linearization schemes such as feedforward, cartesian feedback, and predistortion schemes, suffer from high complexity; and their bandwidths are often limited. On the other hand, some previously reported analog predistorton designs have been extremely simple, such as a cascode-FET stucture [2] or a diode with a parallel capacitor [3].

In general, the idea of analog predistortion is to deliberately distort the signal in a predefined way before applying it to the main amplifier. The distortion caused by the predistorter should be the "opposite" of the distortion caused by the main amplifier so that, in the end, the signal is free of distortion. This paper proposes a novel and simple technique to linearize bipolar junction transistors and alike.

II. The BJT Linearization Scheme

Devices that show exponential nonlinearity, such as BJTs and HBTs, can be linearized using *logarithmic* predistortion. We propose a predistortion scheme depicted in Fig. 1, where the transistor Q2 is the amplifier to be linearized. This transistor is preceeded by a logarithmic amplifier [4] with a diode-connected transistor Q1 as the feedback element. In the following discussion, this predistortion scheme is analyzed by employing the well-known Ebers-Moll transistor model [5].

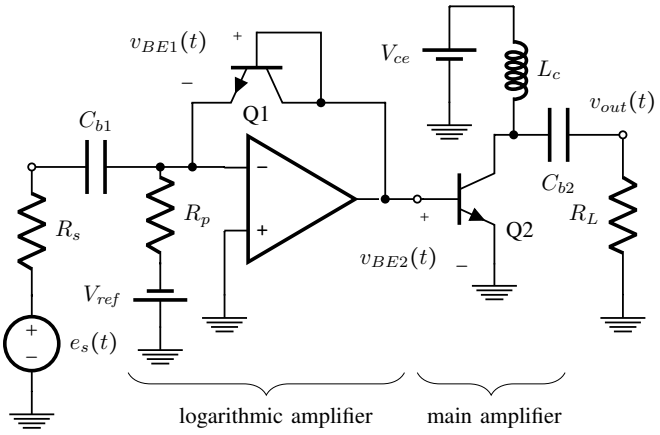

Fig. 1. In the proposed linearization scheme, a logarithmic amplifier creates analogue (RF) predistotion before a BJT amplifier.

The opamp feedback current, i.e., the emitter current $i_{E1}(t)$ of Q1, relates to the base-to-emitter voltage $v_{BE1}(t)$ according to the Shokley equation

$$i_{E1}(t) = I_{s1}\left(\exp\frac{v_{BE1}(t)}{n_1 V_T} - 1\right), \tag{1}$$

which can be written

$$\frac{v_{BE1}(t)}{V_T} = n_1 \ln\left(\frac{i_{E1}(t)}{I_{s1}} + 1\right), \tag{2}$$

where I_{s1} is the reverse saturation current and n_1 the ideality factor of the base-to-emitter pn-junction, while $V_T = qT/k$ is the thermal voltage, with elementary charge q, absolute temperature T , and Boltzmann constant k.

The opamp keeps the potential of its negative input practically at zero because its positive input is grounded. Hence the opamp output voltage is close to $v_{BE1}(t)$. Moreover, since the opamp output connects directly to the base of Q2,

$$v_{BE1}(t) \approx v_{BE2}(t). \tag{3}$$

As the amplifying transistor Q2 is biased to its active region, its collector current can be modeled as [5]

$$i_{C2}(t) = \alpha_{f2} I_{s2} \left(\exp \frac{v_{BE2}(t)}{n_2 V_T} - 1 \right), \tag{4}$$

where α_{f2} is the forward α-current gain of Q2, I_{s2} its base-to-emitter reverse saturation current, and n_2 its ideality factor. Now, using (2) and (3), this can be written

$$i_{C2}(t) \approx \alpha_{f2} I_{s2} \left[\exp \left(\frac{n_1}{n_2} \ln \left(\frac{i_{E1}(t)}{I_{s1}} + 1 \right) \right) - 1 \right] \tag{5}$$

$$= \alpha_{f2} I_{s2} \left[\left(\frac{i_{E1}(t)}{I_{s1}} + 1 \right)^{\frac{n_1}{n_2}} - 1 \right] \tag{6}$$

If $n_1 \approx n_2$, the equation simplifies to

$$i_{C2}(t) \approx \alpha_{f2} \frac{I_{s2}}{I_{s1}} i_{E1}(t) \tag{7}$$

showing that the collector current of Q2 is linearly proportional to the emitter current of Q1.

Going back to Q1, the emitter current $i_{E1}(t)$ of that transistor is partly sinked into the dc voltage source V_{ref} (note the polarity) through R_p, and, partly into the ac voltage source $e_s(t)$ through R_s, as the opamp negative input draws none of this current. The current splits into ac and dc components as

$$i_{E1}(t) = \underbrace{I_{e1}}_{\text{dc}} + \underbrace{i_{e1}(t)}_{\text{ac}} = \underbrace{\frac{V_{ref}}{R_p}}_{\text{dc}} - \underbrace{\frac{e_s(t)}{R_s}}_{\text{ac}}. \tag{8}$$

The dc component of $i_{E1}(t)$ flows through R_p and the ac component through R_s. There is no significant ac through R_p because each end of it are at constant potentials.

III. AC Operation

Due to the decoupling capacitor C_{b2} and the RF choke L_c, the output current $i_{out}(t)$ through R_L is the negative of the ac component of $i_{C2}(t)$, which is obtained from (7) and (8) as

$$i_{out}(t) = -i_{c2}(t) = -\alpha_{f2} \frac{I_{s2}}{I_{s1}} i_{e1}(t) = \alpha_{f2} \frac{I_{s2}}{I_{s1}} \frac{e_s(t)}{R_s}. \tag{9}$$

Thus the output voltage across R_L is

$$v_{out}(t) = i_{out}(t) R_L = \alpha_{f2} \frac{I_{s2}}{I_{s1}} \frac{R_L}{R_s} e_s(t). \tag{10}$$

If the reverse saturation currents are approximately equal ($I_{s1} \approx I_{s2}$) and if the current gain is high ($\alpha_{f2} \approx 1$) then

$$v_{out}(t) \approx \frac{R_L}{R_s} e_s(t) \tag{11}$$

This means that, regardless of the load or source resistances, the load current, given by $i_{out}(t) = v_{out}(t)/R_L$, always equals the source current $i_s(t) = e_s(t)/R_s$. Hence, the current gain of the system is unity. As the input voltage at the negative input is practically zero, voltage gain is infinite, in theory. The input impedance is almost zero.

In case of sinusoidal drive $e_s(t) = \hat{e}_s \cos(\omega t)$ and $v_{out}(t) = \hat{v}_{out} \cos(\omega t)$. By the general definition [6], transducer power gain is

$$G_T = 10 \log \frac{P_L}{P_{avg}} \text{ (dB)}, \tag{12}$$

where the power delivered to the load is $P_L = \hat{v}_{out}^2/(2R_L)$ and the power available from the source is

$$P_{avg} = \frac{\hat{e}_s^2}{8R_g}. \tag{13}$$

Combining (11), (12), and (13) yields the transducer power gain of the linearized system:

$$G_T = 10 \log \frac{\hat{v}_{out}^2/(2R_L)}{\hat{e}_s^2/(8R_s)} = 10 \log \frac{4R_L}{R_s} \text{ (dB)}. \tag{14}$$

This gain expression was derived without small-signal approximations, therefore, it is the small-signal *and* the large-signal gain. Surprisingly, G_T of the linearized system is determined by the termination resistances, only. It is completely independent of transistor parameters.

$G_T = 6$ dB when $R_L = R_s$. However, G_T increases by 3 dB for every doubling of the load resistance or halving of the source resistance.

IV. DC Operation and Power Consumption

From (3) it follows that for nearly identical transistors with $I_{s1} \approx I_{s2}$, $\alpha_{f1} \approx \alpha_{f2}$, and $n_1 \approx n_2$, the dc collector currents are nearly equal:

$$I_{c2} \approx I_{c1} \approx I_{e1} = \frac{V_{ref}}{R_p} \tag{15}$$

Those can be adjusted by either V_{ref} or R_p. In theory Q2 needs no additional base bias network and the currents are automatically equal. (In practise their dc values may differ considerably.) The collector currents depend *linearly* on V_{ref}. The total dc power consumption of the system comes from three constituents: collector currents of each transistor and the opamp quiescent current.

V. Verification

The proposed system was constructed from a matched transistor pair BFM520 and a low-cost operational amplifier AD8055. Testing was done at a comparably low frequency, 3.3 MHz, firstly because of the frequency limitations of the AD8055, and secondly, because the purpose of the testing was only to proove the concept. An LC high-pass impedance matching circuit consisting of an 8-μH shunt inductor and a 320-pF series capacitor was used to transform the 50-Ω external load into an effective load of $R_L \approx 500\ \Omega$ at 3.3 MHz. For simplicity, no impedance matching were used on the generator side, thus, $R_s = 50\ \Omega$. According to (14), expected gain is then 16 dB. The dc currents of Q1 and Q2 were set to 5 mA while V_{ce} of Q2 was 3 V.

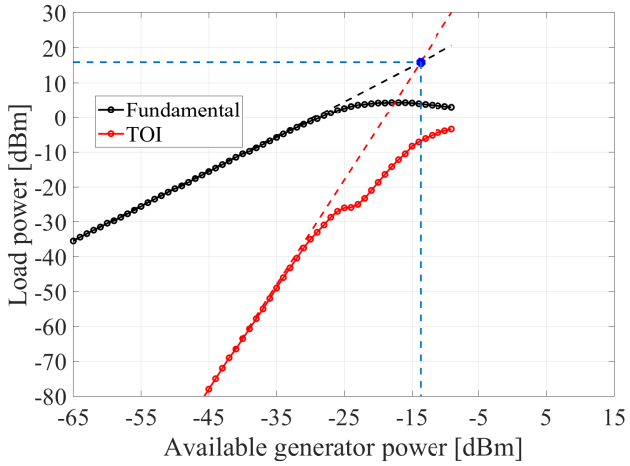

Fig. 2. Measured two-tone performance of the *BJT amplifier alone*. At −5 dBm output power, the third-irder intermodulation (TOI) products are -46 dBc below the carriers. OIP= 17 dBm.

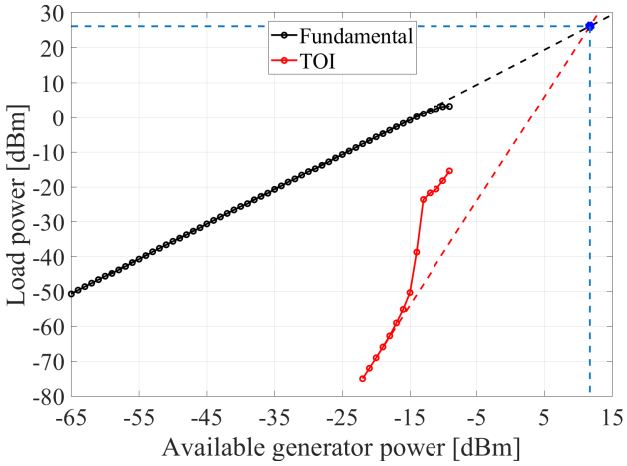

Fig. 3. Measured two-tone performance of the *linearized system*. At −5 dBm output power, the third-order intermodulation products are -66 dBc below the carriers. OIP= 27 dBm.

A. Stability of the real system

Keeping the system stable was a practical challenge. We noticed that a diode-connected transistor, with high enough transsusceptance, can be unstable. This finding is not supported by all prior studies [4, p. 119]. For achieving unconditional stability, a 27-Ω resistor was added in series with the Q1 collector. Simulation (see next sub-section) showed that the resistor has little effect on anything else.

Further, Q2 was stabilized against high-frequency oscillation using standard procedures [6, p. 228] with added frequency selectivity: a series RC circuit from the base and from the collector to the ground stabilized the device against the tendency to oscillate at high frequencies. These additions had negligible effects at 3.3 MHz.

B. Simulated and measured gain

It is straightforward to simulate the proposed system (Fig. 1), for instance, using Keysight ADS, as we did. Simulations showed 16-dB gain, as expected, for R_L/R_s = 10. However, the actually measured gain was only 12 dB. To find out the reason, we developed the simulation circuit model to include elements that describe non-ideal performance. The step-wise process revealed that the lacking 4 dB was mostly due to our RF inductor performance.

C. Suppression of intermodulation distortion

Intermodulation distortion testing (IMD, [7]) was performed for both, the transistor alone (Fig. 2), and the linearized transistor (Fig. 3). The IMD test of Q2 alone shows OIP3 of 16 dBm, whereas the IMD test of the linearized transistor shows OIP3 of 26 dBm. Thus, the linearization has increased the OIP3 by 10 dB. For output power levels below −5 dBm, the third-order intermodulation products of the linearized transistor are 20 dB lower than they are for the transistor alone.

VI. Conclusion

This paper proposed a novel linearization technique for the exponential nonlinearity of BJT-like transistors by using logarithmic predistortion. In this technique the amplifier output voltage $v_{out}(t)$ is a linear function (10) of the signal source electromotive force $e_s(t)$, in theory.

The proposed technique is novel, much simpler than many of the previously presented techniques, and inherently broadbanded. Such things as impedance matching or the operational amplifier gain-bandwidth product may limit the system bandwidth in practice. The efficacy of the system depends also on how identical the transistors are.

The measurements done at 3.3 MHz show the technique is actually feasible. The OIP3 was boosted by 10 dB and intermodulation products were suppressed by 20 dB. One may expect the technique works also at higher frequencies.

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