An enumeration-based model predictive control strategy for the cascaded H-bridge multilevel rectifier

An Enumeration-Based Model Predictive Control Strategy for the Cascaded H-Bridge Multilevel Rectifier

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***Abstract*—In this paper, a model predictive control (MPC) strategy is adapted to the cascaded H-bridge (CHB) multilevel rectifier. The proposed control scheme aims to keep the sinusoidal input current in phase with the supply voltage, and to achieve independent voltage regulation of the H-bridge cells. To do so, the switches are directly manipulated without the need of a modulator. Furthermore, since all the possible switching combinations are taken into account, the controller exhibits favorable performance not only under nominal conditions, but also under asymmetrical voltage potentials and unbalanced loads. Finally, a short horizon is employed in order to ensure robustness; in this way the required computational effort remains reasonable, making it possible to implement the algorithm in a real-time system. Experimental results obtained from a two-cell CHB rectifier are presented in order to demonstrate the performance of the proposed approach.**

***Index Terms*—Cascaded H-bridge multilevel rectifier, model predictive control, optimal control.**

I. Introduction

AMONG the multilevel converters, the cascaded H-bridge (CHB) embodies the qualities of the most attractive topology in comparison to the neutral point clamped (NPC) and the flying capacitor (FC). The reasons for this are the reduced number of the switching devices, as well as its high modularity [1]. However, several issues are still open, specifically, when the topology is operated as a multilevel rectifier. In this mode of operation, the CHB rectifier aims to achieve n isolated dc buses, each of which may perform independently from the others, resulting in the need for more complex control strategies. In addition, the converter has to operate always under unity power factor with minimum power losses, while at the same time respecting the operational limits imposed by the topology [2]. Thus, numerous research works have been reported in literature.

Particularly, several algorithms have been developed to meet most of the control goals. A high percentage of them rely on the multicarrier approach [3], [4] which gives the benefit of constant switching frequency. Others use conventional [5] or generalized [6] modulation methods with low computational complexity exhibiting noteworthy performance. Furthermore, advanced control techniques have been employed in order to achieve various performance objectives, such as robustness and model parameter estimation. Specifically, for purposes of robustness, the sliding mode control [7], and the hysteresis current control [8] are more suitable, while for the estimation of the model parameters the adaptive-passivity control [9] is ideal. For switching frequency reduction and power losses minimization selective harmonic elimination pulse width modulation (SHE-PWM) control [10] is very promising.

Despite the effectiveness of the existing control approaches, there are still open tasks such as ease of controller design and elimination of tuning. Furthermore, the rapid development of fast microprocessors enabled the application of computationally demanding algorithms, such as model predictive control (MPC) [11], to the field of power electronics. Over the last years many works have been presented demonstrating the advantages of this control strategy [12]–[18], including works about the CHB converter operated as either an inverter [19], [20], or as a rectifier [21], [22].

MPC thanks to its straightforward implementation has achieved a lot of popularity [23]. An objective function that incorporates the control objectives is formulated based on the mathematical model of the converter and it is minimized over the finite prediction horizon. The underlying optimization problem is solved in real-time; the optimal solution at each sampling instant is the sequence of control inputs that results in the best predicted behavior of the system. Only the first element of the optimal sequence is implemented. At the next step all the variables are shifted by one sampling interval and the complete procedure is repeated. This strategy, known as *receding horizon policy*, is employed in order to provide feedback [24].

In this work an MPC scheme for the CHB multilevel rectifier consisting of n cells is proposed, as the one in [25], and it is presented in more detail. In the inner loop, posed in the MPC framework, the input current is regulated to its sinusoidal reference by directly manipulating the switches of the converter. An exhaustive search of all the possible switching combinations takes place resulting in a controller which is suitable to predict the behavior of the plant for the whole operation range. Furthermore, and in order to maintain

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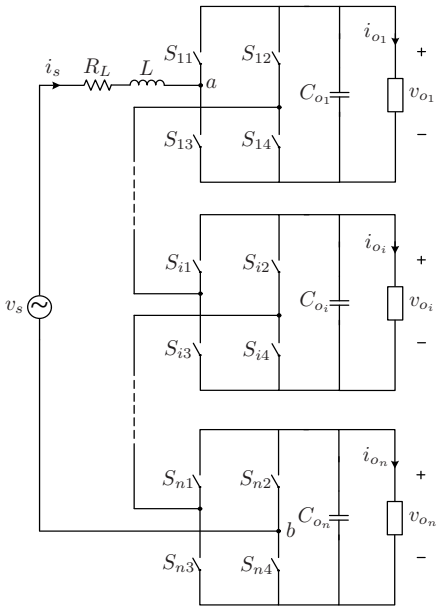


Fig. 1. Topology of the single-phase CHB multilevel rectifier consisting of n cells connected in series.

the effectiveness of the controller during transients and to enhance the dynamic behavior of the system, the deviation of the respective voltages from their references is taken into account. In this way the controller aims to reject all kind of disturbances, including load and output voltage variations.

A key benefit of the proposed algorithm is that despite its design simplicity it is capable of stabilizing the system over the entire operating regime. Furthermore, the control objectives are expressed in the objective function in a straightforward manner; in this way excessive tuning is avoided. Other advantages include the fast dynamics achieved by MPC. On the other hand, the absence of a modulator and the direct manipulation of the converter switches imply a variable switching frequency. Moreover, the dominant drawback is that the computational power needed increases exponentially when the prediction horizon is extended further into the future. However, control design issues related to the computational complexity are presented and solutions to address them are proposed.

This paper is organized as follows. In Section II the discrete-time model suitable for the controller is derived. The control objectives, the formulation of the optimization problem, and the proposed approach are presented in Section III. The control algorithm and computational issues are discussed in Section IV. Section V evaluates the performance of the proposed control approach by means of experimental results. Finally, the paper is summarized in Section VI, where conclusions are drawn.

II. Model of the Cascaded H-Bridge Multilevel Rectifier

The topology of the CHB rectifier with n cells connected in series is illustrated in Fig. 1. The ac side consists of a boost inductance L, with internal resistor R_L. At the dc side each cell consists of a filter capacitor C_{o_i}, where $i \in \{1, 2, \ldots, n\}$ denotes the number of the cell, connected in parallel with the load.

TABLE I
Switching States of a Single-Phase Cascaded H-Bridge Multilevel Rectifier Consisting of n Cells and ac Side Voltage v_{ab}

$T_{11}T_{12}$		$T_{i1}T_{i2}$		$T_{n1}T_{n2}$	v_{ab}
††	$\cdots$	10	$\cdots$	10	$\sum_{\zeta\in\mathcal{H}} v_{o_\zeta}$
10	$\cdots$	††	$\cdots$	01	$\sum_{\zeta\in\mathcal{H}} v_{o_\zeta} - \sum_{\xi\in\mathcal{L}} v_{o_\xi}$
††	$\cdots$	††	$\cdots$	††	$0,\ i \in \mathcal{O}$
††	$\cdots$	01	$\cdots$	01	$\sum_{\xi\in\mathcal{L}} -v_{o_\xi}$
$\mathcal{H} = \{\zeta \in \mathbb{N}^* \mid \zeta \le n,\ T_{\zeta 1}T_{\zeta 2} = 10\}$					
$\mathcal{L} = \{\xi \in \mathbb{N}^* \mid \xi \le n,\ T_{\xi 1}T_{\xi 2} = 01\}$					
$\mathcal{O} = \{1, 2, \ldots, n\}$					

TABLE II
Switching States of a Single-Phase Cascaded H-Bridge Multilevel Rectifier Consisting of Two Cells and ac Side Voltage v_{ab}

$T_{11}T_{12}$	$T_{21}T_{22}$	v_{ab}
10	10	$v_{o_1} + v_{o_2}$
10	††	v_{o_1}
††	10	v_{o_2}
10	01	$v_{o_1} - v_{o_2}$
01	10	$v_{o_2} - v_{o_1}$
††	††	0
††	01	$-v_{o_2}$
01	††	$-v_{o_1}$
01	01	$-v_{o_1} - v_{o_2}$

Each H-bridge cell is composed of four switches S_{ij}[1], where $j \in \{1, \ldots, 4\}$ refers to the respective switch of the cell. The switches of each cell operate dually and in pairs denoted by T_{ip}, with $p \in \{1, 2\}$; the odd indexed switches (S_{i1} & S_{i3}) form one pair ($p = 1$) and the even indexed (S_{i2} & S_{i4}) the other ($p = 2$). Furthermore, when the upper switch of the pair of the ith cell T_{ip} is *off*, then $T_{ip} = 0$; when it is *on*, then $T_{ip} = 1$. In Table I the switching combinations for an n-cell CHB rectifier and the resulting reflected multilevel voltage to the ac side are summarized. The symbolism "††" stands for the case where the switching states T_{ip} of both pairs of the ith cell are the same, i.e. $T_{i1}T_{i2} = 00$ or $T_{i1}T_{i2} = 11$. Moreover, in Table II the switching combinations and the corresponding level of the voltage v_{ab} for a two-cell CHB rectifier are summarized.

The MPC controller is built around the discrete-time state-space model of the converter, which is derived by discretizing the continuous-time model using the forward Euler approximation approach. This yields:

$$x(k+1) = A_d(u)x(k) + B_d w(k) \tag{1a}$$

$$y(k) = C_d x(k)\,, \tag{1b}$$

where the matrices are $A_d(u) = (\mathbb{I} + A_1 T_s + A_2 T_s u(k))$, $B_d = T_s B$, and $C_d = C$, where $\mathbb{I}$ is the identity matrix and

[1]Usually each switch is composed of an IGBT and an anti-parallel freewheeling diode.

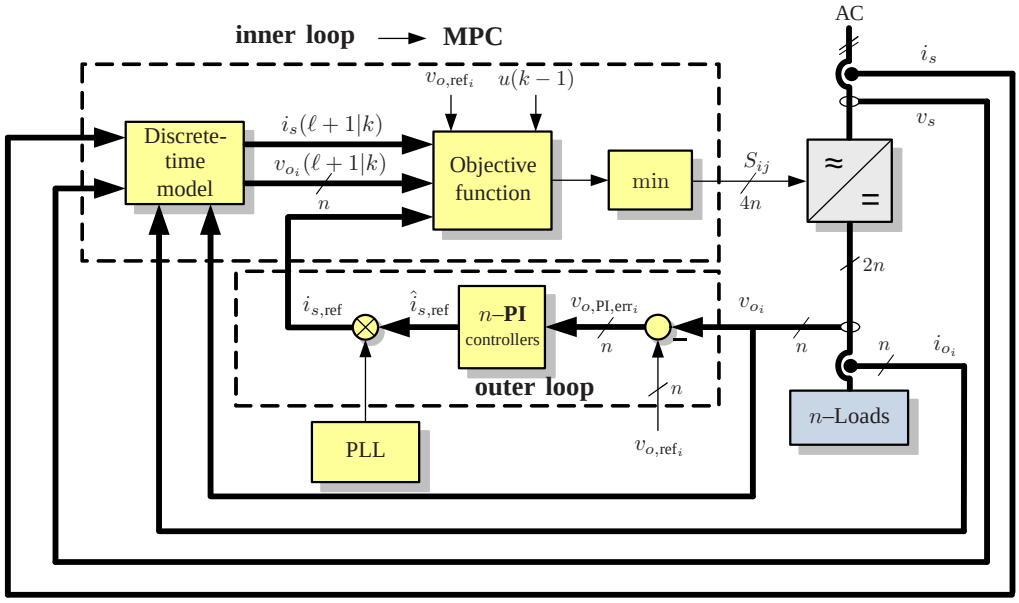


Fig. 2. Block diagram of the proposed model predictive control (MPC) scheme.

T_s is the sampling interval. In (1)

$$x(k) = \begin{bmatrix} i_s(k) & v_{o_1}(k) & \dots & v_{o_n}(k) \end{bmatrix}^T , \tag{2}$$

is the state vector, encompassing the inductor current and the output voltages of the individual cells. The input matrix $u(k) \in \mathbb{R}^{m\times m}$, with $m = n+1$, is given by

$$u(k) = \begin{bmatrix} d_{11} & 0 & \cdots & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \ddots & \vdots \\ d_{i1} & 0 & \cdots & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \ddots & \vdots \\ d_{n1} & 0 & \cdots & 0 & \cdots & 0 \\ 0 & d_{m2} & \cdots & d_{mi+1} & \cdots & d_{mn+1} \end{bmatrix} , \tag{3}$$

where the entries of the matrix are

$$d_{i1} = d_{mi+1} = u_{i1} - u_{i2} \, . \tag{4}$$

The binary variable $u_{ip} \in \{0,1\}$ is introduced in order to model the switching state of each dually operated pair of switches T_{ip}; $u_{ip} = 1$ refers to the case where $T_{ip} = 1$, and $u_{ip} = 0$ to the case being $T_{ip} = 0$. The input voltage $v_s(k)$ and the load current $i_{o_i}(k)$ of each cell form the vector of the disturbances $w(k) = [v_s(k)\ i_{o_1}(k)\ \dots\ i_{o_n}(k)]^T$, while the respective output voltages are considered as the output, i.e.

$$y(k) = \begin{bmatrix} v_{o_1}(k) & \dots & v_{o_n}(k) \end{bmatrix}^T . \tag{5}$$

Finally, the matrices A_1, A_2, $B \in \mathbb{R}^{m\times m}$ and $C \in \mathbb{R}^{n\times m}$ are given by

$$A_1 = \begin{bmatrix} -\frac{R_L}{L} & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 \end{bmatrix} , \tag{6}$$

$$A_2 = \begin{bmatrix} 0 & 0 & \cdots & 0 & -\frac{1}{L} \\ \frac{1}{C_{o_1}} & 0 & \cdots & 0 & 0 \\ 0 & \frac{1}{C_{o_2}} & \ddots & \vdots & \vdots \\ \vdots & & \ddots & 0 & 0 \\ 0 & \cdots & 0 & \frac{1}{C_{o_n}} & 0 \end{bmatrix} , \tag{7}$$

$$B = \mathrm{diag}\Big(\frac{1}{L}, -\frac{1}{C_{o_1}}, \dots, -\frac{1}{C_{o_{(n-1)}}}, -\frac{1}{C_{o_n}}\Big) , \tag{8}$$

$$C = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & 0 & \cdots \\ \vdots & \vdots & \ddots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 & 1 \end{bmatrix} . \tag{9}$$

III. Control Problem and Approach

In this section an MPC scheme for the CHB multilevel rectifier is introduced. The variables of concern are controlled by directly manipulating the switches of each cell, thus a modulator is not required. The proposed control algorithm is shown in the block diagram in Fig. 2.

A. Control Objectives

For the CHB multilevel rectifier the control objectives are multiple and of equivalent importance. Firstly, the input current i_s of the topology should be sinusoidal and in phase with the supply voltage v_s, resulting in a unity power factor. Furthermore, the harmonic content of the current should be kept as low as possible, with a low total harmonic distortion (THD), while simultaneously the switching frequency should remain low in order to reduce the switching losses. Finally, the output voltage of each cell v_{o_i} should accurately track its reference, and remain unaffected by changes in the load.

B. Optimal Control Problem

The chosen objective function to be minimized in real-time is:

$$J(k) = \sum_{\ell=k}^{k+N-1} \Big(||i_{s,\text{err}}(\ell+1|k)||_1 + \lambda_1 ||v_{o,\text{err}}(\ell+1|k)||_1 + \lambda_2 ||\Delta u(\ell|k)||_1 \Big) , \quad (10)$$

which penalizes the evolution of the variables of concern over the finite prediction horizon N using the 1-norm (sum of absolute values).

The first term in (10) stands for the input current error. In the control method introduced here, the inner loop aims to regulate the inductor current to its reference, derived from the outer loop. Therefore, the respective deviation is taken into account, given by

$$i_{s,\text{err}}(k) = i_{s,\text{ref}} - i_s(k) . \quad (11)$$

The second term defined as

$$v_{o,\text{err}}(k) = \sum_{i=1}^{n} |v_{o,\text{ref}_i} - \bar{v}_{o_i}(k)| , \quad (12)$$

is added to ensure the regulation of the output voltages of the rectifier cells to their references even when they are of different levels. In (12) $\bar{v}_{o_i}$ is the dc component of the output voltage of the ith cell, i.e.

$$\bar{v}_{o_i}(k) = \frac{1}{M} \sum_{l=0}^{M-1} v_{o_i}(k-l) , \quad (13)$$

where $M \in \mathbb{N}^*$ is the number of samples in one period of the second harmonic (relative to the input voltage frequency) of the output voltage, i.e. $2MT_s = T$, with T being the period of the input voltage. This means that when the rectifier operates under steady-state conditions—assuming accurate regulation of the output voltage of each cell to its reference—the voltage error given by (12) tends to zero. Thus, in steady-state operation the inner control loop is a current loop; current regulation suffices. On the other hand, under transient conditions the voltage term is "active"; it contributes to the improvement of the dynamic behavior of the system, since the controller aims to eliminate the non-zero voltage error by fast charging the capacitors C_{o_i}. Furthermore, augmented by the outer loop presented in Section III-C, it ensures a zero steady-state voltage tracking error: when a difference between the actual and the reference voltage of one cell exists, the total cost, as it is calculated by (10), increases, thereby the controller should achieve both voltage and current tracking. However, in (10) the voltage term (12) is multiplied by the factor λ_1, given by [26]

$$\lambda_1 = \frac{n i_{s,\text{nom}}}{\sum_{i=1}^{n} v_{o_i,\text{nom}}} , \quad (14)$$

where $i_{s,\text{nom}}$ is the amplitude of the nominal input current, and $v_{o_i,\text{nom}}$ is the nominal value of the output voltage of the ith cell. This term is added so that the voltage error term will not significantly overshadow the current error term, and thus deactivating it. If the controller focuses only on the voltage error, then the current regulation will not be achieved, and then stability issues may arise[2].

Finally, the third term aims to decrease the switching frequency and to avoid excessive switching, by penalizing the difference between two consecutive switching states, i.e.

$$\Delta u(k) = u(k) - u(k-1) . \quad (15)$$

The weighting factor $\lambda_2 \in \mathbb{R}^+$ sets the trade-off between the current and the output voltage errors and the switching frequency f_{sw}. Some guidelines for tuning the weighting factor λ_2 are presented in [26]. In Section IV additional information on the impact of the weighting factor on the defined objective function are presented.

The control input at time-instant kT_s is obtained by minimizing the objective function (10) over the optimization variable, which is the sequence of switching states over the horizon $U(k) = [u(k)\ u(k+1) \dots u(k+N-1)]^T$. Thus the following constrained optimization problem is formulated:

$$\begin{aligned} &\underset{U}{\text{minimize}} && J(k) \\ &\text{subject to} && \text{eq. (1)} . \end{aligned} \quad (16)$$

The underlying optimization problem is a mixed-integer optimization problem [27]. For solving such type of problems enumeration is a straightforward option. By taking into account all possible combinations of the switching states ($u_{ip} = 0$ or $u_{ip} = 1$) the switching sequences to be examined are created. The evolution of the state is calculated based on (1a) for each of the 2^{2nN} sequences and the objective function is evaluated. The sequence U^* with the smallest associated cost is considered as the optimal solution, given by

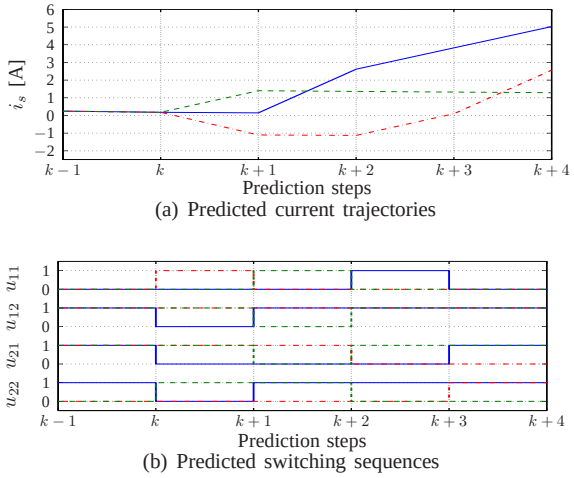
$$U^*(k) = \arg\min J(k) . \quad (17)$$

Out of this sequence, the first element $u^*(k)$ is applied to the converter; the procedure is repeated at $k+1$, based on new measurements acquired at the following sampling instance. An illustrative example of the predicted state—here the inductor current—and the sequence of the control actions, i.e. the switching state, is depicted in Fig. 3. Three candidate switching sequences are shown for the prediction horizon $N = 4$, and for a CHB rectifier consisting of two cells. In Fig. 3(a) the current of step k is the measured one, while from $k+1$ to $k+N$ the current evolution is depicted according to the switching sequences shown in Fig. 3(b).

C. Outer Loop

The outer loop is used for the voltage regulation. A proportional-integral (PI) controller is employed—one for each cell—to regulate the respective output voltage to its reference value. The input of the ith PI controller is the voltage error $v_{o,\text{PI,err}_i} = v_{o,\text{ref}_i} - v_{o_i}$ (see Fig. 2). The reference current $\hat{i}_{s,\text{ref}}$ derived, shown in Fig. 2, is further synchronized with the

[2]This is due to the fact that the output voltage exhibits a non-minimum phase behavior with respect to the switching action.



(a) Predicted current trajectories

(b) Predicted switching sequences

Fig. 3. Three candidate switching sequences for a four-step prediction horizon, i.e. $N = 4$.

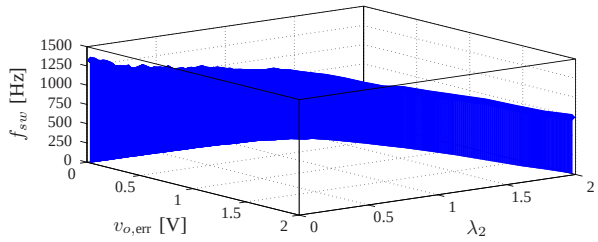


Fig. 4. The output voltage error $v_{o,\text{err}}$ and the corresponding switching frequency f_{sw} versus the weighting factor λ_2 when the converter operates under nominal conditions.

supply voltage by a phase-locked loop (PLL), resulting in a sinusoidal reference current $i_{s,\text{ref}}$.

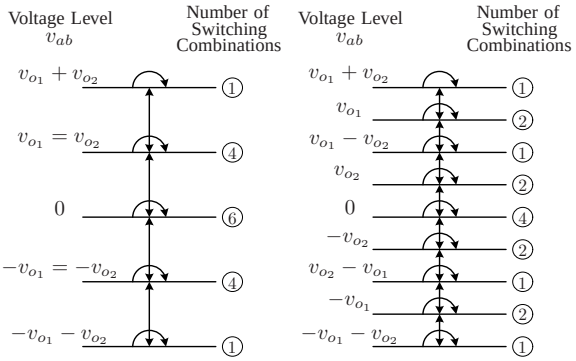
The outer loop is tuned in such a way that the desired settling time and overshoot are achieved during start-up or step changes in the output reference voltage of a cell. In order to achieve a fast voltage regulation with as little overshoot as possible, the dynamics of the output voltages were registered under reference voltage step changes. The information acquired was used to adjust a simple first order model, and to select the gain parameters, k_{pr_i} and k_{int_i}, of the n-PI controllers[3]. With this procedure, the superior performance of the MPC-based inner loop is not deteriorated, as can be seen in Section V.

IV. Discussion and Computational Complexity

A. Impact of Weighting Factor λ_2

To further investigate the impact of the weighting factor λ_2 on the switching frequency and the output voltage error a case of a two-cell CHB rectifier operating under steady-state conditions is considered. The system parameters are shown in Table III, while the prediction horizon is $N = 4$. As can be seen, the sampling interval is $T_s = 100\,\mu$s; this means that the maximum possible switching frequency is equal to $f_{sw,\text{max}} = 5\,$kHz, i.e. $f_{sw,\text{max}} = 1/(2T_s)$. However, in reality

[3]The same values are used for the proportional gains k_{pr_i} of the n-PI controllers. The integral gains k_{int_i} are set at equal values, as well.



(a) Five-level v_{ab}. (b) Nine-level v_{ab}.

Fig. 5. Allowable switching transitions in a two-cell CHB rectifier when the cells operate (a) at the same voltage potential and (b) at different potentials.

TABLE III
System Parameters

Number of cells	n	2
Rated power	P	1 kW
Nominal frequency	f	50 Hz
Input voltage	v_s	110 V rms
Boost inductance	L	8 mH
Internal resistance	R_L	0.7 Ω
Filter capacitance	C_{o_i}	2.2 mF
Sampling interval	T_s	100 μs

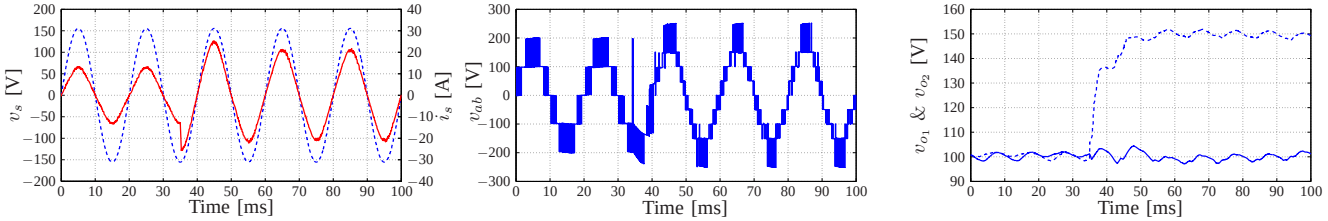
the switching frequency is much lower; the switches are not turned on and off every $2T_s$.

In Fig. 4 the output voltage error given by (12) and the switching frequency f_{sw} are depicted. As it can be observed, an increase in the weighting factor causes a reduction in the switching frequency. However, for values of λ_2 greater than $\lambda_2 \approx 1.1$ a steady-state voltage error occurs. This is due to the fact that the controller puts more effort into penalizing the switching transitions, rather than minimizing the input current and output voltages errors.

B. Switching Constraints

As already mentioned, the controller introduced here takes into account 2^{2nN} sequences, generated by all the possible switching combinations, in order to select the optimal one U^*. In reality, however, when the converter operates under steady-state conditions not all the transitions from one switching state to another are possible. Hence, constraints could be posed to the switching transitions in order to trim the number of the examined switching sequences, resulting in a reduced computational effort.

The constraints are imposed by considering the multilevel waveform of the voltage v_{ab} in the ac side converter terminals (see Fig. 1). As can be seen in Table I, the total voltage levels of v_{ab} are $2n + 1$ when the cell voltages are equal. These levels depend on the switching state of the cells, i.e. the way that the output voltage of each cell is reflected to the ac side. Hence, only these switching sequences that ensure smooth transition from one level to the neighboring one (lower or higher) are considered *feasible* and examined. Furthermore,

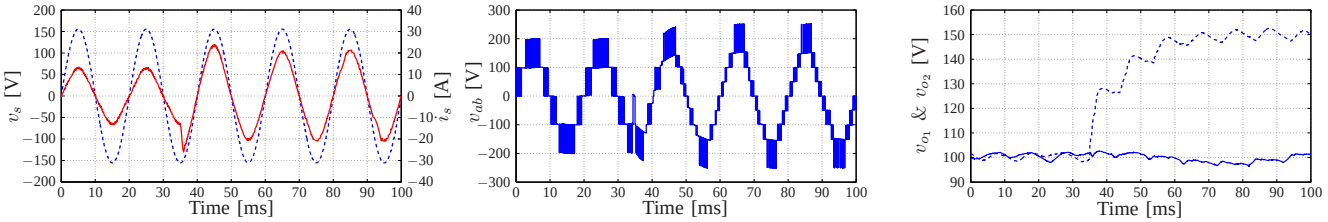


(a) Input voltage (dashed line) and current (solid line).

(b) Ac side voltage.

(c) Output voltage of first (solid line) and second cell (dashed line).

Fig. 6. Without considering the switching constraints: Transient response of a two-cell CHB rectifier to a step-up change in the output voltage reference of the second cell (simulation results).



(a) Input voltage (dashed line) and current (solid line).

(b) Ac side voltage.

(c) Output voltage of first (solid line) and second cell (dashed line).

Fig. 7. Considering the switching constraints: Transient response of a two-cell CHB rectifier to a step-up change in the output voltage reference of the second cell (simulation results).

when the converter is operating under unbalanced output cell voltages, the number of the voltage levels of v_{ab} increases, depending on the number of the different potentials. In such case the redundant states are significantly decreased, resulting in a further reduction of the computational complexity; the switching sequences that guarantee smooth transition from one voltage level to the next one are fewer.

Fig. 5 shows an example of the allowable switching transitions for the case of a two-cell CHB rectifier. In Fig. 5(a) the converter operates under balanced output voltages, i.e. a five-level voltage waveform v_{ab} is produced. As can be seen in Table II, 6 different switching states can produce the zero-voltage level. Thus, the maximum number of switching sequences to be examined corresponds to the case of $v_{ab}(k) = 0$. Assuming a one-step horizon the number of the possible optimal sequences is equal to 14: 6 sequences lead to a transition $v_{ab}(k) = 0 \rightarrow v_{ab}(k+1) = 0$, 4 sequences to a transition $v_{ab}(k) = 0 \rightarrow v_{ab}(k+1) = v_{o_1} = v_{o_2}$, and 4 sequences to a transition $v_{ab}(k) = 0 \rightarrow v_{ab}(k+1) = -v_{o_1} = -v_{o_2}$ (see Table II). For the case of a two-step horizon, again the most computational effort is required when $v_{ab}(k+1) = 0$; 14^2 sequences should be examined. By extending the prediction horizon to N-steps, the worst-case scenario is when $v_{ab}(k) = 0 = v_{ab}(k+1) = \ldots = v_{ab}(k+N)$, corresponding to 14^N sequences. On the other hand, when the switching constraints are not considered the feasible sequences are $2^{2\cdot 2N} = 16^N$. Following the same procedure, it can be shown that when the switching constraints are active the number of the sequences examined for the case of an n-level CHB rectifier is reduced, compared to the respective number of the unconstrained case.

In Fig. 5(b) the allowable transitions in a nine-level waveform v_{ab}, resulting from the unbalanced cell voltages of a two-cell CHB converter, are depicted (it is assumed that $v_{o_2} < \frac{v_{o_1}}{2}$). Under these operating conditions the number of the feasible sequences is further reduced, since the redundancies are not that many. Once again, more redundant states correspond to the zero-voltage level compared to the other voltage levels. Therefore, following the same approach as before, in a one-step horizon the maximum feasible sequences are 8: 4 sequences for the transition $v_{ab}(k) = 0 \rightarrow v_{ab}(k+1) = 0$, 2 sequences for $v_{ab}(k) = 0 \rightarrow v_{ab}(k+1) = v_{o_2}$, and 2 sequences for $v_{ab}(k) = 0 \rightarrow v_{ab}(k+1) = -v_{o_2}$ (Table II). For a N-step horizon the maximum switching sequences to be examined are 8^N, far fewer than the 16^N sequences encountered when the switching constraints are not considered.

However, the reduced computational complexity comes at a cost: the transient response of the system is deteriorated. This can be seen in Figs. 6 and 7, where a step-up change in the output voltage reference of the second cell of a two-cell CHB rectifier occurs at $t = 35\,\text{ms}$, from $v_{o,\text{ref}_2} = 100\,\text{V}$ to $v_{o,\text{ref}_2} = 150\,\text{V}$; the reference voltage of the first cell is $v_{o,\text{ref}_1} = 100\,\text{V}$ (the parameters of the system are shown in Table III).

When the switching constraints are not taken into account (Fig. 6), the voltage of the second cell reaches its reference in about $t \approx 20\,\text{ms}$ (Fig. 6(c)). Due to the fact that there are no restrictions on the switching transitions, these switching states are applied that allow the instantaneous change in v_{ab} from its lowest voltage level $\{-v_{o_1} - v_{o_2}\}$, to its highest $\{v_{o_1} + v_{o_2}\}$ (Fig. 6(b)). This change results in a high di_s/dt, and consequently in a fast capacitor charging, see Fig. 6(a).

On the other hand, when the switching constraints are active (Fig. 7), the transient lasts more; the voltage of the second cell

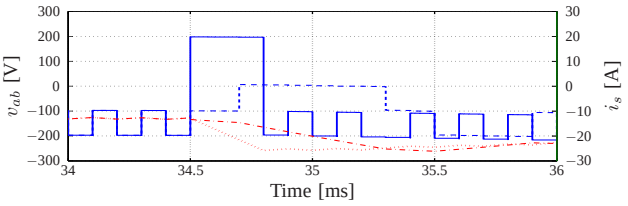


Fig. 8. Detail of the ac side voltage without the switching constraints (solid line) and with them (dashed line), and of the input current without the switching constraints (dotted line) and with them (dash-dotted line) when the step change in the output voltage reference occurs.

reaches its reference in about $t \approx 40\,\text{ms}$ (Fig. 7(c)), while a small undershoot in the voltage of the first cell is observed. For this case the current increases slower (Fig. 7(a)); the current slope di_s/dt is lower due to the fact that the switching states that lead to an immediate transition from level $\{-v_{o_1} - v_{o_2}\}$ of the multilevel voltage v_{ab} to level $\{v_{o_1} + v_{o_2}\}$ are not allowed. The ac side reflected voltage is initially equal to $\{-v_{o_1} - v_{o_2}\}$. Following, the only permitted switching transition generates a voltage v_{ab} equal to $\{-v_{o_1} = -v_{o_2}\}$. Finally, since the goal is to increase the input current, a switching state is selected that results in a further decrease in the multilevel voltage to the next allowable level, i.e. the zero-voltage level. In Fig. 8 the multilevel voltage v_{ab} and the input current i_s from both implementations—with and without the switching constraints—are shown in detail at the beginning of the transient. Finally, it should be noted that if the high input current during the transients is a concern, a current limit can be added, with the trade-off of higher settling time.

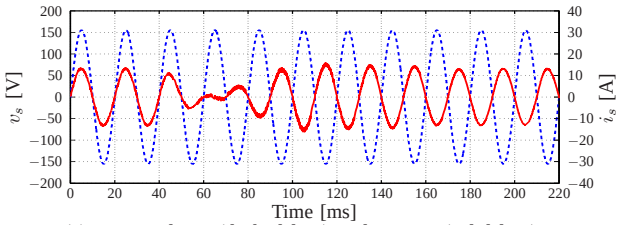
C. Regeneration Mode

An additional feature of the proposed MPC strategy is its ability to fulfill the control objectives even when the converter is operating in regenerative mode, i.e. when the load delivers power to the supply. In order to investigate the performance of the proposed strategy under regenerative load conditions a two-cell CHB rectifier, the parameters of which are shown in Table III, is considered. The system is operating under nominal conditions and balanced loads; the output voltage reference values are $v_{o,\text{ref}_1} = v_{o,\text{ref}_2} = 100\,\text{V}$, i.e. the load current of each cell is $i_{o_i} = 5\,\text{A}$. In order to model the load current a 5-A current source is connected to each cell. Finally, a two-step prediction horizon is used, while the switching constraints are not taken into account.

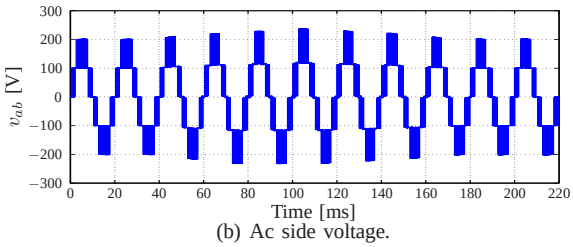
In Fig. 9 the transition from motoring to generating mode is shown. At time $t = 40\,\text{ms}$ the direction of the current flow is reversed to both cells so as to change the power flow from the cells to the grid. This forces the inductor current to change its polarity; the input current is $180°$ out of phase with respect to the supply voltage, as can be seen in Fig. 9(a). Furthermore, after an initial increase because of the power delivered by the loads, the output voltages of the cells, v_{o_1} and v_{o_2}, accurately track their reference values, see Fig. 9(c).

V. Performance Evaluation

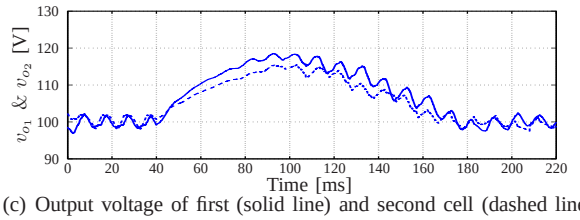
In this section experimental results of the proposed control algorithm are presented. As a case study a CHB single-phase



(a) Input voltage (dashed line) and current (solid line).



(b) Ac side voltage.



(c) Output voltage of first (solid line) and second cell (dashed line).

Fig. 9. Simulation results of a two-cell CHB rectifier operating under normal (for $t < 40\,\text{ms}$) and regenerative conditions (for $t > 40\,\text{ms}$).

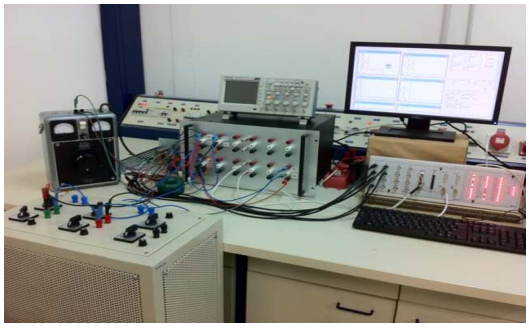


Fig. 10. Experimental setup that includes a prototype CHB rectifier (left—below the oscilloscope) and the dSpace real-time system used for control (right—below the monitor).

rectifier consisting of two H-bridge cells is considered, i.e. as the one shown is Fig. 1 with $n = 2$. The parameters of the experimental setup are shown in Table III. It should be noted that the converter is connected to the grid (power supply) via an autotransformer; the autotransformer is used to step down the grid voltage from $230\,\text{V}$ to $110\,\text{V}$.

For the performance test the switching constraints are not taken into account in order to highlight the dynamic response of the controller. Thus, a two-step prediction horizon is employed ($N = 2$) so as to keep the computational complexity modest. Furthermore, the weight in the objective function (10) is heuristically chosen as $\lambda_2 = 0.2$. Finally, the proportional gain of the PI controllers is chosen as $k_{\text{pr}_1} = k_{\text{pr}_2} = 0.1$, and the integral gain as $k_{\text{int}_1} = k_{\text{int}_2} = 0.7$. The control algorithm was implemented on a dSpace 1104 system with I/O card for

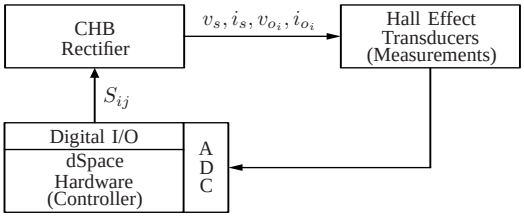
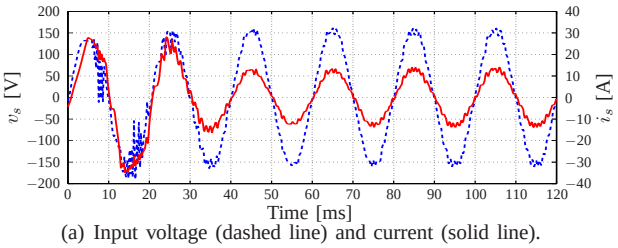
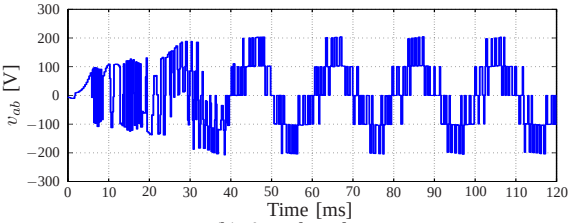


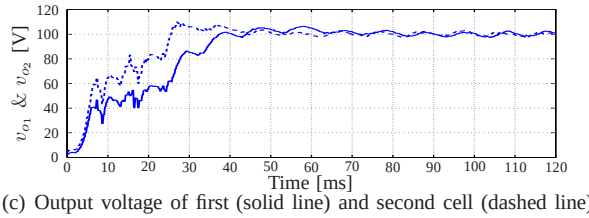
Fig. 11. Schematic of the experimental setup (ADC stands for the analog-to-digital converter).



(a) Input voltage (dashed line) and current (solid line).



(b) Ac side voltage.



(c) Output voltage of first (solid line) and second cell (dashed line).

Fig. 12. Experimental results from a single phase rectifier consisting of two cascaded H-Bridge cells for nominal start-up.

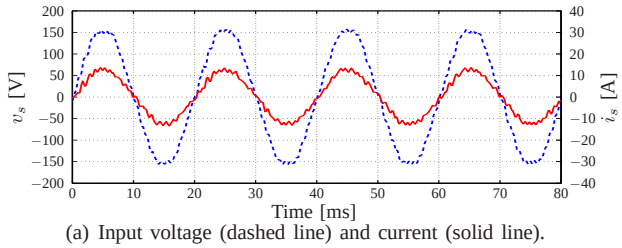
real-time control. The experimental setup and its schematic diagram are shown in Figs. 10 and 11, respectively.

A. Start-up

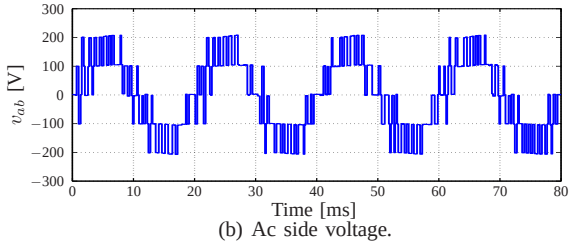
The first case to be examined is that of the dynamic behavior of the CHB rectifier during start-up and nominal conditions. The output voltage reference for both cells is set equal to $v_{o,\text{ref}_1} = v_{o,\text{ref}_2} = 100\,\text{V}$. As can be seen in Fig. 12, the input current quickly increases in order to charge the capacitors to the demanded voltage levels (Fig. 12(a)). After about $t \approx 50\,\text{ms}$ the output voltages of both cells reach their reference values (Fig. 12(c)), and the input current reaches its nominal value. Furthermore, the ac side reflected voltage consists of five levels (Fig. 12(b)), since the cell voltages are of the same level.

B. Steady-State Operating Conditions

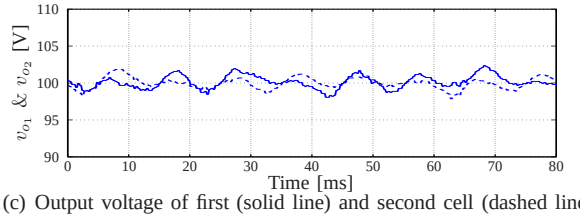
Operating with a switching frequency of about $f_{sw} \approx 1.1\,\text{kHz}$ at the previously attained operating point,



(a) Input voltage (dashed line) and current (solid line).



(b) Ac side voltage.



(c) Output voltage of first (solid line) and second cell (dashed line).

Fig. 13. Experimental results under steady-state operating conditions.

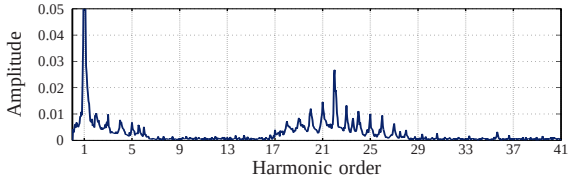
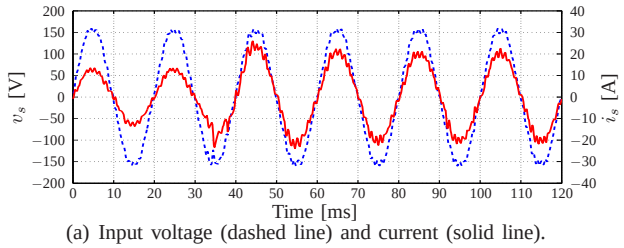


Fig. 14. Input current spectrum. The THD of the input current i_s is 3.54%. The current is given in p.u..

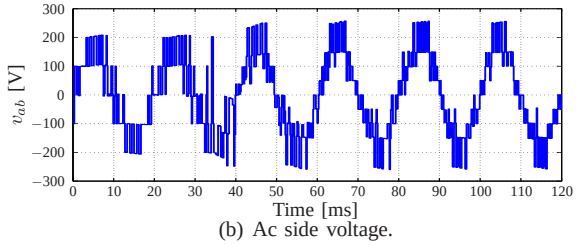
the steady-state performance is examined and the results are presented in Fig. 13. The input current i_s is a sinusoidal waveform and in phase with the supply voltage v_s (Fig. 13(a)). The harmonic content of the input current is low, resulting in a THD of 3.54%, according to Fig. 14 where the current spectrum up to the 41^{st} harmonic is depicted. It can be observed that the current spectrum is distributed around the 22^{nd} harmonic, i.e. the most significant harmonics are located in high frequencies corresponding to the switching frequency and the frequencies around it. In Fig. 13(b) the five-level reflected voltage to the ac side is illustrated, resulting from the fact that the two-cell converter is operating under balanced output cell voltages (see Fig. 13(c)).

C. Step Change in the Output Reference Voltage

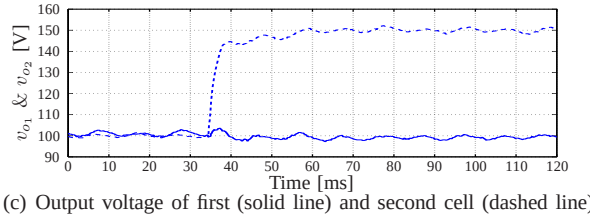
Next, a step change in the reference of the output voltage of the second cell takes place (Fig. 15). At time $t \approx 35\,\text{ms}$ the reference is stepped up from $v_{o,\text{ref}_2} = 100\,\text{V}$ to $v_{o,\text{ref}_2} = 150\,\text{V}$. The output voltage of the second cell reaches its new reference value in about $t \approx 25\,\text{ms}$ without any overshoot or undershoot, while the output voltage of the first cell remains practically



(a) Input voltage (dashed line) and current (solid line).

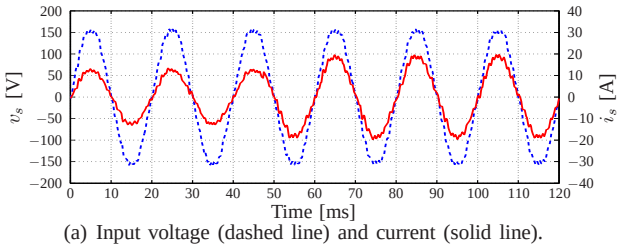


(b) Ac side voltage.

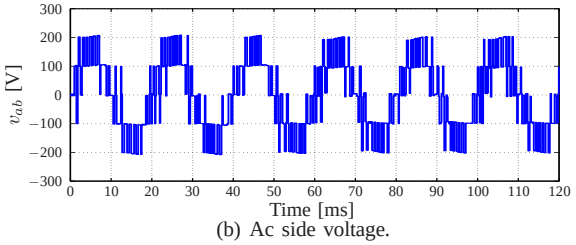


(c) Output voltage of first (solid line) and second cell (dashed line).

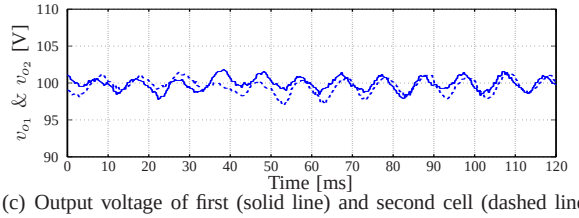
Fig. 15. Experimental results for a step-up change in the output voltage reference of the second cell.



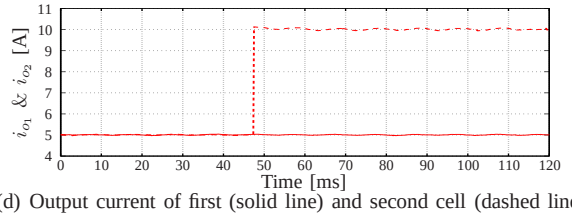
(a) Input voltage (dashed line) and current (solid line).



(b) Ac side voltage.



(c) Output voltage of first (solid line) and second cell (dashed line).



(d) Output current of first (solid line) and second cell (dashed line).

Fig. 16. Experimental results for a load step change on the second cell.

unaffected by this change (Fig. 15(c)). The input current response to the aforementioned change is depicted in Fig. 15(a); the amplitude instantaneously increases, while the unity power factor is maintained. Finally the ac side reflected multilevel voltage (Fig. 15(b)) is composed of nine distinctive levels due to the unbalanced output cell voltages, as it is expected.

D. Load Step

Finally, a step-down change in the load resistance of one cell is examined. For this case the cells operate again at the same voltage potential, i.e. $v_{o,\text{ref}_1} = v_{o,\text{ref}_2} = 100\,\text{V}$, thus a five-level v_{ab} is generated. As shown in Fig. 16, at $t \approx 48\,\text{ms}$ the nominal load resistance of the second cell decreases by half, i.e. from $R = 20\,\Omega$ to $R = 10\,\Omega$. The load current of the second cell is instantaneously doubled (Fig. 16(d)), while the voltages of both cells remain unaffected by this change, see Fig. 16(c).

VI. Conclusions

In this work a model predictive control (MPC) approach for the cascaded H-bridge (CHB) multilevel rectifier based on enumeration is introduced. By directly manipulating the switches of the converter the regulation of the input current to its reference is achieved; the voltage term added in the objective function maintains and improves the effectiveness of the strategy introduced under transient operating conditions. The controller is able to stabilize the system for the entire operating regime due to the exhaustive search of all possible switching combinations. Furthermore, the proposed algorithm exhibits favorable performance during transients. In addition, the nature of the controller implies that it is directly extendable to other topologies such as the three-phase rectifier. These benefits overshadow the drawbacks of the proposed technique such as the increased computational complexity and the variable switching frequency resulting from the absence of a modulator. However, methods to significantly reduce the computational effort, e.g. by imposing constraints on the switching transitions, are proposed. Finally, the performance of the presented control algorithm is verified by experimental results from a two-cell CHB single-phase multilevel rectifier.

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