2019 IEEE Nordic Circuits and Systems Conference (NORCAS 2019): NORCHIP and International Symposium of System-on-Chip (SoC 2019) proceedings

2019 IEEE Nordic Circuits and Systems Conference (NORCAS):

NORCHIP and International Symposium of System-on-Chip (SoC)

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2019 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)

Welcome to NORCAS 2019

On behalf of the Organizing Committee, we would like to welcome all of you to Helsinki and to the Fifth IEEE Nordic Circuits and Systems Conference (NorCAS 2019). The conference is a merge of the well-established conferences NORCHIP and the International Symposium on System-on-Chip (SoC).

We have a high-quality program with keynotes and papers to be presented as well as a pre-conference tutorial. Research covering a wide range of topics within circuits and systems in the digital, analog and mixed domains will be presented.

From in total 105 papers submitted, 39 papers were selected for oral presentations and an additional 14 papers for poster presentations. There will be four invited speakers who will share their view on emerging key technologies in the circuits and systems field. In the opening session Prof. Andreas Herkersdorf from TU Munich, Germany, will present "Tackling the MPSoC Data Locality Challenge with Regional Coherence and Near Memory Acceleration." Later in the afternoon Prof. Mircea Guina from Tampere University, Finland, will give insights to new optoelectronics platforms for photonic integrated circuits and their synergy with electronics. In the second morning, Dr. Philippe Flatresse, Dolphin Design, France, will present FDSOI, an energy-efficient technology for cost-effective SoC platform. The final talk is given by Dr. Mikko Varonen from VTT, Finland, introducing solutions for MMIC design – from 5G RF front-ends to cryogenic receivers for radio astronomy. There will also be an exciting tutorial on Ultra-Low Power ICs for IoT devices and sensor nodes, by Orazio Aiello from National University of Singapore, on the day before the official opening of the conference.

The electronics industry in Finland is of a notable size, represented both by international and local companies. The best known from international ones are Nokia, ABB, Kone, Vaisala, Teleste, Bittium, Polar, Suunto, Metso, Patria and HMD Global, but there are also considerable branch offices of global giants such as Huawei, Ericsson, Intel, AMD and Nvidia. Other major sectors in the Finnish industry are shipyards, paper industry, machinery, utility vehicles, and information technology (including e.g. data security, computer games).

We would like to forward great thanks to IEEE Circuits and Systems Society (CAS) for financial co-sponsoring of the conference. Thanks also to The Federation of Finnish Learned Societies for financial support, and Tampere University for the efforts of the congress office. We are also thankful to all the Program Committee members and reviewers who have put time and effort into reviewing the submitted papers. Moreover, we are grateful to the NorCAS steering committee for helpful advice and their contribution in the paper selection process.

We hope that you will enjoy your time in Helsinki. We wish you an inspiring conference where your knowledge is increased and friendships are both established and strengthened.

Jari Nurmi
General Chair
Tampere University

Technical program committee chairs
Analog: Kari Halonen, Aalto University
Digital: Juha Röning, University of Oulu
SoC: Peeter Ellervee, Tallinn University of Technology

Tampere University CAS IEEE

IEEE Nordic Circuits and Systems Conference (NorCAS) 2019

October 28-30, 2019 Scandic Grand Marina, Helsinki

Conference Program

Monday October 28

1:00pm – 2:30pm Tutorial lectures (Orazio Aiello) – room Lars

2:30pm – 3:00pm Coffee break

3:00pm – 5:00pm Tutorial lectures (Orazio Aiello) – room Lars

Tuesday October 29

9:00 Opening (Jari Nurmi)

9:15 **Keynote 1 – room Nordia**

Chair: Jari Nurmi, Tampere University

Prof. Andreas Herkersdorf, TU Munich, DE: Tackling the MPSoC Data Locality Challenge with Regional Coherence and Near Memory Acceleration

10:00 **Plenary 1 – room Nordia**

Chair: Dag T. Wisland, UiO

10:00 Self-Calibrated Delay-Based LSB Extraction for Resolution Improvement in SAR ADCs
Ayca Akkaya, Firat Celik, Yusuf Leblebici, *EPFL, Switzerland*

10:20 A Real-Time Fast Ethernet Transceiver achieving Sub-ns Time Synchronization
Simon Buhr, Martin Kreißig, Frank Ellinger, *Technische Universität Dresden, Germany*

10:40 IEEE 802.11ad SC-PHY Layer Simulator: Performance in Real-world 60 GHz Indoor Channels
Jiri Blumenstein[1], Jiri Milos[1], Ladislav Polak[1], Christoph Mecklenbrauker[2]
[1]Brno University of Technology, Czech Republic; [2]TU Wien, Austria

11:00 Coffee break

11:30 **MMIC – room Nordia**

Chair: Ted Johansson, Linköping University

11:30 Optimizing Inductorless Static CML Frequency Dividers up to 23GHz Output Using 45nm CMOS PD-SOI
Mikko Hietanen, Janne Aikio, Alok Sethi, Rehman Akbar, Timo Rahkonen, Aarno Pärssinen
University of Oulu, Finland

11:50 Ka-Band Stacked Power Amplifier on 22 nm CMOS FDSOI Technology Utilizing Back-Gate Bias for Linearity Improvement
Jere Rusanen, Mikko Hietanen, Alok Sethi, Timo Rahkonen, Aarno Pärssinen, Janne P. Aikio
University of Oulu, Finland

12:10 Designing at Millimeter-Wave: Lessons from a Triple Coil Variable Transformer
Alok Sethi, Rehman Akbar, Janne P. Aikio, Rana A. Shaheen, Aarno Pärssinen, Timo Rahkonen
University of Oulu, Finland

11:30 **Machine Learning Implementations – room Compass**

Chair: Juha Röning, University of Oulu

11:30 A Hardware Inference Accelerator for Temporal Convolutional Networks
Rashid Ali[1], Maen Mallah[1], Martin Leyh[1], Philipp Holzinger[2], Marco Breiling[1], Marc Reichenbach[2]
[1]Fraunhofer IIS, Germany; [2]Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany

11:50 Dual-Stage Phase Unwrapping
Bardia Barabadi[1], Matthew Gara[2], Ali Jooya[2], Amirali Baniasadi[1], Nikitas Dimopoulos[1]
[1]University of Victoria, Canada; [2]3v Geomatics Inc., Vancouver, Canada

12:10 Low-Power, High-Speed Adversarial Attack based 4:2 Compressor as Full Adder for Multipliers in FIR Digital Filters
Ravindra JVR, Lavanya Maddisetti, *Vardhaman College of Engineering, India*

12:30 Lunch break

13:40 **Analog and Digital Radio Issues – room Nordia**

Chair: Atila Alvandpour, Linköping University

13:40 Linearization of Active Transmitter Arrays in Presence of Antenna Crosstalk for 5G Systems
Feridoon Jalili, Martin H. Nielsen, Ming Shen, Ole K. Jensen, Jan H. Mikkelsen, Gert F. Pedersen, *Aalborg University, Denmark*

14:00 Practical Stimulus Design for a Multi-Tone Fit
Marko Neitola, *University of Oulu, Finland*

14:20 Sphere Decoder for Massive MIMO Systems
Dimitris Vordonis, Vassilis Paliouras
University of Patras, Greece

13:40 **Harnessing Machine Learning Techniques – room Compass**

Chair: Jiri Blumenstein, Brno University of Technology

13:40 How Diversity Affects Deep-Learning Side-Channel Attacks
Huanyu Wang, Martin Brisfors, Sebastian Forsmark, Elena Dubrova
Royal Institute of Technology, Sweden

14:00 Hardware Implementation Aspects of a Syndrome-based Neural Network Decoder for BCH Codes
Emmanouil Kavvousanos, Vassilis Paliouras
Electrical and Computer Engineering Department, University of Patras, Greece

14:20 A Configurable and Versatile Architecture for Low Power, Energy Efficient Hardware Acceleration of Convolutional Neural Networks
Steinar Thune Christensen[1], Omer Qadir[2], Snorre Aunet[1]
[1]Norwegian University of Science and Technology, Norway; [2]Nordic Semiconductor, Norway

14:40 **Coffee and posters 1 – Nordia foyer**

The Validation of Graph Model-Based, Gate Level Low-Dimensional Feature Data for Machine Learning Applications
Aneesh Balakrishnan[1], Thomas Lange[1], Maximilien Glorieux[1], Dan Alexandrescu[1], Maksim Jenihhin[2]
[1]IROC Technologies, France; [2]Tallinn University of Technology, Estonia

A Real-Time Gesture Recognition System with FPGA Accelerated ZynqNet Classification
Ricardo Nunez-Prieto[1], Pablo Correa-Gomez[2], Liang Liu[1]
[1]Lund University, Sweden; [2]Universidad Politecnica de Madrid, Spain

Machine Learning-based Prediction for Dynamic, Runtime Architectural Optimizations of Embedded Systems
Ruben Vazquez, Ann Gordon-Ross, Greg Stitt, *University of Florida, USA*

An Explicitly Parallel Architecture for Packet Processing in Software Defined Networks
Hesam Zolfaghari[1], Davide Rossi[2], Jari Nurmi[1]
[1]Tampere University, Finland; [2]University of Bologna, Italy

Layout Optimization Techniques for rg and fmax of Cascode Devices for mmWave Applications
Rana Azhar Shaheen, Timo Rahkonen, Rehman Akbar, Janne Aikio, Alok Sethi, Aarno Pärssinen, *University of Oulu, Finland*

A 36 nW trimless voltage reference with low sensitivity to PVT variations
Calvin Maxsen[1,2], Pere Llimós Muntal[1], Gunnar Gudnason[2], Ivan H. H. Jørgensen[1]
[1]Technical University of Denmark, Denmark; [2]Demant A/S

Ultra Low Voltage Subthreshold Binary Adder Architectures for IoT Applications: Ripple Carry Adder or Kogge Stone Adder
Somayeh Hossein Zadeh, Trond Ytterdal, Snorre Aunet, *NTNU, Norway*

15:30 **Keynote 2 – room Nordia**

Chair: Juha Röning, University of Oulu

Prof. Mircea Guina, Tampere University, FI: New optoelectronics platforms for photonic integrated circuits and synergy with electronics

16:15 **Sigma-Delta ADCs – room Nordia**

Chair: Kari Halonen, Aalto University

16:15 Two-Stage Internal DAC Mismatch Mitigation for a Continuous-Time Delta-Sigma ADC
Marko Tuomo Tapani Neitola, *University of Oulu, Finland*

16:35 A 5 GHz CT ΔΣ ADC with 250MHz Signal Bandwidth in 28 nm-FDSOI CMOS
Siyu Tan[1], Lars Sundström[2], Mattias Palm[2], Sven Mattisson[1,2], Pietro Andreani[1]
[1]Lund University, Lund, Sweden; [2]Ericsson Research, Lund, Sweden

16:55 A 500mV, 118nW, Sigma Delta Modulator ADC for Audio Detection in 28 nm FD-SOI
Markus Mogensen Henriksen, Dennis Øland Larsen, Pere Llimós Muntal, Ivan H. H. Jørgensen
Technical University of Denmark, Denmark

16:15 **Reliability and Security Issues of SoC Implementations – room Compass**

Chair: Juha Röning, University of Oulu

16:15 Accelerating Transient Fault Injection Campaigns by using Dynamic HDL Slicing
Ahmet Cagri Bagbaba[1,2], Maksim Jenihhin[2], Jaan Raik[2], Christian Sauer[1]
[1]Cadence Design Systems; [2]Tallinn University of Technology, Estonia

16:35 A Fault-Tolerant Time-Predictable Processor
Christos Gkiokas, Martin Schoeberl
Technical University of Denmark, Denmark

16:55 Reconfigurable Module of Multi-mode AES Cryptographic Algorithms for AP SoCs
Arthur Silitonga[1], Zhou Jiang[2], Nadir Khan[3], Juergen Becker[1]
[1]Institute for Information Processing Technologies - Karlsruhe Inst. of Tech, Karlsruhe, Germany; [2]Datang Mobile Communications Equipment Co., Ltd., Shanghai, China; [3]FZI Research Center for Information Technology, Karlsruhe, Germany

17:15 End of day 1 program

19:00 **Conference Dinner – Restaurant Marine** (on-site)

Wednesday October 30

9:00 **Keynote 3 – room Nordia**

Chair: Peeter Ellervee, Tallinn University of Technology

Dr. Philippe Flatresse, Dolphin Design, FR: FDSOI, an energy-efficient technology for cost-effective SoC platform

9:45 **Coffee and posters 2 – Nordia foyer**

End-to-End Approximation for Characterizing Energy Efficiency of IoT Applications
MohammadReza Nakhkash[1], Anil Kanduri[1], Amir M. Rahmani[2], Pasi Liljeberg[1]
[1]University of Turku, Finland; [2]University of California, Irvine, USA

Optimizing Mitchell's Method for Approximate Logarithmic Addition via Base Selection with Application to Back-Propagation
Mark G Arnold[1], Ed Chester[2], John R Cowles[3], Corey Johnson[3]
[1]XLNS Research, USA; [2]Catena Space, United Kingdom; [3]University of Wyoming, USA

1/f-Noise and Offset Cancellation for Rail-to-Rail Single-Slope ADCs in MEA Applications
Lukas Straczek, Dominik J. Veit, Jürgen Oehm, *Ruhr University Bochum, Germany*

T-LINC Architecture with Digital Combination and Mismatch Correction in the Receiver
Emilio José Martínez-Pérez, Feridoon Jalili, Ming Shen, Jan H. Mikkelsen, Ole K. Jensen, Gert Pedersen, *Aalborg University, Denmark*

Instruction Extension of a RISC-V Processor Modeled with IP-XACT
Saman Payvar[1], Esko Pekkarinen[1], Rafael Stahl[2], Daniel Mueller-Gritschneder[2], Timo D. Hämäläinen[1]
[1]Tampere University, Finland; [2]Technical University of Munich, Germany

Exploring optimal back bias voltages for ultra low voltage CMOS digital Circuits in 22 nm FDSOI Technology
Somayeh Hossein Zadeh, Trond Ytterdal, Snorre Aunet, *NTNU, Norway*

Semantic segmentation with inexpensive simulated data
Jukka Matias Peltomäki, Mengyang Chen, Heikki Huttunen
Tampere University, Finland

10:30 **Plenary 2 – room Nordia**

Chair: Ted Johansson, Linköping University

10:30 A New Interpretation to Groszkowski's Effect
Mostafa Jafari Nokandi, Sumit Pratap Singh, Aarno Pärssinen, Timo Rahkonen
University of Oulu, Finland

10:50 An Analogue Baseband Chain for a Magnetic Tunnel Junction Based RF Signal Detector
Rui Ma, Simon Buhr, Zoltán Tibenszky, Martin Kreißig, Frank Ellinger
Technische Universität Dresden, Germany

11:10 **Analog Systems – room Nordia**

Chair: Ivan Harald Holger Jørgensen, DTU

11:10 Single Burst Depth-Resolving Raman Spectrometer Based on a SPAD Array with an On-Chip TDC to Analyse Heterogenous Liquid Samples
Jere Kekkonen, Ilkka Nissinen, *Circuits and Systems Research Unit, University of Oulu, Finland*

11:30 A 40-GHz Fully-Integrated CMOS-Based Biosensor Circuit With an On-Chip Vector Network Analyzer for Circulating Tumor Cells Analysis
Taiki Nakanishi[1], Shunya Murakami[1], Atsuki Kobayashi[1], Md. Zahidul Islam[1], Kiichi Niitsu[1,2]
[1]Nagoya University, Japan; [2]JST/PRESTO, Japan

11:50 A Time-based Sensing Scheme for Multi-level Cell (MLC) Resistive RAM
John Reuben, Dietmar Fey
Friedrich-Alexander-University Erlangen-Nurnberg, Germany

11:10 **Providing HW Resources – room Compass**

Chair: Jari Nurmi, Tampere University

11:10 Nwise: an Area Efficient and Highly Reliable Radiation Hardened Memory Cell Designed for Space Applications
Azam Seyedi, Snorre Aunet, Per Gunnar Kjeldsberg, *NTNU, Norway*

11:30 An All-Digital Duty-Cycle Corrector for Parallel High-Speed I/O Links
Nico Angeli, Klaus Hofmann
TU Darmstadt, Germany

11:50 Dynamic Resource Allocation for HEVC Encoding in FPGA-Accelerated SDN Cloud
Panu Sjövall, Arto Oinonen, Mikko Teuho, Jarno Vanne, Timo Hämäläinen
Tampere University, Finland

12:10 Lunch break

13:15 **Keynote 4 – room Nordia**

Chair: Kari Halonen, Aalto University

Dr. Mikko Varonen, VTT, FI: MMIC design - from 5G RF front-ends to cryogenic receivers for radio astronomy

14:00 **Best paper award and NorCAS 2020 – room Nordia**

14:15 **Voltage Converters and Amplifiers – room Nordia**

Chair: Kari Halonen, Aalto University

14:15 Novel Clocking Scheme with Improved Voltage Gain for a Two-Phase Charge Pump Topology
Jakob Kenn Toft, Ivan Harald Holger Jørgensen, *Technical University of Denmark*

14:35 A Time-Based Control Scheme for Power Factor Correction Boost Converter
Christopher H. K. Jensen, Rasmus B. Lind, Jens C. Hertel, Ahmed M. Ammar, Arnold Knott, Michael A. E. Andersen, *Technical University of Denmark*

14:55 A 300mV-Supply Standard-Cell-Based OTA with Digital PWM Offset Calibration
Pedro Toledo[1,2], Orazio Aiello[1,3], Paolo Crovetti[1]
[1]Politecnico di Torino, Italy; [2]Federal University of Rio Grande do Sul, Brazil; [3]National University of Singapore, Singapore

14:15 **Approximate Computing – room Compass**

Chair: Jari Nurmi, Tampere University

14:15 MemOpt: Automated Memory Distribution for Multicore Microcontrollers with Hard Real-Time Requirements
Philipp Jungklass[1], Mladen Berekovic[2]
[1]IAV GmbH, Germany; [2]University of Lübeck, Institute of Computer Engineering, Germany

14:35 On Applications of Configurable Approximation to Irregular Voltage
Toshinori Sato, Tomoaki Ukezono, *Fukuoka University, Japan*

14:55 Fast Fixed-point Bicubic Interpolation Algorithm on FPGA
Janne Koljonen, Vladimir A. Bochko, Sami J. Lauronen, Jarmo T. Alander
University of Vaasa, Finland

15.15 **Coffee break – Nordia foyer**

15:40 **SAR ADC – room Nordia**

Chair: Ivan Harald Holger Jørgensen, DTU

15:40 Two-Step Pipeline SAR ADC with passive Charge Sharing between Cascades
Dmitry Osipov[1], Aleksandr Gusev[1], Vitaly Shumikhin[2], Steffen Paul[1]
[1]University of Bremen, Germany; [2]National Research Nuclear University MEPhI, Germany

16:00 An AFE for Catheter-Based IEGM sensing with Inverter-based SAR ADC
Yuchen Zhao[1], Haoming Chu[1], Bengt Kallback[2], Yajie Qin[1], Zhuo Zou[1], Lirong Zheng[1]
[1]Fudan University, China; [2]Cathprint AB, Stockholm, Sweden

15:40 **High-Level Design Methodologies – room Compass**

Chair: Peeter Ellervee, Tallinn University of Technology

15:40 HLS-Based Flexible Hardware Accelerator for PCA Algorithm on a Low-Cost ZYNQ SoC
Mohammad Amir Mansoori, Mario R. Casu, *Politecnico di Torino, Italy*

16:00 Towards a Python-Based One Language Ecosystem for Embedded Systems Automation
Zhao Han[1,2], Keerthikumara Devarajegowda[1,3], Michael Werner[1,2], Wolfgang Ecker[1,2]
[1]Infineon Technologies AG; [2]Technical University of Munich, Germany; [3]Technical University of Kaiserslautern, Germany

16:20 HALib: Hardware Assertion Library for on-board verification of FPGA-based modules using HLS
Julian Caba, Fernando Rincón, Jesús Barba, José Antonio De La Torre, Julio Daniel Dondo, Juan Carlos López, *UCLM, Spain*

16:40 End of the program

Have a good trip back home!