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# Use of microcutting for high throughput electrode patterning on flexible substrate

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**Abstract.** The use of printing technologies is promising for low-cost manufacturing of flexible, light-weight and large-area electronics, such as electronic paper or solar cells. Here, we demonstrate a microcutting technique and methods to fabricate cutting blades for patterning of metal structure on a polymer substrate. Microcutting is done using a hot embossing and nanoimprinting techniques. The metallic fine patterns obtained using stamps fabricated using different techniques are compared. Combination of microcutting and our recently proposed dielectric alignment opens up a novel platform for a variety of applications, such as the fabrication of metal crossover or organic field effect transistors as well as contact resistance measurement of metal-semiconductor junctions.

## 1. Introduction

The use of printing technologies for electronic applications has received growing interest in industry as well as various fields of research during recent years. Whereas conventional microelectronics minimizes the cost of devices by miniaturization, printed electronics can produce large-area patterns with high throughput at very low cost. Printing technologies are especially suitable for low-cost manufacturing of flexible, light-weight and large-area applications [1]. Printing has been used recently to fabricate electronic devices such as diodes [2], rectifying circuits [3], transistors [4], solar cells [5] or sensors [6].

Since conventional microelectronics is soon coming to its resolution limit, alternative approaches are needed to decrease manufacturing costs and fulfill other requirements of an information technology society. One potential solution for this challenge is the field of molecular electronics [7], where the atoms and molecules would themselves serve as electronic components. Recently, electron-beam lithography has been applied to fabricate high resolution patterns for instance for electrical characterization of biomolecules [8, 9]. Recent improvements in high throughput, high resolution patterning using printing techniques also opens promising ways also for purposes of molecular electronics [10].

Nanoimprint lithography (NIL) is a promising high throughput and high resolution patterning technology which allows the fabrication of devices for various fields, such as electrical, optical, photonic and biological applications [11]. One example of electrical applications is an organic field-effect transistor (OFET) fabricated using NIL [12, 13].

It has been demonstrated that by optimizing NIL process feature size can be reduced to 20 nm [14].In addition, it has been shown that NIL technology can be transferred to a continuous roll-to-roll imprinting process for high-speed, large-area nanoscale patterning when flexible moulds are used instead of conventional stamps [15]. For this purpose silicon stamps can be replicated into nickel plates which are compatible with a roll-to-roll manufacturing process if the polarity of silicon template for the nickel shim is inverted [16, 17].

Microcutting is another method that has been successfully used for patterning sub-micrometer features of metal [18] as well as ceramic or conducting polymer [19, 18] on a polymer substrate. For instance a vertical-channel OFET was demonstrated using this approach [20]. Even as small as 100 nm metal lines can be obtained using the microcutting method [18].

One challenge in roll-to-roll production of electronic products is the accurate alignment and patterning of microscale structures while maintaining high throughput, low cost fabrication. One approach that can be taken is to define the size critical features first, followed by high speed, low resolution processes, but this approach can easily fail due to registration errors from layer to layer. These challenges potentially can be overcome by combining fast low resolution patterning with roll-to-roll fine resolution microcutting. For example coarse patterning by shadow mask evaporation or by resist printing and wet etching can be followed by NIL stamping or microcutting in order to

define final microelectrodes.

After definition of microelectrodes, further layers can be deposited onto these electrodes in a self-aligned way. The authors have for example previously demonstrated that well-defined dielectric patterns can be fabricated on narrow wires using Joule heating [21]. Such dielectric patterns are required for instance for making passivation layers required when making vias for 3D-wiring [22], for defining gate dielectrics in OFET devices, or for passivation of current distribution grids for large area devices.

Here, we demonstrate realisation of the combination of coarse patterning followed by microcutting and self-aligned passivation. We define a low resolution metal pattern and subdivide this into smaller patterns by pressing a stamp into the pattern, then align dielectric onto a narrow electrode strip using Joule heating [21]. We discuss some of the issues that need to be addressed to perform the patterning successfully, such as stamp geometry and fabrication. We evaluate fabrication of the silicon stamps using different approaches and compare hot embossing to room temperature NIL microcutting. The presented structure is suitable for fabrication of metal crossovers as well as OFETs.

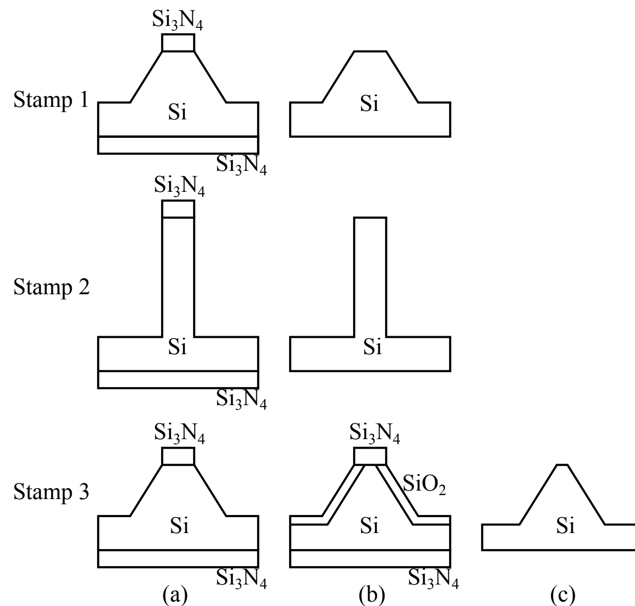


**Figure 1.** Fabrication of the stamps. The first set of the stamps were fabricated using a $Si_3N_4$-mask and wet etching. Second set of the stamp was etched with RIE. The fabrication process for the third set was similar to the first one, but after the wet etching step silicon was oxidized, and finally the $Si_3N_4$-mask and $SiO_2$ were removed.

## 2. Experimental details

All the materials were purchased from Sigma-Aldrich unless otherwise noted. The dielectric was a solution of poly (4-vinylphenol) (PVP) and suberoyl chloride (SC) formulated in propylene glycol monomethyl ether acetate (PGMEA) as described previously [21].

A 125 µm thick heat stabilized poly(ethylene terephthalate) (PET, Melinex ST506 from DuPont Teijin Films; melting temperature $T_m$= 255 °C, glass transition temperature $T_g$= 78 °C ) film was used as a substrate. Cross-shaped gold or copper conductors of a thickness of 50 nm were deposited onto the substrate using electron beam evaporation and a shadow mask (see figure 2). The same procedure was used for evaporation of metal crossovers with exception of the copper thickness being 100 nm (see figure 2 column II).

Silicon stamps were structured using UV-photolithography and different etching techniques. Two micro blades (presented in figure 2) were separated by a gap of 10, 30, 70 or 150 µm. Directions on blade were selected so that parallel lines are in <110> direction and other lines in <100> direction on (100) wafer. Each 7 × 7 $mm^2$ stamp contained one large blade pair. Three sets of blades were fabricated. Fabrication processes of the blades are illustrated in figure 1.

The first set (figure 3, stamp 1) of stamps was fabricated using a $Si_3N_4$-mask and wet etching using Potassium hydroxide (KOH) chemistry. As patterns were exposed along proper crystallographic directions, KOH-etching revealed smooth well defined [111]-

planes that formed sidewalls of parallel lines and [110]-planes that form sidewalls in other parts of blade. KOH-etching showed a very low etch rate to <111>-direction but some etching occurred to <110>-direction. This anisotropic etching reduced the linewidth of the blade making it sharper. This can be seen in figure 3. Linewidth reduction however put an ultimate limit to etch depth since for every etched micrometer the linewidth was reduced by 0.45 μm. In the first stamp batch etching depth was targeted to 2.8 μm.

The second series of stamps (figure 3, stamp 2) was made using reactive ion etching to realise a well defined structure where upper edges of the line form two sharp blades. In the RIE-etch structure width and depth do not correlate with line direction and therefore the freedom in blade design is greater.

For the fabrication of the third batch of stamps (figure 3, stamp3), we used a similar process to the first batch but a longer KOH-etch was performed to achieve deeper structures that were expected to cut better. After KOH-etch the $Si_3N_4$ covered wafer was cleaned and thermally oxidized. Here $Si_3N_4$-acts as a diffusion barrier that limits oxidation mainly to <111> and <110> directions depending on direction of line. After oxidation both $Si_3N_4$ and $SiO_2$ were removed in buffered hydrofluoric acid. Thermal oxidation and oxide removal were subsequently performed to reduce the linewidth of the pattern and make a sharper blade.

The second and third series of stamps were treated with fluorosilane anti-adhesive coating (Optool DSX, Daikin Industries). Prior coating, the stamps were activated 10 minutes in oxygen plasma. 0.1-0.3 wt% of Optool in perfluorohexane was applied on the stamps by spin coating 40 s with rate of 500 rpm. The coated stamps were heat treated 1 hour at 60 °C, and finally the residues of the coating was rinsed away with perfluorohexane.

Scanning electron microscopy (SEM) was used to assess the blade dimensions. The height of the blade was measured with a stylus profilometer (Veeco Dektak). Embossed patterns were imaged with an optical profilometer (Veeco Wyko NT1100) and an optical microscope (Olympus BX51) using brightfield setting, a reflected illuminator, objective lenses (Olympus MPLAN 5×/0.10 and 100×/0.90), and a digital camera (ARTRAY ARTCAM).

The procedure for fabricating a thin film transistor (TFT) platform or metal crossover is illustrated in figure 2, columns I and II, respectively. For this purpose we patterned electrodes by pressing a silicon stamp into PET substrate coated with a low resolution cross-shaped pattern of metal electrodes (figure 2(a)). The stamp is pressed into contact using a mask aligner (EVG620, EV-Group) equipped with NIL-tool or a manual press (Rondol 10 Tonnes Bench Hand Press). The stamp, having patterned sharp edges, separates a narrow electrode from the roughly patterned metal structure (figure 2(b)).Since the low resolution pattern is large compared to the separation of cutting blades, the alignment of the stamp is not critical.

For dielectric alignment, polymer dielectric is applied on the separated electrodes by spin coating at a rate of 2000 rpm. Subsequently an electrical current is passed through the narrow conductor in order to cure the insulator locally. The uncured insulator was

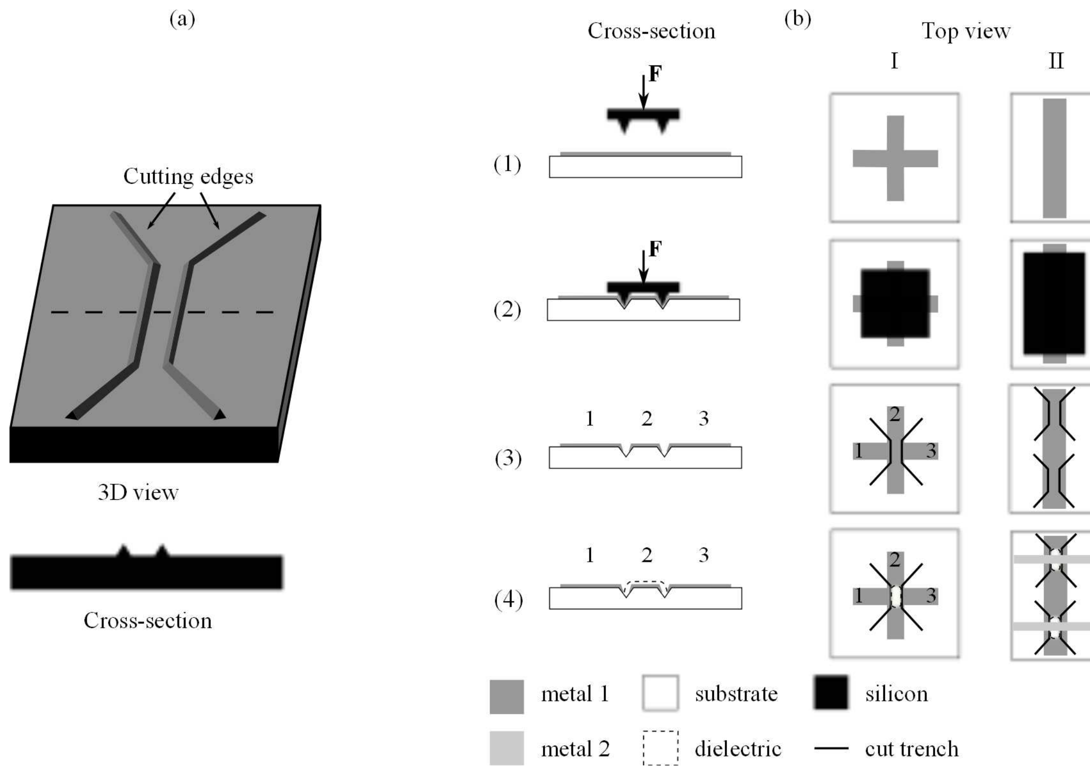


**Figure 2.** (a) Stamp topography. (b) A method to fabricate planar electrodes. Left column, cross-section; right column, top view. Column I, fabrication of thin film transistor platform; column II fabrication of metal crossover. (1-2) The silicon stamp is pressed into contact to cross-shaped gold electrodes (3) separating three electrodes. (4) A dielectric layer is patterned on the narrow electrode by Joule heating, and in the case of metal crossover, electrode is deposited on the dielectric. Note that the separation between the blades is not to scale with the electrode pattern. The width of the electrode is between 7 and 100 times the blade separation width. This enables the use of low resolution alignment during the stamping process.

then rinsed off with the same solvent used for the solution deposition of the dielectric. As a result the cured dielectric is localized on the narrow electrode (figure 2(c)). In the case of 3D wiring (figure 2(c), column II) the second layer of conductor could then be deposited on top of the dielectric. This Joule heating method for dielectric deposition is described in more detail in a previously published paper [21].

The electrodes were prepared by two methods - microcutting by hot embossing in the solid state and microcutting via NIL-tool - to provide a comparison of techniques. The hot embossing experiments were carried out with a manual press and chemically etched silicon stamps having gap sizes of 10 and 30 µm. The preferred embossing temperature for semicrystalline polymers thereby was between their glass transition temperature $T_g$ and melting temperature $T_m$ and around $T_g$ for amorphous polymers [18]. The PET substrate used here is semicrystalline and embossing was carried out at 115 °C. A force of 3 kN was applied for 60 minutes. After embossing the temperature was decreased to 70°C, which is below the glass transition temperature of PET. Finally

the load was removed.

In the microcutting experiments with the NIL-tool, the metal electrodes were separated by a mask aligner pressing the stamp to substrate at a force from 1.7 kN to 1.8 kN depending on the blade and the pattern design. In contrast to the hot embossing experiments described above, the electrode separation was carried out in room temperature. The imprinting time was 10 s. The experiments were carried out with all stamps and gap sizes.

To fabricate the TFT platform three layers of SC/PVP solution was spin coated onto the patterned electrode with a rate of 2000 rpm. Subsequently, an electric current of 37 mA for 30 μm wide conductor was passed through the conductor after each spin coating step. The curing times for the layers were 1, 2, and 5 minutes, respectively. The uncured dielectric was rinsed off after each curing step using the same solvent it was deposited on.

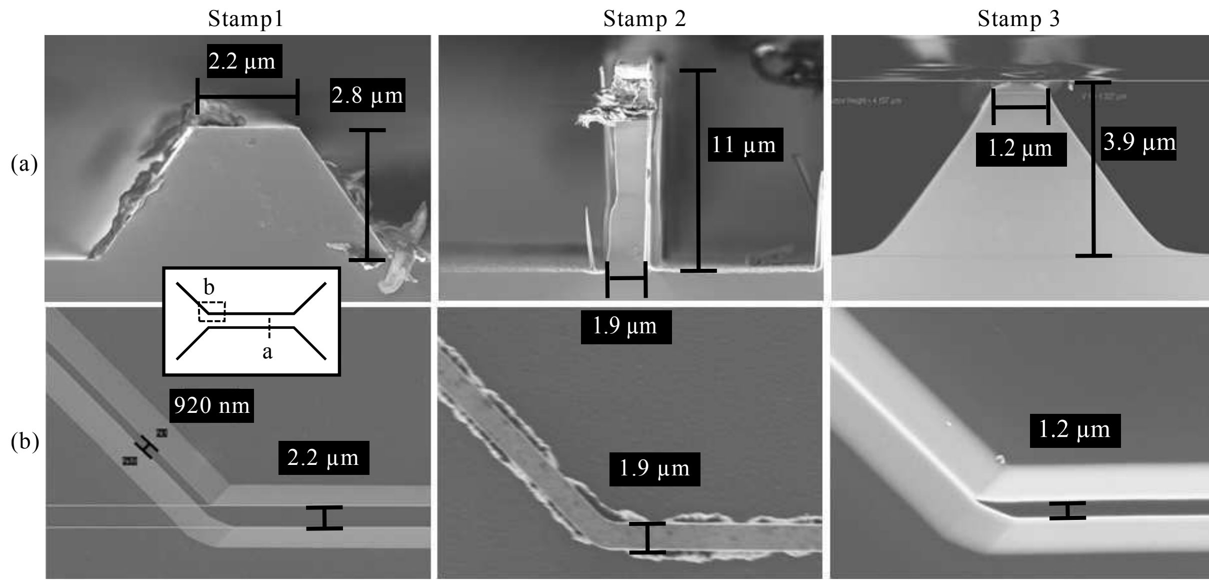


**Figure 3.** SEM images of the stamps. (a) cross section profile and (b) top view of the cutting blade. Inset: schematics of the stamp.

## 3. Results and discussion

Figure 3 shows SEM images of the fabricated stamps. The inset of the figure 3 presents the schematic structure of the stamp with the locations of the cross section (figure 3(a)) and top (figure 3(b)) views of the blade. Contamination that appears in the micrograph of the cross section of stamp 1 results from the embossing process, since the stamp was imaged after the experiments. To avoid contamination stamps 2 and 3 were coated with an anti-adhesive coating.

From the micrographs it is evident that the height of the KOH-etched stamp 1 is 2.8 µm, which was close to the maximum that can be achieved by etching. The width of the structures at the parallel part is 2.2 µm and at the diagonal part is 0.92 µm (see figure 3). The height and the width of the blade limit the cutting capability of the stamp. The plastic substrate deforms onto the shape of the stamp, and the thin metal layer is stressed upon the force of the stamps until it breaks. If the pressure created by the tip of the blade is sufficiently high to deform the plastic, the metal breaks when it has been stressed over the fracture point. The strain durability of the metal is dependent on the film thickness. The strain durability reported for an approximately 60 nm thick gold film is 1 % [23]. This value is dependent on the material, metallization method and width of the film, so it can be only used as an approximation for these films. However, the maximum strain of stamp 1 defined by the plain geometry is 60%. This is significantly more than the strain durability of the thin gold film. In addition, the height of the stamp is also sufficiently high to bring the metal to its fracture point. Therefore, the limiting factor for the successful microcutting is the pressure defined by the width of the blade.

Stamp 2 was defined by was anisotropic RIE-etching to achieve a blade of a higher

aspect ratio. The resulting height and the width of the created tip were 11 μm and 1.9 μm, respectively. The blade is thus sufficiently high to bring the metal to the breaking stress. However, there is a burr left from the process near the edge (see figure 3(b) and Supplementary material), which increases the contact area between the tip and the substrate and thus decreases the local pressure.

In the case of stamp 3, the fabrication process used for stamp 1 was continued by oxidation to overcome the limitations of the first stamp design and retain the quality of the structure. In this way higher and sharper blades were obtained. The oxidation creates structures that are 3.9 μm high and a blade is 1.2 μm wide at the parallel and tens of nanometres at the diagonal part of the stamp (see figure 3).

Hot embossing experiments were performed using stamp 1. Note though that because the polymer material is heated only slightly above its glass transition temperature, the flow of the polymer is relatively low, thus requiring a relatively large embossing time to ensure sufficient microcutting.

We were able to microcut the electrode after 1 h hot embossing. Since the blade of stamp 1 is comparatively blunt (see figure 3 (a)), the pressure needed to decrease the embossing time would have been too high for the fragile silicon stamps not to break. Note also the adhesion of the metal (in this case copper) to the PET surface was relatively low, thus, a thin layer of copper adhered to the stamp during hot embossing. This can be seen in microscope images displayed in figures 3 (a) and (b). The electrodes are slightly translucent resulting from small holes in the metal as some material was transferred to the stamp. Furthermore, heating during embossing oxidised at least partly the copper. This was most pronounced near the microcuts. As a result, the narrow electrode, which is the most critical element of this architecture for successful Joule heating patterning, is fully oxidised limiting the embossing time that could be used.

Figure 4 shows the microscope images and profile of a hot embossed sample. The height of the embossed structure is 2.1 μm(see figure 4), which is 75 % of the blade height (2.8 μm) of the stamp. This can have various reasons. On the one hand, the flow of the polymer substrate in the solid state is hindered, thus complete transfer of the relief structures can be challenging. An additional effect may result from the fact that the stamp and the substrate are after the embossing step first cooled below the $T_g$ of the substrate. As a consequence the plastic is hardened to the shape of the cutting tool. Furthermore, the substrate is coated with a metal layer, which furthermore retrains the polymer flow. The origin for the rounded shapes between the two parallel microcuts and the surface roughness of the embossed sample, seen in the profile image, is probably due to the poor adhesion of the metal alluded above. The yield of successful microcutting was 1/2 showing a leakage of less than 1 nA at 15 V. Leakage currents are presented in Supplementary material.

The Joule heating process defines the quality that is required for the narrow electrode. The width and thickness of the electrode should be even, otherwise there will be local spots were the temperature might increase over the $T_g$ of PET leading to a break-down of the electrode. The oxidation of copper changes the resistivity of the

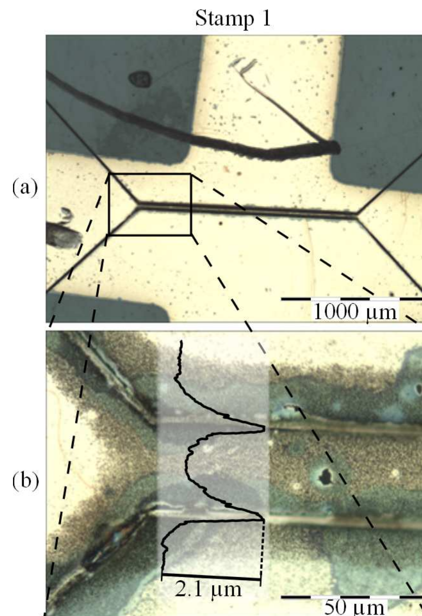


**Figure 4.** Hot-embossed copper electrodes with stamp 1 on PET substrate. Microscope images with (a) 5× magnification and (b) 100 × magnification including the profile of the microcut imaged by optical profilometer.

conductor. Unevenly oxidized conductor behaves similarly as a geometrically uneven conductor. The oxidation could be overcome by using gold electrodes instead of copper. However, the adhesion of the electrode still would need to be increased to prevent transfer to the stamp.

Figure 5 shows the microscope images and the corresponding profiles of the microcuts produced using the NIL process. The resulting microcuts using stamp 1 is presented in column I in figure 5. The height of the imprinted structure is 0.5 µm (see figure 5 (c)), which is significantly smaller than the blade height of the stamp as well as the feature produced by hot embossing. This is very likely due to the low temperature used in the NIL process. Also, the force applied to the stamp was only 60% of the force used in hot embossing experiments. The yield of the microcutting using NIL-tool and stamp 1 was low. The separation was mostly uncompleted at the diagonal part of the stamp.

Microscope images and the profile of the microcut copper conductor patterned by stamp 2 and NIL process are shown in figure 5 column II. The profile of the microcut could not be obtained and is not presented in the figure 5 due to the resolution limit of optical profilometer. However, the height of microcut was determined to be 9 µm by using SEM (see Supplementary material). It is also evident from microscope and SEM images that the cuts produced with stamp 2 produce the deepest and widest relief structure. The width of the relief structure is not only determined by the actual width of the blade width, but it is the depth which the stamp is pressed into the structure under patterning. However, the yield of the microcutting process for this stamp was not possible to define; experiments were made with different stamps of design 2, and

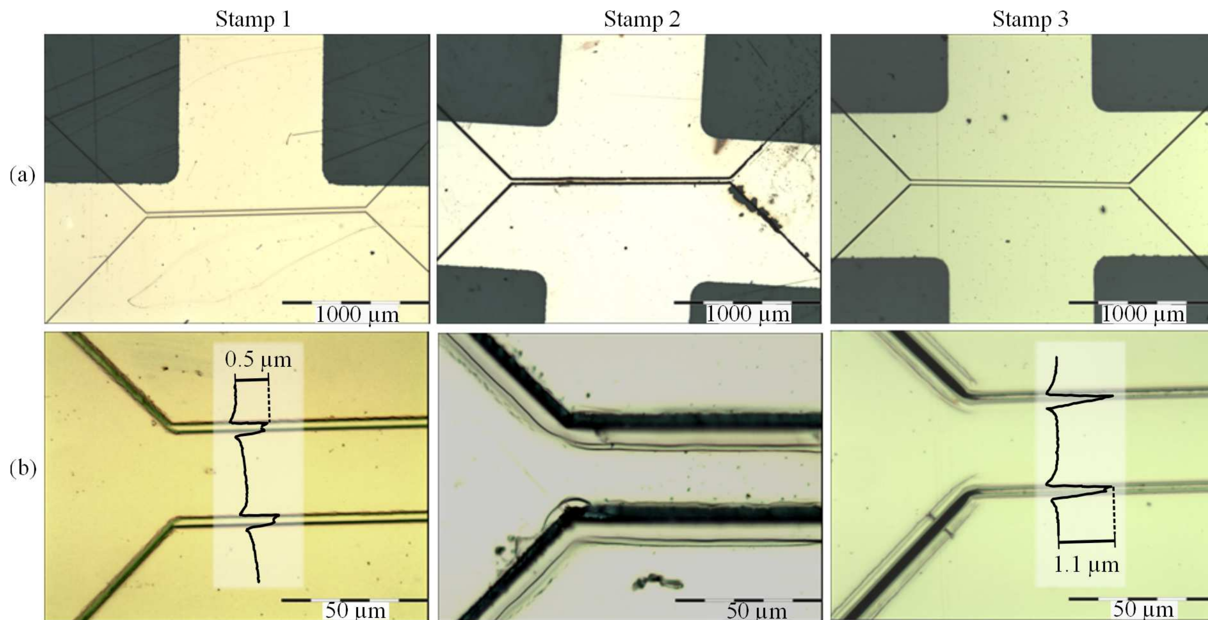


**Figure 5.** Copper electrodes nanoimprinted with the stamps 1 and 2, and gold electrode nanoimprinted with stamp 3 on PET substrate. Microscope images with (a) 5× magnification and (b) 100× magnification including profiles of the microcuts imaged by optical profilometer.

the quality of the stamps was variable. From figures 5(a) and (b) it is obvious that the resulting microcut is of too low quality to produce a uniform temperature at the conductor during the Joule heating process. This is due to the burr left at the blades (see Supplementary material).

The best results were obtained using stamp 3 and the NIL-tool. The yield of microcutting was 55/78 on gold. However, some of the individual stamps had a yield of 100 %. The difference between the stamps seemed to be caused by the roughness at the outline of the stamps. The depth of the cut is 1.1 µm and the cut is clean as can be seen in figure 5. The gap size did not have significant effect on the microcutting, thus only electrodes patterned with stamp having 30 µm separation between the blades is presented in the figure 5. The leakage currents between the separated electrodes were on the order of tens of picoamperes at 15 V. Leakage currents are presented in supplementary material.

In the microcutting application the substrate does not need to conform to the shape of the stamp precisely. The only critical parameters are the distance between the blades and the surface roughness of the electrodes. Patterns fabricated with hot embossing conform to the shape of the blade more accurately than microcuts created with NIL-tool. The NIL-tool microcutting needs a stamp with higher aspect ratio blades. Thus the yield in NIL-tool microcutting is more dependent on the stamp topography than in the hot embossing process. The disadvantages of hot embossing methods are the long processing times which were exceeding 1 h in our experiments, the high surface

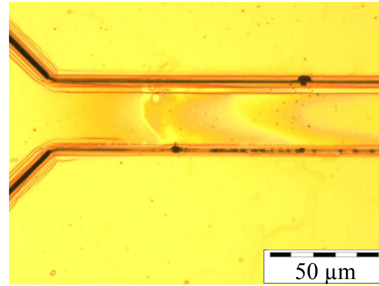


**Figure 6.** Applications for microcutting and Joule heating. 50 × magnified microscope imagesofadevicewithaligneddielectriconanarrowconductor.The separation betweenthepatternsis30 µm.

roughness that results during the pattern transfer and the oxidation of metal electrodes due to the need for use of elevated temperatures. MicrocuttingwiththeNIL-tooldoes not sufferthedrawbacksthehotembossingmethodhas;cleancutscanbeproduced, the resulting, patternedmetalsurfacesaresmoothandtheprocessingtimesareshort, only 10s.Furthermore,thequalityoftheelectrodespatternedusingtheNIL-toolis sufficiently high for dielectric alignment using Joule heating. MicrocuttingwithNIL-tool thus appear more suitable for future mass production than patterning via hot embossing.

To illustratethecompatibilityofmicrocuttingprocessbyNIL-toolandJoule heating, TFTplatform was fabricated.Figure6showstheTFTplatformon patterned goldelectrodes.ThreelayersofPVPdielectricwerealignedontopofthe micropatterned 30 µm wideelectrodepatternedusingNILtoolandstamp3.

## 4. Conclusions

We have compared microcutting by hot embossing in the solid state and microcutting using an NIL-tool, in order to pattern metal electrodes on a PET substrate. Although the hot embossed patterns conform to the shape of the blade more precisely than microcut patterns using a NIL-tool, the NIL-tool is a more promising approach to pattern metal electrodes on plastic substrates. The processing time is only 10 s whereas time needed for hot embossing is more than an hour. In addition to the short processing time the surface of the electrodes is smoother after patterning using the NIL-tool than what is achieved by hot embossing. Also, no heat needs to be applied on the surface during microcutting. As a conclusion, microcutting via NIL-tool is a promising patterning tool with the potential for up-scaling whereas hot embossing suffers from processing parameters that are less compatible with the Joule heating process.

For our investigations we compared three different silicon stamps: KOH etched, RIE etched and combination of KOH etch and thermal oxidation. The plain KOH-etched stamps suffered from the wide blade resulting into a relatively low local pressure on the substrate during pattern transfer. The RIE etching process did not completely succeed leading to unsatisfactory patterns with a burr left near the blades, thus decreasing the cutting pressure. To achieve higher and sharper blades, KOH etched stamps were thermally oxidized. The yield of pattern transfer by microcutting was highest with this approach and the patterned electrodes were suitable for Joule heating.

In addition to microcutting, dielectric patterns were successfully aligned on 30 μm wide micropatterned electrodes using Joule heating method. Combination of proposed microcutting and dielectric alignment methods makes a versatile toolkit which can be integrated with existing mass manufacturing processes. Our approach is suitable for the fabrication of metal crossover or organic field effect transistors with customized channel length and width.

## 5. Acknowledgments

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