Svetozar Brousev
High-Performance LC-VCOs and their Analysis using Time-Varying Root-Locus

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Abstract

A stable time reference is crucial for the proper operation of communication systems, digital electronic circuits, banking systems, etc. The time reference provides synchronization between events occurring in most of the systems built by humans. A realization of precise time reference is critical for the everyday life and it has attracted research from different prospective. Electronic circuits, like any other system, need an appropriate time base in order to synchronize internal events with the external world to guarantee proper operation. A precise time (frequency) reference is necessary for complex systems involving digital processing and communication with other systems. A perfect time base is physically impossible to realize, and thus the problem reduces to how much imperfections the system can tolerate, and how much is the impact of an imperfect reference.

The time (frequency) reference in wireless communication systems is realized by an oscillator (or Voltage-Controlled Oscillator (VCO)). The oscillator produces repetitive signal (sinusoidal or square-wave) whose transitions are used for synchronizing the building block of the system. Noise and physical imperfections of the oscillator components causes instabilities of the timing transitions, which are seen as jitter in time domain, or phase noise in frequency domain. The time (frequency) instabilities degrade the quality of signal transmission and reception in communication systems. Thus, the generation of stable reference is a primary issue in communication units. The unavoidable instabilities should be suppressed to a tolerable level for proper system operation. In addition, the ever growing demand for wireless communications requires new methods and engineering solutions for building high-performance and low-cost oscillators.

The research in the area of oscillators and VCOs has been in the focus for at least the past 30 years, but the area still offers a wide range of improvement opportunities. New silicon technologies, new materials, and new radio architectures demand different performance metrics from the VCOs, which inspires continuous circuit development. However, circuit solutions that are applicable in one scenario may become sub-optimal in another scenario. On the other hand, theoretical studies on frequency instability and phase noise have tried to explain the physical aspects in the noise generation. The goal of the theoretical studies is to provide design guidelines for low-noise oscillators, or accurate prediction of phase noise in computer
simulation environment. The work presented in this thesis focuses on \( LC \)-VCOs, which can be divided into:

- Circuit-based approach centered around innovations for improving the oscillator performance,
- Theoretical-based approach explaining physical phenomena in oscillators.

This thesis proposes a fourth-order dual-band VCO as a circuit-based solution that mitigates the inherent tradeoff between wide tuning range and low phase noise. A second circuit-based approach proposed in the thesis is a programmable \( K_{\text{VCO}} \) concept that achieves performance enhancement and provides reconfigurable opportunities. We show that both circuit approaches provide competitive state-of-art performance. We argue that the next generation VCOs would utilize the increased computation possibilities of modern digitally-intensive CMOS technologies, and they will utilize more complex than second-order resonator to fulfill the multiple system requirements. In this respect, both circuit approaches contribute to the development of modern VCO architectures.

This thesis develops a Time-Varying Root-Locus method, which is central theme on the theoretical-based approach. The method provides additional insights to the \( LC \) oscillator operation. The thesis shows the utilization of the method for comparing different \( LC \) oscillators, for evaluating critical parasitic components associated with the \( LC \) oscillators, and for estimating the effective oscillator \( Q \)-factor and its deterioration depending on oscillator topology and design variables.
Preface

The research work presented in this thesis was carried out at the Department of Communications Engineering (DCE), Tampere University of Technology (TUT), Finland. The research work was done in number of projects with industrial partners, such as IBM Microelectronics, Texas Instruments, and Infineon Technology AG, who also financially supported the research developments. During a 2-year period (1.1.2008 – 31.12.2009), the research was also financially supported by Tampere Doctoral Programme in Information Science and Engineering (TISE), and by the Academy of Finland (under Project no. 129077, “Hybrid Analog-Digital Signal Processing for Communications Transceivers”), which are gratefully acknowledged.

Foremost, I would like to express my gratitude to my supervisor Prof. Nikolay T. Tchamov for providing the great opportunity to work in the area of RF integrated circuits. His guidance and continuous support through the years has encouraged me to go through the long dissertation path. The time he spent discussing with me various research ideas has been invaluable for the outcome of my research.

I would like to thank Dr. Ivan Uzunov for his insightful advices and for constructive remarks that he was always sharing with me. I am grateful to Prof. Mikko Valkama and Prof. Markku Renfors leading the Department of Communications Engineering and for creating a good atmosphere for research. Special thanks to Tarja Erälaakko, Sari Kinnari, Kirssi Viitanen, and Ulla Siltaloppi for helping me with practical things and everyday matters.

I would like to express my gratitude to my thesis pre-examiners Assoc. Prof. Svante Signell from Royal Institute of Technology, Sweden, and Dr. Babak Soltanian from Quantenna Communications, CA, USA, for their insightful comments that helped me to improve the thesis. I also would like to thank Prof. Stephen I. Long from University of California, Santa Barbara, USA, for agreeing to act as an opponent on my dissertation defense.

Furthermore, I would like to thank to all personnel at DCE for supporting a friendly working environment. Above all, I would like to thank all my former and present colleges in the RFCC group, with whose we had challenging times in numerous occasions, but we managed to stay also friends. Special thanks to Tapio Lehtonen, Pekko Ruippo, Sami Sipilä, Kim Östman, Kari Rantala, and many others.
I thank all my friends in Tampere that created a unique atmosphere outside the university, and in particular Stanislav, Nikolay, Vladislav, Mihail, Kostadin, and many others.

Finally, I wish to thank my family for their continuous support and inspiration. I can only say a big thank you to my parents, Irena and Sasho, who always know how to encourage me in difficult times; to my brother Tihomir, who is more than a brother to me; to my little nephews Sashko and Veni, who never let me forget that there is another side of the life. Last but no least, I express my special thanks to Juja for her unconditional love.

Svetozar Broussev

Tampere, April 2012.
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Publications

A. List of publications

The thesis is a monograph and it is based on the following publications. In the text, these publications are referred to as [P.1], [P.2], … , [P.7].


B. Author’s contribution

The author’s contribution has been crucial in all publications listed above.

In [P.1] (Chapter 2) Prof. Tchamov proposed a dual-band VCO architecture that avoids the typical (at the time) switches in LC resonator. The author was responsible for the design, optimization, implementation, and measurements of the VCO that fulfills GSM specifications. Later, Dr. Uzunov joined the team, and he derived the equations for synthesizing the resonator components based on specified angular frequencies (Table 2-I), and he plotted the root-locus diagram presented in Subchapter 2.3. The author found the relationship between the angular frequencies of the two frequency bands, which allows a tradeoff evaluation and reveals practical limitations in the design of 4th-order resonator. In addition, the author evaluated the $Q$-factor of the 4th-order resonator and proposed a graphical-based design of the resonator.

Chapter 3 presents an extension of the 4th-order resonator concept realized with tapped inductor. The theoretical background of the modified resonator presented in Subchapter 3.2 was developed jointly with Dr. Uzunov. The rest of the development was contributed by the author (frequency planning of the design example, tapped inductor modeling, the proposed inductor structure, root-locus investigation, design, and silicon implementation). Part of the theoretical investigation presented in Chapter 3 is published in an IEEE journal ([P.7]).

Publication [P.2] (Chapter 4) presents a high-performance LC VCO developed during a project with Infineon Technologies AG. The programmable $K_{VCO}$ concept was proposed by the author, including the large amount of the work on the design, implementation and measurements. Tapio Lehtonen helped in the VCO design under the author’s supervision.

The work on Time-Varying Root-Locus presented in [P.3]-[P.6] (Chapters 5-8) is developed by the author starting from the idea to extend the root-locus method towards the analysis of large-signal oscillators. Prof. Tchamov, and also Dr. Uzunov during the initial development of the TVRL, contributed with very valuable discussions and guidelines. Prof. Tchamov helped to structure the research in this area and his critical comments lead to various oscillator topology investigations and comparison. The work on extracting the effective $Q$-factor from the TVRL ([P.6], Chapter 8) originated from the author.
**List of Abbreviations**

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>AM-PM</td>
<td>Amplitude-to-Phase Modulation</td>
</tr>
<tr>
<td>BCL</td>
<td>Bias Control Loop</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar Junction Transistor</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer-Aided Design</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>CV</td>
<td>Capacitance-Voltage characteristic of a varactor</td>
</tr>
<tr>
<td>DCS</td>
<td>Digital Cellular Service (GSM frequency band)</td>
</tr>
<tr>
<td>FoM</td>
<td>Figure-of-Merit</td>
</tr>
<tr>
<td>FSSA</td>
<td>Fast Steady-State Algorithm</td>
</tr>
<tr>
<td>GSM</td>
<td>Global System for Mobile Communications</td>
</tr>
<tr>
<td>HB</td>
<td>Harmonic Balance</td>
</tr>
<tr>
<td>HF</td>
<td>High Frequency</td>
</tr>
<tr>
<td>IQ</td>
<td>In-Phase / Quadrature (for signal)</td>
</tr>
<tr>
<td>IR</td>
<td>Inner radius (for inductor)</td>
</tr>
<tr>
<td>IRAM</td>
<td>Implicitly-Restarted Arnoldi Method</td>
</tr>
<tr>
<td>ISM</td>
<td>Industrial, Scientific, and Medical (ISM) radio band</td>
</tr>
<tr>
<td>ISF</td>
<td>Impulse Sensitivity Function</td>
</tr>
<tr>
<td>JTAG</td>
<td>Joint Test Action Group (standard)</td>
</tr>
<tr>
<td>$K_{\text{VCO}}$</td>
<td>VCO tuning sensitivity, VCO Gain</td>
</tr>
<tr>
<td>LF</td>
<td>Low Frequency</td>
</tr>
<tr>
<td>LHP</td>
<td>Left-Half Plane (of $s$-plane)</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LU</td>
<td>Lower-Upper (decomposition)</td>
</tr>
<tr>
<td>MD-QR</td>
<td>Modified QR (decomposition)</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-Insulator-Metal (for capacitor)</td>
</tr>
<tr>
<td>MNA</td>
<td>Modified Nodal Analysis</td>
</tr>
<tr>
<td>MOM</td>
<td>Metal-Oxide-Metal (for capacitor)</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>MTAP</td>
<td>Multi-tapped (for inductor)</td>
</tr>
<tr>
<td>NMOS</td>
<td>Negative-channel Metal-Oxide-Semiconductor (transistor)</td>
</tr>
<tr>
<td>NPN</td>
<td>Negative-Positive-Negative (for BJT transistor)</td>
</tr>
<tr>
<td>NT</td>
<td>Number of Turns (for inductor)</td>
</tr>
<tr>
<td>PCF</td>
<td>Power Conversion Factor</td>
</tr>
<tr>
<td>PCS</td>
<td>Personal Communication Services (GSM frequency band)</td>
</tr>
<tr>
<td>PFTN</td>
<td>Power-Frequency-Tuning-Normalized (Figure-of-Merit)</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>PMOS</td>
<td>Positive-channel Metal-Oxide-Semiconductor (transistor)</td>
</tr>
<tr>
<td>PPV</td>
<td>Perturbation Projection Vector</td>
</tr>
<tr>
<td>PSS</td>
<td>Periodic Steady State</td>
</tr>
<tr>
<td>QR</td>
<td>QR decomposition (matrix $A$ decomposed as $A = Q \cdot R$)</td>
</tr>
<tr>
<td>QZ</td>
<td>Generalized Schur decomposition, or QZ</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RHP</td>
<td>Right-Half Plane (of $s$-plane)</td>
</tr>
<tr>
<td>SS</td>
<td>State-Space (for circuit description)</td>
</tr>
<tr>
<td>SSA</td>
<td>Semi-Symbolic Analysis</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>TR</td>
<td>Taping Ratio (for inductor)</td>
</tr>
<tr>
<td>TVRL</td>
<td>Time-Varying Root-Locus</td>
</tr>
<tr>
<td>UMTS</td>
<td>Universal Mobile Telecommunications System (UMTS)</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra Wide Band</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage-Controlled Oscillator</td>
</tr>
<tr>
<td>WCDMA</td>
<td>Wideband Code Division Multiple Access</td>
</tr>
</tbody>
</table>
List of Principal Symbols

$C$ Capacitance

$f_0$, $\omega_0$ Oscillation frequency

$f_{\text{offset}}$, $\Delta \omega$ Frequency offset

$f_{\text{norm}}$ Normalization frequency for matrix scaling before pole computation

$g_m$ Transistor transconductance

$g_{\text{ds}}$ Transistor drain-source conductance

$g_{\text{pass}}(\phi)$, $g_{\text{act}}(\phi)$ Time-varying passive (positive) and active (negative) conductance associated with cross-coupled pair oscillator

$g_{\text{eff},To}$, $g_{\text{act},To}$ Effective positive and negative conductance for one oscillation period

$H_{\text{sub}}$ Substrate thickness

$k$ Mutual coupling factor between adjacent inductors

$L$ Inductance

$P_{\text{DC}}$ DC power consumed by an oscillator

$Q$ Quality factor

$q_{\text{max}}$ Maximum charge stored in $LC$ tank ($= C \cdot V_{\text{max}}$)

$R_{\text{norm}}$ Normalization resistance for matrix scaling before pole computation

$R_{\text{norm,opt}}$ Optimum normalization resistance leading to the minimum condition number for computation of $\lambda_0$

$T_0$ Oscillation period

$Y$ Admittance

$Y(s)$ Admittance matrix for MNA circuit formulation

$Y_{\text{cp, pos}}(\phi)$, $Y_{\text{cp, neg}}(\phi)$ Time-varying positive and negative admittance of a cross-coupled pair

$Z$ Impedance

$\alpha(\tau)$ Modulation Function for the Impulse Sensitivity Function computation

$\varepsilon_{j,k}$ Oscillator node voltage change for $j$-th instant and $k$-th node
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\epsilon_{\text{max}}$</td>
<td>Maximum node voltage change between the selected data points</td>
</tr>
<tr>
<td>$\delta_{\text{PSS,max}}$</td>
<td>Maximum node voltage change between the original PSS data points</td>
</tr>
<tr>
<td>$\phi \equiv \omega t$</td>
<td>Normalized time (0 - $2\pi$)</td>
</tr>
<tr>
<td>$\Gamma(\tau)$</td>
<td>Impulse Sensitivity Function</td>
</tr>
<tr>
<td>$\Gamma_{\text{eff}}$</td>
<td>Effective ISF function</td>
</tr>
<tr>
<td>$\Gamma_{\text{eff,rms}}$</td>
<td>Effective $\text{rms}$ ISF function</td>
</tr>
<tr>
<td>$\gamma_n, \gamma_p$</td>
<td>Channel noise factor for NMOS and PMOS transistor</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>Condition number</td>
</tr>
<tr>
<td>$\kappa_0(t)$</td>
<td>Time-varying condition number for the computation of $\lambda_0$</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Pole spectrum</td>
</tr>
<tr>
<td>$\lambda_0$</td>
<td>Main pole responsible for oscillations</td>
</tr>
<tr>
<td>$\lambda_L, \lambda_C$</td>
<td>Inductive and capacitive ratio ($\lambda_L = \sqrt{L_a/L_b}$ and $\lambda_C = \sqrt{C_a/C_b}$)</td>
</tr>
<tr>
<td>$\lambda_{C,\text{min}}$</td>
<td>Capacitive ratio needed to achieve $(\omega_3/\omega_1)_{\text{min}}$</td>
</tr>
<tr>
<td>$\mathcal{L}$</td>
<td>Oscillator phase noise</td>
</tr>
<tr>
<td>$\rho$</td>
<td>Substrate resistivity</td>
</tr>
<tr>
<td>$(\omega_3/\omega_1)_{\text{min}}$</td>
<td>Minimum achievable frequency spacing in dual-band VCO</td>
</tr>
<tr>
<td>$(\omega_3/\omega_1)_{\text{crit}}$</td>
<td>Critical frequency spacing that ensure proper dual-band operation</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(\cdot)^{-1}$</td>
<td>Inverse</td>
</tr>
<tr>
<td>$</td>
<td>\cdot</td>
</tr>
<tr>
<td>$|\cdot|_2$</td>
<td>Two-norm of an eigenvector</td>
</tr>
<tr>
<td>$\text{det}(\cdot)$</td>
<td>Matrix determinant</td>
</tr>
<tr>
<td>$\text{Re}(\cdot), \Re(\cdot)$</td>
<td>Real part of complex variable</td>
</tr>
<tr>
<td>$\text{Im}(\cdot), \Im(\cdot)$</td>
<td>Imaginary part of complex variable</td>
</tr>
<tr>
<td>$\min(\cdot), \max(\cdot)$</td>
<td>Minimum and maximum of a function</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

1.1. Background and Motivations, Research Problems

The Voltage-Controlled Oscillator (VCO) provides a reference signal in transceivers to
down-convert the RF signal into a baseband signal during reception, and to up-convert the
baseband signal into an RF signal during transmission. The VCO frequency is adjusted to the
frequency of the desired signal during transmission or reception in direct-conversion receivers.
The integration of multiple communication standards within a single transceiver requires a
VCO with wide tuning range able to cover the target applications. The VCO should be adaptive
(reprogrammable) in order to serve the requirements posed by the different communication
standards, namely tuning range, phase noise, and power consumption. Realization of a VCO
with very wide tuning range is one option to satisfy the required frequency coverage. However,
a widely tunable VCO has in general poor phase noise performance [138]. The use of LC VCOs
is typical in transceivers, as they provide the best phase noise among the other classes of
oscillator. Unfortunately, typical LC oscillators reach their fundamental limits imposed by the
moderate $Q$-factor of the passive devices implemented on chip, and good signal quality and
wide tuning range cannot be simultaneously achieved. A solution(s) that breaks the tradeoff
between phase noise performance and wide tuning range is therefore needed.

A circuit-based approach to tackle the above-mentioned problem is to develop an oscillator
architecture that achieves wide tuning range without significantly deteriorating the oscillator
phase noise. In this direction, dual-band or multi-band oscillator topologies have been seen in
recent years to provide promising results. In addition, there is an increasing trend to use more
digital control and signal processing to enhance the oscillator operation and to help the inter-
operability of oscillators for multiple standards. The digitally-intensive trend is in line with
modern CMOS technologies, which are friendlier to digital processing rather than analog processing.

A theoretical approach fighting with the above-mentioned problem focuses on gaining deeper understanding of the phase noise mechanisms in oscillators. One way to combat the tradeoff between phase noise and tuning range is to minimize the internally generated noise in the oscillator. Despite the huge development on the oscillator noise theory, the origin of the noise and its conversion mechanism to phase noise are still not well understood, which is seen as number of different interpretation of phase noise mechanisms in the literature. More advanced noise theory relies on heavy mathematical apparatus giving limited guidelines for circuit optimization. On the other hand, designer-friendly phase noise theories are either over-simplified neglecting the time-varying noise properties, either too theoretical to lose the link with the physical interpretation. A different treatment of the problem is needed, which carries both physical meanings and analysis precision.

1.2. Objectives and scope of the research

The work presented in this thesis contributes to the circuit-based and to the theoretical-based approach to mitigate VCOs non-idealities and to improve their performance.

The goal of the circuit-based approach is to develop VCO architectures that break the fundamental tradeoff between low phase noise and wide tuning range. A dual-band VCO using fourth-order resonator is central to the circuit-based approach. The VCO architecture utilizes dual-resonance network to realize widely spaced oscillation frequencies with no penalty on VCO phase noise. Another circuit solution proposed in the thesis is a programmable $K_{VCO}$ concept, which allows re-programmability to adjust the tradeoff between phase noise and tuning range.

The goal of the theoretical-based approach is to gain deeper understanding into the oscillator operation, which would facilitate an optimization of the oscillator performance. The developed concept of Time-Varying Root-Locus (TVRL) is a central theme in the theoretical part of the thesis. As most of the theoretical oscillator analysis are either oversimplified, or either too theoretical, the proposed approach sits in between by obtaining precise numerical results while retaining their physical interpretation.
1.3. Thesis outline

A review of different methods to achieve dual-band or multi-band operation is given in Subchapter 1.4. Chapter 2 reveals the principle of the dual-band VCO architecture and presents specific technical details. The proposed dual-band concept is further developed in Chapter 3 for a tapped inductor, where the implications of combining all inductors into one single tapped inductor are evaluated. Chapter 4 is dedicated on a programmable $K_{\text{VCO}}$ scheme in $LC$ VCOs, which improves phase noise in communications standards with small tuning range requirements.

The rest of the thesis is dedicated on the theoretical analysis of oscillators. First, Subchapter 1.5 gives an overview of the existing methods for analytical and numerical analysis of oscillator phase noise. The concept of Time-Varying Root-Locus is introduced in Chapter 5, where the method also shows its capabilities for comparing $LC$ oscillator topologies. Chapter 6 makes more extensive oscillator comparison and extends the TVRL analysis towards VCOs. Chapter 7 shows the TVRL ability for analyzing parasitic components in oscillator. Chapter 8 uses the extracted roots from the TVRL algorithm to evaluate the $Q$-factor degradation in large-signal $LC$ oscillators. Finally, Chapter 9 concludes the thesis.
1.4. Review of circuit techniques for building dual-band (multi-band) VCOs

![Diagram of circuit techniques for dual-band or multi-band VCOs]

The problem to generate multiple frequencies with a single oscillator structure has bothered the academic and industrial community at least for the last decade. The reason is obvious – multiple communication standards should be covered in cost-efficient and in power-efficient way. Various solutions for building dual-band and multi-band VCOs have been proposed. Fig. 1.1 presents a block diagram summarizing the reported techniques in different categories. Starting from the trivial solution to use multiple oscillators, the research has gone through frequency synthesis techniques, and expanding lately towards modifications of the LC resonance tank. The modifications of the LC tank include switching of a resonance capacitor, switching of a resonance inductor or transformer, or employing a higher-order resonator. The LC tank modifications are represented in Fig. 1.1 as different methods due to their specifics. The techniques shown in Fig. 1.1 are briefly summarized in the following subchapters, where their advantages and shortcomings are underlined. The method presented in this thesis is based on the use of fourth-order LC tank, which is studied in details in Chapters 2 and 3, while Subchapter 1.4.5 summarizes the similarities and the differences between the proposed concept and other concept based on similar resonance tank configurations.
1.4. Review of circuit techniques for building dual-band (multi-band) VCOs

1.4.1. Standard solutions: array of oscillators; oscillator followed by frequency dividers

A multi-band frequency generator can be realized by combining the outputs of multiple VCOs, each covering specific frequency range (Fig. 1.2(a)). The solution called “array of oscillators” was demonstrated in [81], where numbers of single-band VCOs are connected in parallel, with only one VCO being operational at the time. The simplicity of this solution requires no huge implications for design, and each VCO core can be separately optimized for phase noise performance or power consumption. Furthermore, the frequency band selection is independent i.e. there is no interdependence between frequency bands, which could be a limiting factor in more advanced multi-band VCO structures. However, the occupied silicon area increases proportionally with the numbers of implemented VCOs. Combining the different VCO outputs may cause performance degradation compared to single oscillator. The oscillator array may be justified when limited numbers of frequency bands are targeted. In modern terminals, however, more and more communications standards are integrated, thus the array of oscillator becomes prohibitively expensive solution. Reference [171] presents a recently reported single-chip signal source employing as may as five separate VCOs in combination with frequency dividers and multipliers for covering a frequency range from 125 MHz up to 32 GHz. The occupied silicon area of $2.1\text{mm} \times 2.1\text{mm}$ does not include any additional block needed in typical transceivers, and thus it only confirms the area penalty associated with the oscillator array.

Another standard solution that is widely used in practice is a VCO followed by frequency divider(s) (Fig. 1.2(b)). The frequency divider(s) enhances the VCO phase noise performance due to the frequency division (6 dB phase noise improvement for division of two). The number of the covered frequency bands depends on the amount of frequency dividers utilized. However, one disadvantage of the divider solution is that the obtained frequency bands are related in
CHAPTER 1: INTRODUCTION

Frequency domain with an integer number (2, 4, 8, etc.) i.e. the frequency band selection is not arbitrary. Nevertheless, this solution is largely popular among dual-band/quad-band GSM transceivers due to the convenient frequency specifications of the GSM. The VCO usually oscillates at around 4 GHz, and the transceiver can easily cover the four standards using one and/or two frequency dividers. The VCO frequency tuning requirements are in general not tough to achieve, and an oscillator based on conventional second-order LC tank suffices. However, if a communication standard like Bluetooth / ISM (2.4GHz) is added to the quad-band GSM, then the frequency synthesizer should be architecturally different in order to accommodate those standards, thus the VCO-divider solution has a limited applicability. A mitigation of this problem is demonstrated in [42], where the first frequency divider is switchable and it can be programmed for a division-by-2 or for a division-by-3 operation. The frequency extension provided by the switchable divider in [42] covers the gaps in the tuning range in the typical VCO and divider topology from Fig. 1.2(b). The frequency dividers do not increase visibly the silicon area of the synthesizer, thanks to the fact that they can be build without on-chip inductors.

1.4.2. Frequency-synthesized generators, UWB generators

Single-band VCO combined with some frequency-translation technique (division, multiplication, mixing) can realize dual-band or multi-band generator. A realization of such principle is shown in Fig. 1.3, where frequency division and mixing is used to generate a reference signal with a frequency of $f_{osc}$ or $(3/2)f_{osc}$ [146]. The frequency translation technique requires additional blocks on the signal path, which increases the occupied silicon area. Furthermore, the additional blocks could deteriorate the phase noise performance of the system. Nevertheless, this technique provides certain flexibility for frequency planning of the whole system. The generation of two frequency bands in [146] allows reducing the tuning range of the VCO, thus decreasing the VCO Gain and improving its phase noise performance [138].

Further development of the frequency-translation idea is demonstrated in Fig. 1.4 for
1.4. Review of circuit techniques for building dual-band (multi-band) VCOs

Fig. 1.4. Block diagram of the continuously tunable IQ-VCO system based on single-band VCO and frequency translations.

realization of continuously-tunable oscillator system [60]. The continuously tunable signal generator shown in Fig. 1.4 avoids the required notch filter in the previous example, and provides three distinct frequency bands \((1/3) \cdot f_{osc}; (1/2) \cdot f_{osc};\) and \((2/3) \cdot f_{osc}\). A VCO with ±20% tuning range covers the gaps between the three bands, which results in ±50% frequency range covered by the entire frequency-generation system. Similarly to the previous example, the use of additional blocks for the dividers and mixers may deteriorate the system performance. Because the blocks used for the three bands are different, the performance of the system is different for the three bands, i.e. the behavior of the system is not equal throughout the tuning range.

Common problem for the frequency-synthesized architectures is the generation of spurious tones, which require special attention in the circuit design [60], [146]. These spurious tones are result of the mixer operation, which is a core component in frequency-translation technique (as shown in Fig. 1.3 and Fig. 1.4). A notch filter is used in [146] to suppress the unwanted spur at \(f_{osc}/2\). An IQ mixer is used in [60] instead of a notch filter, but the unavoidable quadrature error between the IQ signals still produces undesired spurs [60].

Other variations of the frequency-translation technique are often used in Ultra-Wide Band (UWB) generators [103], [164], [172]. The UWB standard defines 14 equally spaced frequency bands (Fig. 1.5(a)). The equal frequency separation between the bands allows using one VCO followed by a combination of dividers, mixers, and multiplexers. An example realization of UWB signal generator is shown in Fig. 1.5(b) [103], where the LO frequency generates 8448-MHz signal, which is situated between band #10 and #11. The LO signal, or its divide-by-2 replica (4224 MHz), is mixed with signals with frequency of \((264MHz + k \cdot 528MHz)\), where \(k\) is an integer from 0 to 3. The constant frequency shift of 264 MHz, which is also derived from the LO signal with dividers, brings the generated signal in the middle of the desired UWB band. The desired frequency band is selected by controlling digitally the two multiplexers. IQ mixers
Fig. 1.5. (a) UWB frequency bands; (b) realization of UWB generator based on single-band VCO and frequency translation technique [103].

and dividers are used for realizing pure frequency translation. Although the realization of IQ mixers and dividers is not problematic in modern CMOS technology, their use increases the occupied silicon area and the power consumption.

In summary, the frequency-translation technique for realizing multi-band oscillators is gaining popularity mostly in UWB systems. The large number of UWB bands justifies the design complexity, which is facilitated by the equal band spacing. However, the popular communication standards (GSM, UMTS, ISM) are not synchronized in frequency domain, thus a multi-band VCO targeted for GSM and ISM bands (for example) would face difficulties with the frequency-translation concept. Moreover, the additional blocks added after the VCO are increasing the phase noise floor at far-away offset, which would be hard to tolerate for the GSM standard. From this point of view, it is likely that the frequency-translation concept would be the main technique in UWB generator, but it will be hard to see its deployment in traditional GSM/UMTS/ISM synthesizers. The recent developments of frequency generators covering wide frequency range could be seen also as an extension of frequency-translation methods, where the number of multiplexers and mixers is reduced to minimum for achieving good phase noise [129], [139]. The omitted multiplexers and mixers require VCO with wide frequency range, which is realized in [129] by two separate VCOs in an “array of oscillator” style, whereas [139] uses a dual-band VCO. Nevertheless, the frequency generators in [129] and [139] do not report whether the far-away GSM phase noise specifications are met.

1.4.3. Switched resonator (switched inductor) concept

The main idea of the switched-resonator concept is to vary the resonator inductance by
1.4. Review of circuit techniques for building dual-band (multi-band) VCOs

Fig. 1.6. Switched resonator concept: (a) main idea; (b) simplified model of the switched resonator with $M_{SW}$ at cutoff region; (c) simplified model of the switched resonator with $M_{SW}$ at triode region.

switching-on or switching-off an MOS transistor, which determines the equivalent inductance in the resonator (Fig. 1.6(a)). With the MOS transistor $M_{SW}$ being in off-state, the total inductance of the resonator is approximately $L_{TOT} = L_1 + L_2$ and the low frequency band is selected. The high frequency band is selected by turning on $M_{SW}$, which corresponds to tank inductance of approximately $L_1$. The MOS transistor parasitic resistance and capacitance take part in the whole resonator, with on-state channel resistance $r_{SW}$ affecting the high-frequency band performance (Fig. 1.6(c)), and parasitic capacitance $C_{SW}$ affecting the low-frequency band performance (Fig. 1.6(b)). The channel on-resistance degrades the quality factor of the resonator and worsens the achieved phase noise at the high-frequency band. This problem can be partly solved by making the transistor $M_{SW}$ with large $W/L$ ratio ($r_{SW} \sim (W/L)^{-1}$), but this design technique also increases the parasitic capacitance $C_{SW}$ ($C_{SW} \sim W \cdot L$), which limits the tuning range of the oscillator. This interdependence underlines the main problem of the switched resonator technique – the need to balance resonator quality factor (respectively phase noise performance) with achievable oscillator tuning range. Even if a large $W/L$ transistor is used in the design, the quality factor would be always smaller than the quality factor of the native resonator. An advantage of the switched-inductor technique is the freedom to (almost) arbitrarily space the two frequency bands by designing the taping ratio $L_1/L_2$. Another advantage is the straightforward design and the possibility to utilize any of the performance-enhancing techniques applicable to single-band oscillators.

The switched-resonator technique was demonstrated in [168], which was further developed in [99] to realize four-band VCO with excellent Figure-of-Merit. The excellent phase noise result presented in [99] is achieved with the expense of very small tuning range, which only confirms the fundamental tradeoff associated with the switched resonator technique. The effect of the parasitic components of the MOS transistor to the performance of the oscillator is thoroughly analyzed in [169]. Various other implementations and modifications of the switched-resonator technique have been reported in the literature. For instance, a triple-band VCO is realized in [33] by shortening two sections of a differential inductor with two large
differentially-connected MOS transistors, which results in three overlapping frequency bands that realize a wide-tuning-range VCO.

In the switched-resonator category fall also oscillator architectures using in a MOS switch that shortens the secondary winding of a monolithic transformer (shown in Fig. 1.1 as separate technique). The principal idea is the same: to modify the equivalent inductance in the $LC$ resonance tank. Since the MOS switch is placed on the secondary winding, its impact on $Q$-factor, phase noise, and tuning range is reduced by the transformer ratio. The abovementioned drawbacks associated with the reduced $Q$-factor also takes place, and the tradeoff that the designer should make is the same. Example realizations of this idea are shown in [41], [56], [85], [141], and in particular [85] uses six secondary switched coils to realize three frequency bands, and therefore wide tuning range. The switched-capacitor shown in Fig. 1.1 is also a switched-resonator concept, but this technique is also used for single-band VCOs to realize wide tuning range. Since, within this thesis, it is assumed that a dual-band / multi-band circuit technique is a technique that provides two or more distinct frequency bands, the switched-capacitor technique, when used alone, cannot be assumed as a dual-band / multi-band circuit technique.

A partial mitigation of the problem with the degraded $Q$-factor in the switched-resonator concept is demonstrated in [153], where the MOS switch is placed in an inductor bridge configuration. The inductor bridge replaces the standard inductor in the $LC$ tank, and the MOS switch shortens two nodes of the bridge to change the effective inductance of the resonator. Since only part of the current passes through the MOS switch, the switch resistance has smaller impact on $Q$-factor compared to the conventional solution [153]. The inductor bridge, however, requires complex physical implementation, which may deteriorate the inductor $Q$-factor.

A hybrid architecture that uses the some of the properties of the switched resonator and some of the properties of the 4th-order resonator is demonstrated in [57].

1.4.4. Resonance-Mode switching

The resonance-mode switching principle is based on driving a differential $LC$ resonance tank in common mode and in differential mode [9], as shown in Fig. 1.7. The capacitor $C_f$ takes part of the resonance tank in differential driving conditions, but $C_f$ is not visible when common-mode oscillations are enforced. The system oscillates at two distinct frequencies depending on the driving conditions, thus realizing a dual-band VCO. The frequency spacing between the two bands is controlled with the value of $C_f$ capacitance. The resonance-mode switching principle is inherently limited to dual-band operation only, since there is no other fundamental mode that can be used.
1.4. Review of circuit techniques for building dual-band (multi-band) VCOs

The presence of $C_f$ decreases the amount of tank capacitance $C_o$ that can be controlled, thus the amount of frequency tuning for the differential-driven frequency band is potentially reduced. Possible solution for this problem is to replace $C_f$ with a varactor block. The varactor block, however, should not affect the principle of operation, since the typical differential varactor configuration has a virtual ground in between (the voltage control line), which will transform $C_f$ into a differential grounded capacitance, thus destroying the main idea.

The resonance-mode switching technique is demonstrated in [9] for the realization of 13/22 GHz VCO. Using appropriate bias switching, the oscillator core becomes a differential Colpitts topology in differential-mode drive, or it transforms into two three-point oscillators operating in common-mode conditions. Somewhat similar is the approach used in [170] where a dual-band millimeter-wave oscillator is realized using left-handed resonator. The dual-band generation is realized by enforcing even-mode operation or odd-mode operation of the resonator.

1.4.5. Fourth-order resonator concept and its variations (dual-mode, triple-mode, double-driven transformer)

A new class of oscillators based on increasing the order of the resonance tank has emerged in the literature. The increased order of the resonator displays two or more parallel resonances, which are utilized for frequency generation. One of the first demonstrations of this principle was developed in [P.1], and similar developments were followed by other IEEE publications. Chapter 2 is dedicated on the theory, design, and implementation of [P.1], while in the following are summarized approaches that are similar to [P.1].

Briefly, the 4th-order resonator gives a possibility to realize dual-band oscillator with frequency spacing between the bands that is controllable by the circuit designer. Although the frequency spacing cannot be arbitrary chosen (realization of the passive components imposes practical difficulties), the possibility to do a frequency-band planning offers design flexibility.

A 4th-order dual-band VCO utilizing a transformer instead of four inductors is presented in [11], with simplified representation given in Fig. 1.8. The primary and secondary coil ($L_1, L_2$) of
Reference [11] proposes two ways to build an oscillator around the proposed resonator – as one-port oscillator (Fig. 1.8(b)), or as two-port oscillator (Fig. 1.8(c)). The one-port oscillator is essentially a negative-$G_m$ architecture (used in [P.1]), and the desired mode of oscillation is achieved by placing $-G_m$ at certain port. The two-port oscillator utilizes the resonator in a feedback, which gives different properties of the oscillator itself. The major behavioral difference between the two oscillator configurations is that the two-port configuration always produces the desired oscillation frequency [11], whereas the one-port configuration imposes upper and lower limit of $-G_m$ to produce the desired frequency band ([P.1], [11]). However, the worse phase noise obtained in the two-port oscillator [11] explains why the two methods still exists in practice. In summary, the one-port oscillator offers better phase noise, whereas the two-port oscillator solves the issue of unwanted oscillations at the other frequency band. Recently, a frequency-band-limited negative-$G_m$ stage has been proposed to prevent oscillations at the unwanted frequency band, or even to select the desired parallel resonance from a 4th-order resonator [26].

The two oscillation frequencies achieved by the transformer-based resonator are [11]

$$\omega_{L,H}^2 = \frac{1 + \xi \pm \sqrt{(1 + \xi)^2 - 4\xi(1 - k^2)}}{2(1 - k^2)} \omega_c^2,$$

where $(\omega_1)^2 = (L_1C_1)^{-1}$, $(\omega_2)^2 = (L_2C_2)^{-1}$, and $\xi = (\omega_1 / \omega_2)^2$. The authors of [11] also evaluate the resonator $Q$-factor as a function of magnetic coupling ($k$) and frequency band spacing ($\xi$).

Physical realization of the transformer-based 4th-order resonator is found in [25] by different authors ([11] presents only simulations). The dual-band operation realized in [25] relies on driving the transformer-based resonator in two modes. The low-frequency band is selected as one-port oscillator connected to the primary transformer winding (similar to Fig. 1.8(b)). The high-frequency band is realized by driving the secondary winding of the transformer with opposite currents while keeping the negative-$G_m$ stage connected to the
primary winding of the transformer (double-driven transformer). The solution proposed in [25] needs only one negative-\(G_m\) stage and has only one VCO output (which is not necessarily an advantage), but it requires two transformers. Further detailed analysis of transformer-based one-port and two-port dual-band VCOs is presented in [140].

Fig. 1.9 shows a further development of dual-band transformer-based resonator where the transformer is replaced with a tapped inductor [12]. Again, the resonator itself is of 4th-order, but the silicon size is reduced down to the size of a single inductor. The mutual couplings between the coils impose restrictions for design, and the oscillator design becomes dependent on the inductor physical realization (Fig. 1.9(b)). Because of the inductor complex physical structure, it is hard to satisfy all oscillation requirements and to guarantee with a good margin the needed oscillations conditions in the one-port configuration. This is why the implementation presented in [12] utilizes a two-port oscillator configuration for both bands (Fig. 1.9(c)), which leads to worse phase noise performance, as discussed earlier. A drawback of the tapped inductor is the physical design that focuses mostly on the specified frequency bands rather than on improving the inductor \(Q\)-factor. In [58] and [95] are shown other dual-mode VCOs, which uses a transformer in the resonance tank (Fig. 1.8(a)). One-port oscillator is used for the two frequency bands in both [58] and [95]. Reference [58] also shows possible frequency range extension, or fine frequency tuning, by affecting the secondary resonance tank.

The triple-mode oscillator presented in Fig. 1.10 is a further extension of the dual-band concept based on 4th-order resonator [142]. The resonator is based on trifiliar transformer and it represents a 6th-order system having three parallel resonance frequencies. The magnetic coupling between the three separate windings connects the three individually-controlled negative-\(G_m\) stages. Similarly to [P.1], the desired frequency band is selected by powering up one negative-\(G_m\) stage while the other stages are powered down. The combination of the three coils into a transformer significantly reduces the silicon area. The implementation in [142] uses
one-port oscillator architectures, which requires specific care during the design stage to assure that the oscillation conditions are satisfied for single frequency. Common to all dual-band VCO structures, and even more pronounced here, is the problem of combining all outputs. The physical design of the transformer is tightly coupled to the design of the frequency bands, thus a $Q$-factor-oriented optimization is problematic. Therefore, the triple-mode oscillator design may lead to a degraded phase noise performance compared to a single VCO operating at the same oscillation frequency and power conditions.

A variation of the 4th-order LC tank concept is shown in [77], where the resonance tank configuration is practically the high-frequency band configuration from [P.1]. The band switching is realized with varactor, which controls which resonance has higher magnitude. This configuration allows using a single negative-$G_m$ stage, which is realized as Colpitts oscillator in [77]. The use of single stage removes the need to combine two VCO outputs, but the power consumption of the low-frequency band is relatively high. Yet another variation of the 4th-order resonator combines the 4th-order principle with the resonance-mode switching [98], which provides additional design flexibilities.

### 1.4.6. State-of-art dual-band architecture comparison

This subchapter shows a comparison between reported dual-band techniques. The comparison uses the common figure-of-merit (FoM) and the power-frequency-tuning-normalized (PFTN, [67]) given below, although a fair comparison between different topologies, technologies, and tuning ranges is always difficult to make.

$$ FOM = L \left| f_{offset} \right| - 20 \log \left( \frac{f_0}{f_{offset}} \right) + 10 \log \left( \frac{P_{dc}}{1mW} \right) $$  \hspace{1cm} (1.2)
1.4. Review of circuit techniques for building dual-band (multi-band) VCOs

\[
PFTN = 10 \log \left( \frac{kT}{P_{dc}} \left( \frac{f_{\text{max}} - f_{\text{min}}}{f_{\text{offset}}} \right)^2 \right) - \mathcal{L}\{f_{\text{offset}}\} \tag{1.3}
\]

FOM and PFTN are calculated separately for each frequency band. Table 1-I shows published topologies of dual-band and multi-band VCOs that utilize various concepts. The table summarizes the efforts on different concepts and shows the recent trend to build dual-band oscillators based on high-order resonator.

The frequency-synthesis approach is mostly used in UWB generator, as explained in 1.4.2. Reference [60] is a realization of the frequency-synthesis approach targeted for “standard” applications, but the achieved FoM performance is not impressive due to the additional power consumption consumed by the additional to the VCO blocks. The mode-switching concept has not gained large popularity among circuit designers, but it remains a good candidate despite the reported modest FoM. Instead, the switched-resonator concept has been widely used despite its shortcomings, and it is still often reported in the literature. An excellent FoM reported in [99] is achieved at low-voltage conditions and narrow tuning range. If the tuning range in [99] has to be extended for use in practical implementation, the size of the transistor switch should unavoidably be decreased, and this will be reflected by an increased phase noise and a worse FoM respectively. Another good FoM achievement using switched-resonator is reported in [115] with even lower power supply. The most recent VCO example [85] that uses extensively the switching resonator and achieves reasonable tuning range has a modest FoM numbers.

The comparison in Table 1-I between the switched-resonator and the 4th-order resonator (or the dual-mode variations) does not show particular advantage from FoM sense in favor with any particular techniques. The reason of the seeming performance equality between the two techniques may be explained with the more complex design of high-order resonator, which is not yet allowing better performance over the switched resonator. Table 1-I shows constant performance improvement over the years of development, and by using more advanced silicon process. The dual-band VCO reported in this thesis [P.1] is still competitive with the state-of-art VCOs realized on modern technologies and years after the initial development of the concept (the test chip was fabricated in 2001).
<table>
<thead>
<tr>
<th>Ref (year)</th>
<th>Tech</th>
<th>Area (mm²)</th>
<th>Bands</th>
<th>Frequency (GHz)</th>
<th>Tuning (%)</th>
<th>$V_{DD}$ (V)</th>
<th>$I_{DD}$ (mA)</th>
<th>$L @ 1$ MHz (dBc/Hz)</th>
<th>FOM</th>
<th>PFTN</th>
<th>Strategy</th>
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<td>CMOS</td>
<td>0.176</td>
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<td>-173.3</td>
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<td>5.2</td>
<td>1.8</td>
<td>8.97</td>
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<td>2</td>
<td>0.978 – 1.16</td>
<td>17.0</td>
<td>1.5</td>
<td>7.5</td>
<td>-138.0 ²</td>
<td>-177.9</td>
<td>-10.7</td>
<td>Switched resonator</td>
</tr>
<tr>
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<td>3</td>
<td>2.08 – 2.25</td>
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<td>1.5</td>
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<td>-120 ⁴</td>
<td>NA</td>
<td>Switched resonator</td>
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<td>3.5</td>
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<td>-179.6</td>
<td>-8.0</td>
<td>Dual-Mode</td>
</tr>
<tr>
<td>[58] (2010)</td>
<td>45-nm SOI</td>
<td>0.11</td>
<td>2</td>
<td>5.85 – 8.86</td>
<td>40.9</td>
<td>1.0</td>
<td>2.90</td>
<td>-110.2</td>
<td>-181.1</td>
<td>1.32</td>
<td>Dual-Mode</td>
</tr>
<tr>
<td>[25] (2007)</td>
<td>CMOS</td>
<td>NA</td>
<td>2</td>
<td>1.94 – 2.55</td>
<td>27.2</td>
<td>1.8</td>
<td>1.0</td>
<td>-116.0</td>
<td>-181.6</td>
<td>-4.7</td>
<td>Double-driv. transformer</td>
</tr>
<tr>
<td>[142] (2009)</td>
<td>CMOS</td>
<td>1.00 ³</td>
<td>3</td>
<td>1.28 – 2.27</td>
<td>55.8</td>
<td>1.5</td>
<td>3.2</td>
<td>-120.9</td>
<td>-179.0</td>
<td>0.2</td>
<td>Triple Mode</td>
</tr>
<tr>
<td>[77] (2009)</td>
<td>SiGe</td>
<td>0.35</td>
<td>2</td>
<td>4.78 – 5.19</td>
<td>8.2</td>
<td>0.8</td>
<td>3.20</td>
<td>-118.2 ³ ⁴</td>
<td>-117.2 ⁴</td>
<td>1.9</td>
<td>4th order LC tank</td>
</tr>
<tr>
<td>[P.1] (2007)</td>
<td>SiGe</td>
<td>3.61 ³</td>
<td>2</td>
<td>0.791 – 0.847</td>
<td>6.8</td>
<td>2.5</td>
<td>6</td>
<td>-134.0</td>
<td>-180.6</td>
<td>-16.6</td>
<td>4th order LC tank</td>
</tr>
</tbody>
</table>

2) @ 3-MHz offset, 3) @ 600-kHz offset; 4) normalized to 2.4-GHz carrier; 5) @ 2.5-MHz offset; 6) @ 100-kHz offset; 7) including pads and buffers.
1.5. Review of methods for analysis and simulation of LC oscillator phase noise

The theoretical analysis of oscillator phase noise has been in the attentions of researchers since the early beginning of the communications. The studies of phase noise have been focused in two directions: 1) to give insights and understanding of the physical phenomena related to the generation of phase noise; and 2) to build numerical algorithms for predicting accurately the oscillator phase noise. Fig. 1.11 depicts a simplified block diagram of different methods, where the methods targeting the first goal are named design-oriented, whereas the methods targeting the second goal are named CAD-oriented. The goal of dividing the different methods in two groups is mainly to demonstrate the different approaches from circuit designer point of view. The two groups overlap in many cases: the gained physical understanding leads to improvements of the CAD algorithms, and vice versa – results obtained by CAD algorithms increase the knowledge for phase noise, which are also used for theory verification.

The main goal of design-oriented theoretical analysis is to build a model of oscillator that predicts its phase noise, but still retaining physical quantities. The design-oriented models are typically utilizing simplified analytical expressions in order to arrive at understandable models. Due to the need of simplifications, the design-oriented methods give approximate results that are usually limited to specific oscillator topology. Nevertheless, the analytical expressions are valuable since they give concrete design guidelines for oscillator optimization. On the other hand, CAD-oriented methods target high precision in phase noise computation for arbitrary
oscillators, such that they can be implemented in circuit simulator. Due to their different targets, the analysis methods have gone in these two directions leaving a gap between the circuit designers and the CAD developers. Lately, some of the CAD methods provide more information to circuit designers and the design-oriented analysis are using heavy mathematical apparatus, thus it is hard to draw a clear border between them. Without claiming for completeness, this subchapter summarizes some of the most popular and state-of-the-art methods for oscillator analysis.

As early as 1966, Leeson proposed an equation for estimating the oscillator phase noise based on the main oscillator parameters – the power of the signal \( P_s \), the quality factor of resonator \( Q \), and the noise contribution of the active devices \( F \). The Leeson relationship has been widely used in oscillator design and it inspired various improvements. Details on the Leeson’s phase noise model and its improvement is outlined in 1.5.1, which also summarizes the recent progress on the field of \( Q \)-factor estimation. The \( Q \)-factor analysis is presented in Fig. 1.11 as a separate analysis due to its own peculiarities, but the obtained result is tightly connected to the Leeson’s model. The design-oriented methods using phasors and impulse-sensitivity functions extend the oscillator analysis by taking into account the large-signal operation of the oscillator and the active device nonlinearities. The phasor model performs the analysis in frequency domain (details in 1.5.2), whereas the ISF method does the analysis in time domain (details in 1.5.3). The initial implementations of the ISF method were numerical, thus placing the numerical ISF method closer to the CAD-oriented methods. Later, the ISF functions for certain oscillator topologies were developed analytically, which gave closed-form solutions of phase noise. By its nature, the analytical ISF method derives the noise figure and signal amplitudes of oscillators, and thus it falls in the group of the design-oriented methods. The analysis using phasors arrives at similar results – determination of \( F, P_s \), and \( Q \). The computation of phase noise using ISF does not use the Leeson equation; the arrows in Fig. 1.11 only demonstrate the link between the three phase noise methods.

The most precise method for analyzing and simulating phase noise is based on the Perturbation Projection Vectors (PPV), which was introduced by Kärtner and Demir stepping on the ground of the Floquet theory. The method is central to the CAD-oriented methods, and it employs heavy mathematical apparatus and numerical computations for the PPV. The PPV method is also utilized by advanced commercial circuit simulators, such as SpectreRF [150]. Details on the PPV method are summarized in 1.5.4.

Other analytical methods for oscillator analysis not depicted in Fig. 1.11 are focused mostly on second-order effects observed in oscillator. Recently, the phase noise of oscillator was
explained via frequency pulling caused by noise sources, which gave a sound explanation for the Lorentzian shape of the oscillator phase noise [114]. Other theoretical analysis of oscillator phenomena includes the investigation of AM-PM noise conversion in oscillators ([70], [96], [149]), synchronization of quadrature oscillators ([17], [113]), frequency pulling and locking in oscillators ([105], [107], [114], [137]) etc.

1.5.1. Leeson’s equation for LC oscillator phase noise

The oscillator phase noise $\mathcal{L}$ according to the Leeson’s model is [94]

$$\mathcal{L}(\Delta \omega) = 10\log_{10}\left(\frac{2F \cdot kT}{P_s} \cdot \left(\frac{\omega_o}{2Q \cdot \Delta \omega}\right)^2\right),$$  \hfill (1.4)

where $F$ is the noise factor of the feedback amplifier, $k$ is the Boltzmann constant, $T$ is the absolute temperature, $P_s$ is the power of the generated signal, $Q$ is the effective quality factor of the resonator, $\omega_o$ is the oscillation frequency, and $\Delta \omega$ is the frequency offset from the carrier. The Leeson model was obtained and verified experimentally without explicit analytical derivations. Later, various derivation of (1.4) were given in the literature ([63], [71]), all arriving at similar expressions. The main contribution of (1.4) is the provided summary of possible design methods for improving the oscillator phase noise: 1) to increase the signal level $P_s$; 2) to use resonator with higher quality factor; and 3) to reduce the noise contribution of the active devices. However, no guidelines were given of how to determine analytically $F$, neither the effective $Q$-factor of the resonator. In most practical applications, the noise factor $F$ is obtained experimentally through measurements, and the effective $Q$-factor is assumed identical to the unloaded $Q$-factor of the resonator. Moreover, the derivations of (1.4) uses linear model of the oscillator, which is time-invariant, and it cannot account for high-order effects such as noise up-conversion. The time-varying properties of the oscillators remain hidden, and the model fails to explain physical phenomena that can be observed in practice.

$$\mathcal{L}(\Delta \omega) = 10\log_{10}\left[2F \cdot kT \cdot P_s \left\{1 + \left(\frac{\omega_o}{2Q \cdot \Delta \omega}\right)^2\right\} \left(1 + \frac{\Delta \omega_{1/f^2}}{|\Delta \omega|}\right)\right]$$  \hfill (1.5)

$$\mathcal{L}(\Delta \omega, K_{VCO}) = 10\log_{10}\left[\frac{\omega_o}{2Q \cdot \Delta \omega} \cdot FkT \cdot \frac{2P_s}{\Delta \omega_{1/f^2}} + \frac{K_{VCO} V_m}{2\Delta \omega} \right]^2$$  \hfill (1.6)

Various improvements and modifications of the Leeson equation are found in the literature (equations (1.5) and (1.6)). For example, the phase noise model given by (1.5) includes the system noise floor and the region dominated by the flicker noise [92]. The effect of the VCO gain on the oscillator phase noise is included in (1.6) together with the flicker-noise-dominated
spectra [138]. Other analytical developments give formulas determining the unknown parameter $F$ used in (1.4) depending on the oscillator topology. Reference [135] presents a derivation of the noise generated by the cross-coupled transistors and the bias circuitry in LC oscillator. The derived noise contribution is summarized as a coefficient that replaces $F$ in (1.4). ISF-based derivations of noise contribution come to similar expressions, which could be included as coefficients in the Leeson’s formula. The noise factor obtained with the ISF approach for single-cross-coupled LC oscillator and for Colpitts oscillator can be found in [6], the corresponding factor for double-cross-coupled oscillators is found in [7], whereas [110] gives the expression of $F$ for class-C LC oscillator.

Accurate determination of effective oscillator $Q$-factor is another open question for which the Leeson’s equation does not give an answer. Razavi gives a definition of $Q$-factor for RLC resonator as a ratio between the stored energy and the dissipated energy per cycle [136]. The $Q$-factor of complex feedback can be obtained by using the slope of the phase of the transfer function with respect to the frequency [136]. The second definition of Razavi is very useful in complex resonator or feedbacks, where the feedback of the oscillator can be broken and the slope of the phase of the loop gain can be reliably determined. The Razavi’s definitions determine the $Q$-factors of the feedback topologies only, and no information for the effective $Q$-factor during the oscillator operation can be obtained. Nallatamby extends the Leeson formula for complex resonance tanks [118] by obtaining the loaded $Q$-factor in systematic way based on stored and dissipated energy. The results in [118] are particularly useful for $LC$ and transmission line resonator, but still no active transistors are included in the derivation. The specific problem of finding the loaded $Q$-factor when active transistors are involved is that in equilibrium state the stored and dissipated energies cancel each other, theoretically giving infinite quality factor. An improvement of the $Q$-factor evaluation in oscillators was proposed by Ohira in [126] and [127], where the $Q$-factor is linked to the spectral stability of oscillator (phase noise) without the need to separate the circuit into active part and passive part. As a result, the loaded $Q$-factor was derived as being proportional to the logarithmic derivative of the output impedance, and it resembles the Razavi’s definition. The results agree with the energy-dumping concept for passive resonators, and it is useful in $Q$-factor estimation as long as the output impedance and its logarithmic derivative can be analytically determined. Despite of the mentioned advances, the numerical estimation of output impedance and its derivative face problems, and the analytical derivation can be hardly applied for complex oscillator topologies. In addition, the time-varying nonlinearities that are typically associated with large-signal oscillators are not accounted in [127]. Recently, the work of Murphy using phasors shows a derivation of loaded $Q$-factor in cross-coupled oscillator (in addition to determining the noise
factor), which separates the negative resistance in two parts in order to handle the derivations [116]. The estimated loaded $Q$-factor and its degradation are evaluated for increasing amplitude of the oscillator.

1.5.2. Mechanistic physical model of phase noise, phasors

The mechanistic physical method for analyzing oscillator phase noise was introduced by Abidi and his group and it has gained large popularity among circuit designers [71], [72]. The analysis method uses circuit design parameter and derives the oscillator phase noise using simplified equations and easy-to-explain physical phenomena. By its nature, the method is a large-signal time-varying method, and it can capture effects that are invisible to the linear analysis. The methods handles noise sources in a systematic way and arrives at closed-form solutions for phase noise that can be easily interpret.

A key point of the analysis is the decomposition of different noises into AM and PM components – small rotating phasors superimposed to the main oscillator phasor. The method analyzes all essential noise sources in LC oscillators: noise due to the resonator; noise generated by the cross-coupled pair; and noise introduces by the tail current source. Because of the large-signal steady-state operation of the oscillators, all nonlinear terms can be expressed in frequency domain with their Fourier coefficients, and the corresponding frequency translations can be evaluated. By combining the contribution of all noise sources, the mechanistic physical method arrives at expression of phase noise, where the noise factor $F$ in the Leeson equation is determined by circuit design parameters. The main outcome of the proposed method can be seen as an extension of the Leeson hypothesis, but with clearly determined $F$. The analysis is applied to single cross-coupled topology, double cross-coupled topology, and to Colpitts oscillator [71], [72].

A practical achievement of the mechanistic physical model is the detailed explanation of phase noise arising from the tail current. Since the methods deals with physical quantities, this resulted in specific guidelines of how to design the current mirror in cross-coupled oscillator architecture. Furthermore, in [69] was proposed a method for minimizing the noise contribution from the tail current employing and LC filter tuned to the second harmonic. This architectural solution became almost a standard method to reduce the LC oscillator phase noise, as long as the additional inductor can be afforded on silicon.

Despite its usefulness in explaining certain physical phenomena, the mechanistic physical model suffers from given simplifications made in order to conduct the analysis. For instance, it is assumed that the MOS transistors switch sharply and produce square-wave signals so that they can be easily interpret analytically by Fourier transforms. In addition, the derivation of the
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Voltage amplitudes assume current limiting regime, where the voltage amplitude can be linked with the resonator $Q$-factor and the biasing current in a straightforward way. The analysis recognizes the effect of $Q$-factor deterioration due to large-signal operation [69], but no numerical or analytical estimate is given. In this sense, the method cannot be applied for precise estimation of phase noise, and it will remain in the design-oriented group giving circuit insights but no ultimate numerical precision.

For completeness, this paragraph lists similar works using phasors related to oscillator analysis: [143] evaluate spectrum folding in oscillators caused by the nonlinear devices; [86] carries a simplified phase noise analysis of single-ended Colpitts oscillator; [116] derives the minimum noise figure of cross-coupled oscillators (arriving at the same final results as the ISF theory) and evaluates loaded $Q$-factor of cross-coupled oscillators. As mentioned in [116], the analysis using phasor method assumes nearly sinusoidal oscillator to carry out the analysis, which limits the applicability of the method.

1.5.3. Impulse-sensitivity function (ISF) method

![Diagram](image)

Fig. 1.12. Oscillator time-domain response in case of noise injection at: (a) zero-crossing; (b) maximum/minimum of the voltage swing.

The ISF method introduced in [63], [92] is based on injected noise impulse $\delta(t)$ at different time of the oscillation period and evaluating the resulting phase departure $\Delta \phi$ of the oscillator’s waveform. Due to the time-varying characteristic of the oscillator, the phase departure $\Delta \phi$ depends on the instant for injecting a pulse: the largest departure is obtained when the noise is injected at the zero crossing, whereas no phase departure is observed when the pulse is injected at the voltage maxima/minima (Fig. 1.12). The magnitude of noise is much smaller than the magnitude of the signal, which justifies the use of linearized analysis and the principle of superposition. The transfer function defined as $\Delta \phi$ caused by the injected noise is time-dependent, but periodic function. The amount of phase departure for unity injected charge is defined as Impulse-Sensitivity Function (ISF) denoted with $\Gamma(\tau)$. The ISF may be determined numerically or analytically. Since the ISF is a periodic function, its Fourier coefficients are used for extracting information about the oscillator performance. In general one should minimize
1.5. Review of methods for analysis and simulation of LC oscillator phase noise

Γ(τ) in order to obtain low-noise oscillator. A noise source transforms to oscillator phase noise in the 1/f^2 frequency offset range with

\[ L(Δω) = 10\log_{10} \left( \frac{\bar{i}_n^2/Δf \cdot Γ_{\text{rms}}^2}{2q_{\text{max}}^2Δω^2} \right), \]  

(1.7)

where Γ_{rms} is the \textit{rms}-value of Γ(τ), and \( q_{\text{max}} = C\cdot V_{\text{max}} \) is the maximum charge accumulated at the node where the noise is injected. The cumulative results of multiple noise sources in the oscillator is obtained by summing all noise sources scaled by their corresponding Γ_{rms}. Γ_{rms} should be replaced with Γ_{eff,\text{rms}} in cases of large-signal scenarios, where some of the noises depend heavily on the oscillator waveform and inject noise only for part of the period, or in cases their noise density varies significantly during the oscillation period. The effective ISF is Γ_{eff}(τ) = Γ(τ)⋅α(τ), where α(τ) is a noise-modulation function describing the time-varying properties of the noise. An important conclusion derived by the ISF is that the \textit{dc}-level of Γ(τ) (or the Fourier \( c_0 \) coefficient of Γ(τ)) determines how the 1/f noise corner of the active device converts into 1/f^3 corner of the oscillator phase noise ([63], eq. (24)). This property is linked to the symmetry of the oscillator waveforms – more symmetrical waveform results in smaller \( c_0 \), which respectively reduces the flicker noise up-conversion.

Three possible methods for determining the ISF function are suggested in [63], but it was advised to use the numerical method as being the most precise one. Later, it was shown that the other two methods are generally incorrect [31]. The numerical method requires a Dirac impulse applied to different time instants and the phase departure measured using simulator. Thus, the original ISF theory relies heavily on circuit simulator, and the determination of ISF is time-consuming. Because of the above-mentioned reasons, the numerical ISF method could be considered as a method placed in between the CAD-oriented and the design-oriented approaches. Despite the numerical nature of the results, the conclusions derived in [63], [92] are very useful for circuit designers. The numerical ISF approach has been utilized in [8] to compare the noise performance of single cross-coupled oscillator, double cross-coupled oscillator, and Colpitts oscillator. Furthermore, as a result of the analysis of the ISF behavior, a noise-shifting Colpitts oscillator is proposed, which suggest superior phase noise performance by reducing Γ_{eff}. Similar analysis was performed in [100] for the analysis of the noise contribution due to the NMOS switching pair, the PMOS switching pair, and the resonator utilized in double cross-coupled oscillator. The applications of the numerical ISF are somewhat limiting the understanding of different noise mechanisms in oscillator.
The analytical derivation of the ISF functions in LC oscillator was mainly developed by Andreani, who derived some of the fundamental ISF properties, and provided a link between design parameters, ISF functions, and oscillator phase noise. In [5] the ISF associated with an LC resonator having medium to high Q-factor was shown to be a sinusoidal function scaled by the number \( n \) of the employed LC tanks \( \Gamma = \sin(\omega_0 t) / n \), and respectively the squared \( \text{rms} \)-value of the ISF function is equal to \( (1 / (2n^2)) \). A closed-form solution for phase noise is derived in [6] for Colpitts and cross-coupled oscillator, where certain simplifications of the transistor operation and oscillator topology are made. One key technique to achieve the analytical ISF is to link the ISF function associated with various noise sources (for instance the transistor noise) to the resonator ISF through circuit design parameters. Furthermore, the noise-modulation function \( \alpha(\tau) \) is also derived analytically as a function of the design parameters, which permits to find closed-form solution for \( \Gamma_{\text{eff, rms}} \). A closed-form solution of phase noise for the entire oscillator is obtained by combining the contribution of all noise sources. The obtained phase noise solution has a similar structure as the phase noise predicted by Leeson, with additional terms depending on design parameters that appear as a scaling factor. The ISF method was used in [148] to evaluate the noise sensitivity of the tail current in oscillators, which resulted in phase noise optimization via tail current shaping. Thus, the analytical derivation using the ISF theory in practice determines the noise factor used in the Leeson equation.

Similar to the analysis shown in [6] was performed in [7] for the analysis of CMOS cross-coupled oscillators. Again, the large-signal operation of the oscillator is analytically described with simplified equations that take into account device size, bias current, conduction angle etc. – all being design parameter used by circuit designers. The obtained closed-form phase noise equation for single cross-coupled and double cross-coupled oscillator allows topology comparison. The noise contribution of the active devices and resonator comes as a noise factor \( F \) for the Leeson equation. Reference [48] demonstrates similar analysis for bipolar Colpitts oscillator, where the MOS equations are replaced with BJT equation. An evolution of Colpitts oscillator and cross-coupled oscillator resulted in a high-performance Class-C topology, which was reported in [110]. Similarly to the methods used in [6], [7], [48], reference [110] derives the noise factor associated with the Class-C oscillator.

The powerful result obtained by the analytical ISF methods gives a possibility to analyze oscillator topologies using only circuit parameters. As with all analytical methods, the above-mentioned equations cannot provide sufficient precision as long as an exact numerical value of phase noise is desired. The oscillator simplifications and some of the assumptions made to
simplify the analysis restrict the numerical precision. For instance, in practical applications $\Gamma$ associated with the resonance tank departs from the sinusoidal form, especially when heavy nonlinearities are involved ([110], Fig.8). Furthermore, reference [7] shows that the obtained phase noise is highly sensitive to parasitic capacitance from the oscillator node to ground. Also, in the large-signal derivations of the generated amplitude it is assumed perfect switching of the active devices, thus amplitude being proportional to the biasing current ($A \approx (4/\pi) \cdot R \cdot I_B$, [7]).

It is interesting to compare the phase noise equations obtained by the analytical ISF method and the mechanistic physical model. Although they use very different analysis method, they arrive to the same conclusions for noise generated by different oscillator building blocks. The methods agree with each other for the results, and both are verified against measurement results of LC oscillator prototypes.

1.5.4. Perturbation projection vector (PPV) method

![Fig. 1.13. (a) oscillator limits cycle and its perturbation to noise; (b) decomposition of the perturbation vector in two parts: one vector along the limit cycle, and second vector perpendicular to the limit cycle.](image)

The perturbation projection vector is a method for quantifying the phase noise of oscillators in a precise numerical way. The method was largely adopted after the Demir’s work [37] following the original development of Kärtner [89]. The method is based on the Floquet theory, which treats the stability of a time-varying periodic system. Shortly, the steady-state solution of a periodic system forms a limit cycle encircled by the system on each period. A perturbation of noise at a given time instant cause the oscillator operating point to move in the neighborhood of the limit cycle, both in amplitude and phase. The nonlinear limiting mechanisms move the oscillator back to the limit cycle compensating for the amplitude shift, but it has no mean to compensate the introduced phase shift. The unregulated phase shift can be considered as introduced oscillator phase noise by the particular noise source. In mathematical sense, the autonomous oscillator can be described with a system of differential equations

$$x(t) = f(x(t)), \quad (1.8)$$
where \( x(t) \) and \( \dot{x}(t) \) are circuit state variables and their time-derivative, \( f(\cdot) \) is a nonlinear function describing the oscillator. If a small-signal perturbation \( b(t) \) is injected into the oscillator, then the equations of the perturbed circuit will be

\[
\dot{x}(t) = f(x(t)) + B \cdot b(t),
\]

where \( B \) maps the perturbation source into the system equations. The perturbed steady-state solution \( x_p(t) \) relates to the unperturbed solution \( x_s(t) \) with

\[
x_p(t) = x_s(t + \alpha(t)) + y(t).
\]

\( \alpha(t) \) in (1.10) is the time shift of the perturbed response with respect to free-running oscillator, and \( y(t) \) is amplitude deviation. In order to evaluate the time-shift of the perturbed system, the PPV method takes the derivative, or Jacobian, of the unperturbed system along \( x_s(t) \). From the Floquet theory is known that the state transition matrix \( \Phi(t, \tau) \) of the system can be expressed as

\[
\Phi(t, \tau) = U(t) \cdot \exp(D(t - \tau)) \cdot V(\tau),
\]

where \( U(t) \) is a periodic nonsingular matrix, \( V(t) = U(t)^{-1} \), and \( D = \text{diag}[\lambda_1, \ldots, \lambda_L] \) with \( \lambda_i \) being the Floquet exponents, while \( \exp(\lambda_i T_0) \) are called the characteristic multipliers. Furthermore, if the system is orbitally stable, then one of the characteristic multiplier should be equal to 1 (less than 1 implies for decaying oscillations, more than 1 implies for unbounded growth of oscillations). The PPV method finds the characteristic multiplier that is equal to one (or \( \lambda_1 = 0 \)) and thus responsible for the oscillations. It was shown that the associate with \( \lambda_1 \) eigenvector \( v_1(t) \) is all what is needed to compute the various noise contributions and its effect (projection) on the oscillator limit cycle. The projection of the noise sources along the main eigenvector gives \( \Gamma(t) = v_1(t)^T \cdot B \), where \( \Gamma(t) \) can be considered as time-varying sensitivity of the induced time-shift to given external noise perturbation. The oscillator phase noise can be approximated with [37]

\[
\mathcal{L}(\Delta \omega) \approx 10 \log_{10} \left( \frac{\frac{f_0^2 c}{\pi^2 f_0^4 c^2 + f_{\text{offset}}^2}}{} \right),
\]

where

\[
c = \sum_{i=1}^{p} \frac{1}{T} \int_0^T \left[ v_i^T(\tau) B_i(\tau) \right]^2 d\tau = \sum_{i=1}^{p} c_i,
\]

with \( p \) being the number of the noise sources in the circuit, and \( B_i \) mapping the \( i \)th noise source into the system equations. As seen from (1.12) and (1.13), it is sufficient to find the eigenvector \( v_1(t) \) from the steady-state solution, and respectively the coefficient \( c \), in order to characterize
completely the oscillator phase noise. The computation of phase noise using the PPV method is subsequently divided into two problems: 1) to find the steady-state solution of the large-signal oscillator; 2) to compute the oscillator phase noise using the equations above. The following paragraphs summarize the recent development of the two problems.

A comprehensive review on the different numerical algorithms for computing the steady-state solution is presented in [119], where the methods could be divided on time-domain techniques, such as shooting method, and on frequency domain techniques, such as harmonic balance. Reference [119] presents also iterative methods for finding the steady-state solution of the systems, makes a link between the different methods, and evaluates the precision of the methods and their computation complexity. For instance, iterative techniques based on Krylov subspace are desired in numerical simulators, as their computation complexity increase modestly with the circuit size, thus allowing the simulation of large circuits [154]. A continuous improvement of the methods used for finding the steady-state solutions are found in the literature. For instance, QR factorization is proposed instead of the LU factorization to form the inverse Jacobian matrix used in the shooting method [16]. Reference [106] introduces implicit Runge-Kutta method for finding the steady-state solution of oscillators in the context of Envelope Following technique. The method in [106] displays superior numerical accuracy over the traditional trapezoidal integration method and it is applicable to strongly nonlinear oscillators. Reference [18] presents another efficient time-domain steady-state method named FSSA, which does not require implicit computation of the Jacobian matrix, but it rather evaluates the “most important” dynamic properties of the circuit. As such, the FSSA method is able to find the steady-state solution for systems employing abrupt nonlinearities, and it is converging faster for large system. Improvements of the harmonic-balance steady-state methods are also in the focus of the researchers – for instance [111] proposes a direct computation of the HB Jacobian, which provides superior performance over the preconditioned iterative methods with moderate memory penalty.

The improvements of the PPV computations are mainly focused on the algorithm speed, or focused on providing more reliable computation methods. Even in the original Demir’s paper [37], a great deal of concerns is placed on how to compute the eigenvectors in numerically stable manner by employing integration backward in time. Furthermore, the numerically computed eigenvector \( v_1(t) \) is scaled such that \( v_1(0)^T v_1(0) = 1 \) i.e. the time-varying system properties derived from the Floquet theory are satisfied. Guidelines are also given of how to select the actual characteristic multiplier if more than one multiplier appears to be in the neighborhood of 1. Details on how to compute the Jacobian matrices used by PPV is given in [38], [39] both from the shooting PSS and the HB PSS method. Reference [40] gives further
details of how to form efficiently and precisely the eigenfunctions. Furthermore, [40] performs the computation only for the main eigenfunction, thus increasing the algorithm speed and avoiding the selection algorithm for the correct $v_1(t)$ associated with the traditional method. Reference [91] presents an improvement of the PPV computation when the oscillator involves large time-constants. The improvement is compared against the results obtained with SpectreRF, which uses the standard PPV technique. Reference [14] shows another computational improvement where the PPV is directly computed from the Jacobian employed during the PSS analysis, and it discusses the implications involved with the PPV computations in oscillator with strong nonlinearities. Reference [15] shows an efficient method for computation of all perturbation vectors for the analysis of the phase noise.

Recent developments extend the PPV towards periodic noise analysis (PAC), and even deriving large-signal sensitivity functions allowing oscillator noise optimization or CAD-oriented design with given design constraints [161], [162]. The work of Vytyaz is focused on practical LC oscillators and the application of PPV for assisting the circuit design – in [161] he derives and computes the sensitivity of the PSS solution and the sensitivity of the perturbation vector depending on the design parameters. Later in [162], the developed technique has been applied for the automatic optimization of oscillators with prescribed design constraints with the goal to minimize the oscillator phase noise. Despite of being numerical, the latest enhancements of the PPV method give useful information to circuit designers, which make the PPV technique more design-oriented. The design-oriented results using PPV were shown in [105], [107] for evaluating frequency pulling in oscillators, where even a closed form expression for the frequency shift is derived.

As a design-oriented improvement of the CAD methods could be treated as well the development of PSS and PPV in their analytical form. An analytical PSS solution could be derived using circuit simplifications, but the with preserved large-signal properties. In this area, most notable are the publications of Buonomo giving a closed-form solution for predicting the behavior of large-signal oscillators [20], [22], [23]. In addition, analytical solutions of PPV are also demonstrated in [31] and [62], for which an analytical PSS solution is required. It is obvious that an analytical solution of large-signal steady-state oscillators is possible only in few limited cases, but nevertheless the analytical PPV helps explaining the basic phenomena in oscillators, and helps to demonstrate some pathological cases [31] used for theory verification.

1.5.5. Root-Locus analysis for oscillators and its variations

The root-locus method is a classical small-signal method for analyzing the start-up process in oscillator and for deriving oscillation conditions [123]. The method can be applied to large
class of systems, which can be linearized and represented with Laplace transform. The method evaluates the trajectories of the system poles in the $s$-plane by varying design parameters and observing when the root trajectory crosses the imaginary axes of the $s$-plane. A pole situated in the RHP denotes unstable system, while pole in the LHP denotes stable system. In traditional stability analysis, all poles should be placed in the LHP, and the distance towards the imaginary axis represents a safety margin towards the unstable operation. For oscillators, at least one system pole should be placed in the RHP to start oscillations. The theoretical unbounded growth of amplitude is limited by the nonlinearity of the oscillator structure. In general, the standard root-locus method cannot be applied for large-signal systems. The start-up analysis of oscillators is particularly useful tool in the analysis of high-order oscillators where oscillations may start at multiple frequencies [11], [12], [25], [122], [P.1].

Development and extension of the method towards large-signal operation is however recently developed. One such application is the analysis of multivibrator, which is heavily nonlinear circuit [50]. The switching time in multivibrators is evaluated in [50], where the root-locus is applied only during the transition, where the MOS transistors are in active region and the small-signal representation is valid. Reference [51] evaluates the trajectories of the system roots under large-signal operation and makes the link between the sinusoidal operation and the relaxation for particular class of circuits. Further development of [51] on the root trajectories evaluation for other circuits is presented in [52] and [53]. The works presented in [49]-[53] use circuit simplifications, which reduce the order of the circuit down to two for which a closed form solution of the poles as a function of the design parameters can be obtained. Thus, the hand-held analysis performed in [50] and [51] gives valuable insights to the circuit operation, but their precision of evaluating the roots is limited. Another multivibrator analysis (for sinusoidal operation) using root-locus is shown in [21]. Also, the root-locus method has been used to analyze the stability of nonlinear systems such as Delta-Sigma Modulators [128].

The analysis of system roots in time-varying scenarios has been also in the focus of researchers. Lindberg evaluates the behavior of the “frozen” eigenvalues for class of oscillators and shows that the standard treatment of roots in large-signal systems should be refined [101], [102]. The method of the “frozen” eigenvalue means that the circuit is stopped artificially at given time instant, the circuit is linearized, and roots / eigenvalues are computed for that instant. In particular, Lindberg comes to few important conclusions: 1) all oscillatory systems are nonlinear; 2) the roots / eigenvalues are not moved back to the imaginary axis, but they travel between RHP and LHP during steady-state operation. The set of “frozen” eigenvalues within one oscillation period can be considered as time-varying eigenvalues. A unified eigenvalue theory for time-varying system was proposed by Zhu [175]. Similar discussions and treatment
of the time-varying eigenvalues were later presented in the work of Kloet [43], [120]. A more
detailed mathematical generalization of the time-varying eigenvalues, poles and zeros for linear
time-varying systems was presented in [124], which combines the work of Zhu and Kloet, gives
detailed treatment of the system stability, and proposes the QR decomposition for eigenvalue
computation. The theory in [124] is not strictly developed for autonomous systems, such as
oscillators. Recently in [62] was presented analytical derivation of the PPV for arbitrary second-
order oscillator via the time-varying eigenvalues, which establishes a link between the
eigenvalues and the oscillator phase noise. The analytical derivation of PPV assumes known
analytical steady-state solution of a second-order system so that the analytical derivations can
be applied.

The computation of system roots / eigenvalues is a research problem of its own. Given
circuit description matrices in MNA sense $Y(s) = G + s \cdot B$, the circuit roots are the zeros of the
characteristic polynomial $P(s)$ and formally the circuit roots can be found by evaluating the
zeros of the polynomial. However, this approach is not numerically stable for large circuits as
the roots tend to be sensitive on the polynomial order. Furthermore, the existence of multiple
roots can make the things even worse. Usually matrix methods can be utilized to achieve higher
precision of the roots. The matrix methods could be direct ones (computing all eigenvalues and
eigenvectors), and iterative ones (computing only selected eigenvalues). The iterative methods
are preferred and sometimes the only choice for large matrices. A comprehensive review on the
matrix methods is given in [65] and [160], [65] also presents modified matrix methods for
computing circuit roots, namely MD-QR1 and MD-QR2. A review of root computation
methods based on polynomials can be found in [130], while [59] and [131] presents a similar
review of eigenvalue-based methods ([59], [130], and [131] analyze the problem only from
mathematic point of view).

Briefly in this paragraph are given some the application of root-locus or relevant to the root
locus method. Reference [61] proposes a symbolic pole-zero extraction based on the circuit
time constants that can be obtained via the MD-QR methods. Similar symbolic pole extraction
is shown in [73]. Both methods represent a reduction of the symbolic formula based on defined
precision and reduction of the symbolic problem. Pole-zero analysis, or eigenvalue
computation, is actually involved in many symbolic analyses for general circuits, where the
computation is used to evaluate which symbolic terms of a large set can be dropped in order to
simplify expressions. Reference [47] presents an efficient dominant eigenvalue computation for
large systems described with MNA using iterative method. The article itself has also a good
review of the iterative methods for eigenvalue solving.
The concept of oscillator nonlinearity resulting in time-varying periodic roots is presented in this thesis, which is referred as Time-Varying Root-Locus (TVRL). The TVRL concept is similar to the method of the “frozen” eigenvalue, where the circuit is linearized at a given time, but no stability investigation are conducted. As it is known, in the “frozen” eigenvalue approach all poles of the system may lies in the LHP for an unstable system. The TVRL method utilizes the precise numerical results obtained with PSS analysis to build the root trajectories of the oscillator (Subchapter 5.2). The trajectories of the roots help to demonstrate the difference between oscillator architecture by linking the physical phenomena in the circuits with the obtained trajectories (Subchapter 5.4). Further detailed oscillator comparison utilizing the TVRL method is given in Chapter 6, while Chapter 7 evaluates the root trajectories in cases with small parasitic components. Additional design insights for $LC$ oscillator design are gained by the $Q$-factor analysis, which is based on the TVRL principle (Chapter 8). The TVRL method is placed between the CAD-oriented and the design-oriented method according to the map of methods for oscillator (phase noise) analysis. It uses precise CAD methods to obtain the circuit roots, but does not go in deep mathematics to derive numerically phase noise. Instead, the proposed analysis reveals specifics of the oscillator operation, gives a $Q$-factor estimation in large-signal scenario, reveals some AM-PM mechanisms, and thus it provides valuable information to circuit designers.
Chapter 2

Dual-Band VCO using Fourth-Order Resonator

2.1. Introduction

The tradeoff between phase noise and tuning range associated with the switched-resonator concept limits the performance of the switched-resonator dual-band VCO, as described in 1.4.3. The use of high-order resonator instead of the typical second order LC tank was proposed to solve the shortcomings of the switched-resonator concept. The characteristics of other circuit techniques realizing dual-band operation are summarized in Subchapter 1.4. This chapter presents in details the dual-band concept based on 4th-order resonator published in [P.1].

2.2. Fourth-Order Resonator

The proposed dual-band VCO architecture shown in Fig. 2.1(a) is based on the use of a higher-order resonator. The resonator consists of two symmetrical fourth-order LC circuits, each having two parallel and one series resonance. The oscillation frequency is one of the parallel resonance frequencies, depending where the active negative-$G_m$ stage is connected. During normal operation, only one stage is enabled with control voltage $V_{b1}$ or $V_{b2}$, respectively. The transistors of the non-active negative-$G_m$ stage operate in their cutoff region, adding only their parasitic capacitances to the total capacitance of the resonance tank.

The impedances $Z_{eq1}$ and $Z_{eq2}$ are the equivalent impedances seen by Stage-1 and Stage-2 during their normal operation. If we consider the resonance circuit with included losses, $Z_{eq1}$ has typically a higher maximum at the lower parallel resonance frequency, whereas $Z_{eq2}$ has higher maximum at the upper frequency (see Fig. 2.1(b)). Therefore, if Stage-1 in Fig. 1(a) is activated, the oscillations are initiated at the lower parallel resonance frequency. When Stage-2 is activated, the oscillations occur at the upper resonance frequency because of the larger maximum of $Z_{eq2}$ being there. If the loop gain is bigger than one for both resonance frequencies, then unwanted dual-tone oscillations may occur. The design should ensure that the loop gain at
the unwanted resonance is smaller than one. This condition should be satisfied over process and temperature variations in order to guarantee proper VCO operation.

The control voltages \( V_{B1} \) and \( V_{B2} \) are connected to nodes that are well isolated from the resonance tank, which enables one to switch between generated frequencies without affecting the \( Q \)-factor of the tank. The current sink \( I_{bias} \) provides the quiescent current for the negative-\( G_m \) stages and supplies the stage, which is working at a given time. The two negative-\( G_m \) stages can be separately optimized for minimum phase noise at their frequency of operation.

The dual-band operation of the circuit is defined by the \( LC \) resonance tank that determines the oscillation frequencies. Neglecting the losses, the general expression for the impedances \( Z_{eq1} \) and \( Z_{eq2} \) is

\[
Z_{eq1,2} = \frac{as \left( s^2 + \omega_3^2 \right)}{s^2 + \omega_1^2 \left( s^2 + \omega_2^2 \right)}, \tag{2.1}
\]

where \( \omega_1 \) and \( \omega_3 \) are the parallel resonance frequencies and \( \omega_2 \) is the series resonance frequency. The coefficient \( a \) and the series resonance frequency \( \omega_2 \) are specific for each impedance.

The denominators of \( Z_{eq1} \) and \( Z_{eq2} \) are the determinant of the admittance matrix of the tank. The numerators are co-factors of the admittance matrix, defined by the position of the port where the impedance is measured [29]. Therefore, for every circuit the denominator of the impedance is independent from the nodes between which the impedance is considered. In general this rule does not always hold and exception of the rule is possible when the determinant of the admittance matrix and some of its co-factors have equal multipliers. An example of such case is a series connection of parallel \( LC \) tanks (Foster realization of \( LC \) impedance function) when the input port is taken in parallel to one of the parallel tanks.
However, the examination of the resonance circuit in Fig. 2.1(a) shows that the impedances of $Z_{eq1}$ and $Z_{eq2}$ have the same denominators. The numerators of $Z_{eq1}$ and $Z_{eq2}$ are different, since their corresponding co-factors of the admittance matrix are defined by different ports. Thus, $Z_{eq1}$ and $Z_{eq2}$ have equal parallel resonance frequencies $\omega_1$ and $\omega_3$, and different series resonance frequency $\omega_2$.

The two impedances $Z_{eq1}$ and $Z_{eq2}$ exhibit two maxima at the parallel resonances. The location of the series resonance $\omega_2$ determines which of the two maxima is larger. When $\omega_2$ is closer to $\omega_3$, the first maximum is larger ($Z_{eq1}$ in Fig. 2.1(b)), whereas the second maximum is larger ($Z_{eq2}$ in Fig. 2.1(b)) when $\omega_2$ is closer to $\omega_1$. By choosing $\omega_2$ appropriately it is thus possible to suppress the minor peak enough in order to have stable oscillations at the other parallel resonance frequency.

The two impedances of interest are $Z_{eq1}$ and $Z_{eq2}$ of the $LC$ circuit shown in Fig. 2.2: $Z_{eq1}$ is the load for the first negative-$G_m$ stage, and $Z_{eq2}$ is the load for the second negative-$G_m$ stage. The expressions for the two impedances have the form of (2.1), where the constant $a$ is substituted with $a'$, and $\omega_2$ is substituted with $\omega_2'$ in the expression for $Z_{eq1}$. Similarly, $a''$ and $\omega_2''$ are used for $Z_{eq2}$. The expressions for the circuit elements can be derived by applying the classic Foster and Cauer synthesis procedures for $LC$ impedances and admittances [30]. Considering the general form of the impedance $Z_{eq1}$ ((2.1)), one can write that

$$ Y_{eq1} = \frac{1}{Z_{eq1}} = \frac{(s^2 + \alpha_1^2)(s^2 + \alpha_2^2)}{a's(s^2 + \omega_2'^2)} $$

From the equivalent circuit in Fig. 2.2 it follows that $Y_{eq1} = s \cdot C_1 + Y_a$, and at very high frequencies the admittance $Y_{eq1}$ is dominated by $C_1$. Thus, the value $C_1$ is

$$ C_1 = \lim_{s \to \infty} \frac{Y_{eq1}}{s} = \frac{1}{a'} . $$

The remaining part of the admittance $Y_{eq1}$, denoted here with $Y_a$, is
$Y_a = Y_{eq1} - sC_1 = \frac{s^2 \left( \omega_1^2 - \omega_2^2 + \omega_3^2 \right) + \omega_1^2 \omega_3^2}{a' s \left( s^2 + \omega_2^2 \right)}.$ \hfill (2.4)

Again, the impedance of $C_2$ is negligible at high frequencies, thus the admittance $Y_a$ is determined only by $L_1$:

$$L_1 = \lim_{s \to \infty} \frac{Z_a}{s} = \lim_{s \to \infty} \frac{1}{s Y_a} = \frac{a'}{\omega_2^2 - \omega_2^2 + \omega_3^2}.$$ \hfill (2.5)

Equations (2.3) and (2.5) give the expression of $C_1$ and $L_1$ as a function of the resonance frequencies. The expression of $Y_b$ could be obtained by using (2.2), (2.3) and (2.5), where $Y_b$ is the admittance of the $L_2C_2$ tank as shown in Fig. 2.2. In a similar manner as in the derivations above, $C_2$ dominates the admittance $Y_b$ at high frequencies and $L_2$ dominates the admittance $Y_b$ at low frequencies. The obtained expressions for $C_2$ and $L_2$ are

$$C_2 = \lim_{s \to j \omega_{pa}} \frac{s}{s^2 + \omega_2^2} Z_a = \frac{\left( \omega_1^2 - \omega_2^2 + \omega_3^2 \right)^2}{a' \left( \omega_2^2 - \omega_2^2 \right) \left( \omega_2^2 - \omega_3^2 \right)}.$$ \hfill (2.6)

$$L_2 = \frac{1}{\omega_2^2 C_2} = \frac{a' \left( \omega_2^2 - \omega_2^2 \right) \left( \omega_2^2 - \omega_3^2 \right)}{\omega_2^2 \omega_3^2 \left( \omega_2^2 - \omega_2^2 + \omega_3^2 \right)},$$ \hfill (2.7)

where $\omega_{pa}$ is the parallel resonance frequency of the impedance $Z_a$ and is given by

$$\omega_{pa}^2 = \frac{\omega_1^2 \omega_3^2}{\omega_1^2 - \omega_2^2 + \omega_3^2}.$$ \hfill (2.8)

The equations (2.3), (2.5), (2.6) and (2.7) give the values of the passive components for building the 4th-order resonator based on the desired resonance frequencies. By applying the Foster procedure for $Y_{eq2} = 1 / Z_{eq2}$ one can receive similar equations for the resonance tank components:

$$C_2 = \lim_{s \to \infty} \frac{Y_{eq2}}{s} = \frac{1}{a'^*}.$$ \hfill (2.9)

$$L_2 = \lim_{s \to \infty} \frac{1}{s Y_{eq2}} = \frac{a'' \omega_2^2 \omega_3^2}{\omega_2^2 \omega_3^2}.$$ \hfill (2.10)

$$L_1 = \lim_{s \to j \omega_{eq2}} \frac{s}{s^2 + \omega_2^2} Y_{eq2} = \frac{a'' \omega_2^2 \omega_3^2}{\omega_2^2 \omega_3^2} \left( \omega_2^2 - \omega_2^2 \right) \left( \omega_2^2 - \omega_2^2 \right)$$ \hfill (2.11)

$$C_1 = \frac{1}{\omega_2^2 L_1} = \frac{\left( \omega_1^2 - \omega_2^2 \right) \left( \omega_2^2 - \omega_2^2 \right)}{a'' \omega_2^4}.$$ \hfill (2.12)
Table 2-I: Dual-band tank synthesized component values

<table>
<thead>
<tr>
<th></th>
<th>Low-frequency band</th>
<th>High-frequency band</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$</td>
<td>$\frac{1}{a^1}$</td>
<td>$(\omega_3^2 - \omega_2^2)(\omega_2^2 - \omega_1^2)$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$a^\omega \omega_4^4$</td>
</tr>
<tr>
<td>$L_1$</td>
<td>$\frac{a^1}{\omega_1^2 - \omega_2^2 + \omega_3^2}$</td>
<td>$(\omega_3^2 - \omega_2^2)(\omega_2^2 - \omega_1^2)$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$a^\omega \omega_5^2$</td>
</tr>
<tr>
<td>$C_2$</td>
<td>$\frac{(\omega_3^2 - \omega_2^2)^2}{a^1(\omega_3^2 - \omega_2^2)(\omega_2^2 - \omega_1^2)}$</td>
<td>$\frac{1}{a^\omega}$</td>
</tr>
<tr>
<td>$L_2$</td>
<td>$\frac{a^1(\omega_3^2 - \omega_2^2)(\omega_2^2 - \omega_1^2)}{\omega_1^2 \omega_3^2 (\omega_1^2 - \omega_2^2 + \omega_3^2)}$</td>
<td>$a^\omega \omega_6^2$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\frac{a^\omega \omega_6^2}{\omega_1^2 \omega_3^2}$</td>
</tr>
</tbody>
</table>

Table 2-I summarizes the derived expression for the passive components building the 4th-order resonator. The component values can be calculated using one or both sets of equations as a function of the angular frequencies. By representing the product $L_1C_1$ through both sets of equations, the following relationship can be derived:

$$\omega_1^2 + \omega_3^2 = \omega_2'^2 + \omega_2''^2$$  \hspace{1cm} (2.13)

The angular frequencies $\omega_1$ and $\omega_3$ are the desired oscillation frequencies, and they are fixed by the target application. Equation (2.13) shows that increasing $\omega_2'$ will automatically decrease $\omega_2''$, and vice versa. Thus, a placement of $\omega_2'$ close to $\omega_3$ would result in $\omega_2''$ being close to $\omega_1$. The first condition ($\omega_2'$ close to $\omega_3$) enlarges the difference in magnitude between two maxima of $Z_{eq1}$ with $Z_{eq1}(\omega_1)$ being the larger. The second condition ($\omega_2''$ close to $\omega_1$) enlarges the difference between the maxima of $Z_{eq2}$ with $Z_{eq2}(\omega_3)$ being the larger. Therefore, the suppression of the unwanted resonance for both frequency bands can be done simultaneously. After the choice of resonance frequencies is made, it is enough to use only one set of equations (for $Z_{eq1}$ or for $Z_{eq2}$) from Table 2-I.

The series resonance, however, cannot be placed very close to any of the parallel resonances because the component values become unpractical. For instance, if $f_1=800\text{MHz}$; $f_3=1.8\text{GHz}$; and $f_2'=1.64\text{GHz}$, then the inductor ratio is $L_1/L_2 = 1.84$. If $f_2'$ is $1.75\text{GHz}$, then the new ratio becomes $L_1/L_2 = 4.81$ which is not very convenient for on-chip implementation. The component ratios depend also on the ratio between $\omega_1$ and $\omega_3$. If the maximum inductor ratio is assumed to be 4, and 8 for the maximum ratio of the capacitors, then the ratio $\omega_3/\omega_1$ can range from 1.7 up to 3.5 ~ 4. This is a rough estimation of the ability to spread the two bands throughout the frequency scale. Other limitations stemming from the silicon process, parasitic
capacitances, tuning requirements etc may affect this range.

The frequency tuning of the VCO can be done in the traditional manner by replacing the capacitors $C_1$ and $C_2$ with varactors. The frequency tuning range is maximized if both varactors are controlled simultaneously and proportionally.

### 2.3. Root-Locus Diagram for checking the oscillation conditions

The assumption that the circuit oscillates at the maximum of the corresponding tank impedance is intuitive and needs stringent proof. The ability of the circuit to oscillate at two distinct frequencies can be investigated by using the root-locus diagram of the circuit’s characteristic polynomial. For this purpose, the simplified model of the oscillator shown in Fig. 2.3 is used, which consists of one-half of the resonance circuit ($Z_{eq1}$ and $Z_{eq2}$) and a negative conductance $-G_{m1}$ on the side of $Z_{eq1}$ when Stage-1 is enabled, and $-G_{m2}$ on the side of $Z_{eq2}$ when Stage-2 is enabled. The conductances $-G_{m1}$ and $-G_{m2}$ are the doubled negative conductances created by Stage-1 and Stage-2. The inductor losses are represented by equivalent series resistors $r_L = \omega L/Q_L$, where $Q_L$ is the $Q$-factor of the inductor $L$ at frequency $\omega_Q$. Thus the impedance of the inductors are $Z_1 = sL_1 + r_{L1}$ and $Z_2 = sL_2 + r_{L2}$. The losses in the capacitors are neglected here for simplicity.

The characteristic polynomial of the circuit is the determinant of the nodal admittance matrix $Y$ for each case. The nodal admittance matrix $Y_1$ for the lower frequency band is derived from Fig. 2.3(a); the nodal admittance matrix $Y_2$ for the higher frequency band is derived from Fig. 2.3(b), and they are

$$Y_1 = \begin{bmatrix} sC_1 + \frac{1}{Z_1} - \frac{1}{Z_1} \\ -\frac{1}{Z_1} \\ -\frac{1}{Z_1} \\ \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_2} \end{bmatrix}, \quad (2.14)$$

$$Y_2 = \begin{bmatrix} sC_1 + \frac{1}{Z_1} \\ -\frac{1}{Z_1} \\ -\frac{1}{Z_1} \\ \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_2} - \frac{1}{Z_2} \end{bmatrix}, \quad (2.15)$$
where the first column corresponds to node #1 and the second column corresponds to node #2. The characteristic polynomial $P_1(s)$ is obtained by computing the determinant of $Y_1$ as:

\[
P_1(s) = \det(Y_1) = \left( sC_1 + \frac{1}{Z_1} - G_{m_1} \right) \left( sC_2 + \frac{1}{Z_1} + \frac{1}{Z_2} \right) - \frac{1}{Z_1^2} = \frac{Z_1 (sC_1 - G_{m_1}) (sC_2 Z_1 Z_2 + Z_1 + Z_2) + sC_2 Z_1 Z_2 + Z_1 + Z_2 - Z_2}{Z_1 Z_2}.
\]

(2.16)

Since the roots are the zeros of the $P_1(s)$ numerator, the denominator can be excluded from the evaluation, as it does not affect the value of the computed roots. Finally, the characteristic polynomial when Stage-1 is activated is

\[
P_1(s) = (sC_1 - G_{m_1}) (sC_2 Z_1 Z_2 + Z_1 + Z_2) + sC_2 Z_2 + 1.
\]

(2.17)

The characteristic polynomial $P_2(s)$ when Stage-2 is activated is obtained in the same way using the determinant of matrix $Y_2$, and it is

\[
P_2(s) = (sC_2 - G_{m_2}) (sC_1 Z_1 Z_2 + Z_1 + Z_2) + sC_1 (Z_1 + Z_2) + 1.
\]

(2.18)

$P_1(s)$ and $P_2(s)$ are of fourth order and have two complex-conjugated root pairs. Fig. 2.4 shows the root loci of $P_1(s)$ and $P_2(s)$ for the LC circuit from the example above assuming inductor $Q$-factors of 10 at frequency of 800MHz ($f_1=800MHz$, $f_3=1.8GHz$, $f_2=1.64GHz$). The roots for both frequency bands are computed numerically while sweeping $G_{m_1}$ and $G_{m_2}$, and the arrows in Fig. 2.4 indicate increasing $G_{m_1}$ or $G_{m_2}$. When the negative conductance is added at the side of $Z_{eq1}$, the root with a smaller imaginary part is major and determines the lower frequency of oscillation. Fig. 2.4 shows that the major root has a positive real part for $G_{m_1}$ more than 2.55mS. The secondary root keeps its real part negative up to $G_{m_1} = 10.3mS$. Thus when Stage-1 is enabled there is a wide range of values of $G_{m_1}$ (from 2.55mS till 10.3mS), for which

---

Fig. 2.4. Root loci of $P_1(s)$ and $P_2(s)$ when the added negative conductances $-G_{m_1}$ and $-G_{m_2}$ vary (only the roots with positive imaginary parts are shown).
the characteristic polynomial has only one root with a positive real part and the circuit oscillates at the lower parallel resonance of the tank. If $G_{m1}$ exceeds 10.3mS, then both roots have positive real parts and oscillations are theoretically possible at $f_1$ and $f_3$.

Similar root-locus results are obtained when Stage-2 is enabled. Now the major root is the one with higher imaginary part. Fig. 2.4 shows that the circuit oscillates at the upper parallel resonance frequency when $G_{m2}$ is between 3.21mS and 11.79mS. This example confirms that in proper design the circuit will firmly oscillate at $f_1$ when Stage-1 is active and at $f_3$ when Stage-2 is active.

The polynomials (2.17) and (2.18) have a compact form in which the inductors and their losses are represented by the impedances $Z_1$ and $Z_2$. Including realistic inductor model and the capacitor losses will result in more complicated expressions for $Z_1$ and $Z_2$ as well as for the characteristic polynomials. Further complication of the initial design has little added value, since the next step should always be numerical optimization with the given process parameters.

2.4. Quality-factor in the fourth-order resonator

Combining the two inductors into a more complicated resonator raises the question of the impact on the resonator quality factor. Since the quality factor of the on-chip inductor is usually a limiting factor for the oscillator phase-noise performance, the resulting quality factor of the resonator should not be worse than the $Q$-factor of the inductors themselves. Possible $Q$-factor deterioration cannot be afforded, because it will result in phase noise penalty.

The quality factor of a higher order resonance tank is generally difficult to obtain in closed analytical form, especially if a sophisticated model for the inductor is used. The commonly used formula for determining the quality factor of an arbitrary resonance tank is [136]

$$Q = \frac{\omega_0}{2} \left| \frac{d\Phi}{d\omega} \right|_{\omega=\omega_0},$$

(2.19)

where $\omega_0$ is the resonance frequency and $d\Phi / d\omega$ is the slope of the phase of the impedances $Z_{eq1}$ and $Z_{eq2}$. The $Q$-factor of the 4th-order resonator is drawn in Fig. 2.5 as a function of the inductors’ $Q$-factor. The plot is obtained with numerical simulation, where $Q_1$ denotes the quality factor of the inductor $L_1$, and $Q_2$ is the quality factor of $L_2$. The inductor losses are modeled with a series resistance leading to the desired $Q$-value at the frequency of oscillation, as it was done in Section 2.3. A similar plot has been obtained for the quality factor at the upper frequency band. Fig. 2.5 shows that the resulting quality factor of the 4th-order resonance tank is identical to the $Q$-factor of the inductors, given that the two inductors have the same $Q$-factor.
2.5. Graphically-based selection of the resonance frequencies

In other words, the $Q$-factor of the 4th-order resonator is the same as that of a 2nd-order $LC$ resonance tank, if identical components are used.

2.5. Graphically-based selection of the resonance frequencies

The design of the 4th-order resonator is the core of the proposed dual-band VCO, and it is accomplished by selecting the desired angular frequencies ($\omega_1$ and $\omega_3$) and using the equations in Table 2-I to compute the values of the resonance components. According to (2.13), the selection of the series-resonance frequency for one of the band ($\omega'_2$) automatically determines the series-resonance frequency for the other band ($\omega''_2$). One degree of freedom for choosing the series resonance frequency ($\omega_2$) is left for the designer. The selection can target bigger suppression of the unwanted peak compared to the desired peak, or another target can be achieving resonance components’ values that are as close as possible to each other (for easier implementation on silicon). Bigger suppression can be achieved by selecting the series resonance to be close to the unwanted parallel resonance, but this selection usually leads to big values for the inductors and the capacitors, which are not feasible for realization, i.e. a tradeoff between suppression and components values should be found. To evaluate this tradeoff, the inductor ratio $L_1/L_2$ and the capacitor ratio $C_1/C_2$ is expressed by using the equations in Table 2-I as:

$$\frac{L_1}{L_2} = \frac{k_p^2}{(k_p^2-k_i^2)(k_i'^2-1)}, \quad (2.20)$$
Fig. 2.6. Passive component ratio as a function of the resonance frequencies: (a) \( C_1/C_2 \) ratio; (b) \( L_1/L_2 \) ratio.

\[
\frac{C_1}{C_2} = \frac{\left( k_p^{2} - k_s'^{2} \right) \cdot \left( k_s'^{2} - 1 \right)}{\left( 1 - k_s'^{2} + k_p^{2} \right)^{2}}, \quad (2.21)
\]

where \( k_p = \frac{\omega_3}{\omega_1} \); \( k_s' = \frac{\omega_2'}{\omega_1} \); and \( k_s'' = \frac{\omega_2''}{\omega_1} \). Equations (2.20) and (2.21) are shown as a family of contour plots in Fig. 2.6(a) and Fig. 2.6(b). The upper part of the two figures is not used because \( k_p > k_s' \). From Fig. 2.6(a) and Fig. 2.6(b) it is seen that when the series resonance is getting closer to the parallel resonance, the ratio \( L_1/L_2 \) gets bigger, while \( C_1/C_2 \) gets smaller.

The figure should be read as follow: assuming that the desired frequency ratios are \( k_p = 3.5 \) and \( k_s' = 3.0 \), then resulting component ratio will be \( L_1/L_2 \approx 0.5 \) and \( C_1/C_2 \approx 1.5 \). Realization of capacitors having big or small ratios may not be a big issue when they are integrated on silicon. However, realization of inductors with big ratios is facing practical difficulties.

The selection of resonance frequencies \( \{ \omega_1, \omega_2(\omega_{\text{stop}}), \omega_3 \} \) should be carefully selected not only from realization point of view, but also the magnitude of the impedance \( Z_{\text{eq}1} \) should be bigger than the magnitude of \( Z_{\text{eq}2} \) when the lower frequency band is selected \( (Z_{\text{eq}1}(\omega_1) > Z_{\text{eq}1}(\omega_3)) \), and vice versa \( (Z_{\text{eq}2}(\omega_1) < Z_{\text{eq}2}(\omega_3)) \). Fig. 2.7 shows a log-log approximation of \( Z_{\text{eq}1} \) and \( Z_{\text{eq}2} \) (including losses) having equal magnitudes at \( \omega_1 \) and \( \omega_3 \) [32]. Equal magnitudes are achieved when \( \omega_{\text{stop}} \) and \( \omega_{\text{peak}} \) are the geometric mean of \( \omega_1 \) and \( \omega_3 \)

\[
\omega_{\text{stop}} \left( = \omega_2 \right) = \sqrt{\omega_1 \cdot \omega_3}, \quad (2.22)
\]

where \( \omega_{\text{stop}} \) is the series resonance \( \omega_2 \), \( \omega_{\text{peak}} \) is the intersect angular frequency of the low-frequency and the high-frequency approximation line for \( Z_{\text{eq}1} \) (\( Z_{\text{eq}2} \)). Equation (2.22) can be verified by using the synthesized \( LC \) components from Table 2-I, and expressing \( \omega_{\text{stop}} \) and \( \omega_{\text{peak}} \) for \( Z_{\text{eq}1} \) and \( Z_{\text{eq}2} \). In particular, \( \omega_{\text{stop}}^{-2} = (L_1||L_2)C_2 \) and \( \omega_{\text{peak}}^{-2} = (L_1+L_2)C_1 \) for \( Z_{\text{eq}1} \), whereas
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Fig. 2.8 shows the complete electrical schematic of the VCO core with its component values. The resonance tank is built with four inductors, fixed capacitors and varactors. A compromise between phase noise and tuning range defines the ratio of the values of the metal-insulator-metal (MIM) capacitors and the varactors. The PN-junction varactors are decoupled from the voltage supply to improve the pushing figure of the oscillator. The choice of decoupling resistor values is based on a tradeoff between generated thermal noise and resonator losses. The cathode voltage $V_{\text{var}}$ and the control voltages $V_{b1}$ and $V_{b2}$ were supplied externally. Fig. 2.9 shows the measured tuning ranges for the lower and for the higher frequency band, 6.8% and 6.7%, respectively.

The frequency band is selected by supplying the proper bias for the two amplifier stages as

$$\omega_{\text{stop}}^2 = L_1 C_1 \quad \text{and} \quad \omega_{\text{peak}}^2 = L_2 C_2 \quad \text{for} \quad Z_{eq}. \quad \text{Dual-band operation is achieved when}
$$

$$\omega'_2 > \sqrt{\omega_1 \cdot \omega_3} \quad \text{(2.23)}$$

$$\omega''_2 < \sqrt{\omega_1 \cdot \omega_3} \quad \text{(2.24)}$$

However, the relation between $\omega'_2$, $\omega''_2$, $\omega_1$, and $\omega_3$ given in (2.13) sets one additional limitation for the series frequency selection. Using (2.13), (2.23) and (2.24), it can be shown that

$$\omega''_2 > \omega'_2 + \omega_1^2 - \omega_1 \cdot \omega_3. \quad \text{(2.25)}$$

Equation (2.25) is a stronger requirement than (2.23) for assuring dual-band operation. If (2.25) is satisfied, then (2.24) is automatically fulfilled. Condition (2.25) can be used for initial selection of the resonance frequencies, but precise numerical simulations should be made including all parasitic components and on-chip inductor non-idealities.

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Fig. 2.7. Simplified frequency behavior of the impedances $Z_{eq1}$ and $Z_{eq2}$

$$\omega_{\text{stop}}^2 = L_1 C_1 \quad \text{and} \quad \omega_{\text{peak}}^2 = L_2 C_2 \quad \text{for} \quad Z_{eq2}.$$

Dual-band operation is achieved when

$$\omega'_2 > \sqrt{\omega_1 \cdot \omega_3} \quad \text{(2.23)}$$

$$\omega''_2 < \sqrt{\omega_1 \cdot \omega_3} \quad \text{(2.24)}$$

However, the relation between $\omega'_2$, $\omega''_2$, $\omega_1$, and $\omega_3$ given in (2.13) sets one additional limitation for the series frequency selection. Using (2.13), (2.23) and (2.24), it can be shown that

$$\omega''_2 > \omega'_2 + \omega_1^2 - \omega_1 \cdot \omega_3. \quad \text{(2.25)}$$

Equation (2.25) is a stronger requirement than (2.23) for assuring dual-band operation. If (2.25) is satisfied, then (2.24) is automatically fulfilled. Condition (2.25) can be used for initial selection of the resonance frequencies, but precise numerical simulations should be made including all parasitic components and on-chip inductor non-idealities.
Fig. 2.8. Electrical schematic of the dual-band VCO core

follows: When $V_{B1(2)}$ equals 1.5V, the negative-$G_m$ cell has optimal conditions for operation, and alternatively, when $V_{B1(2)}$ is 0.4V the cell is effectively in cutoff region. Only one amplifier stage is made operational at a time. The simulated transition time between the two bands is less than 50 ns. The architecture allows implementing a power-down function by tying both bias voltages down to 0.4V and powering down the bias circuitry.

The two negative-$G_m$ stages share 2.5-nH inductors for emitter degeneration. The quiescent current of the amplifier stage is set with a current mirror that has the possibility for external
2.6. Test chip validation

Fig. 2.10. Electrical circuit of the all-NPN buffer used for measurement current control. The VCO core consumes approximately 6 mA from a 2.5-V power supply.

Fig. 2.10 shows an all-NPN single-ended on-chip buffer implemented for measurement purposes. The all-NPN buffer topology was selected instead of MOS buffer topology, because the available in the process MOS transistors are slower than NPN transistors, and the evaluated MOS buffers had much higher current consumption for similar output power levels. The buffer isolates the resonance tank from the load and delivers an output power level convenient for good phase noise measurements. The buffer takes the differential VCO signal from the nodes between the two coils for the two frequency bands, as shown in Fig. 2.8. If desired, two separate outputs for each band could be taken from the collectors of the corresponding cross-coupled transistors ($Q_{11}$-$Q_{12}$ for the lower frequency band, and $Q_{21}$-$Q_{22}$ for the upper frequency band). The good isolation is provided by the two-stage structure of the buffer. The first stage is comprised of two cross-connected differentially-driven buffers that ensure symmetrical loading of the resonance tank. The second stage transforms the differential signal from the first stage in single-ended output, and works in class-C fashion for good power efficiency.

Fig. 2.11 shows the measured harmonic spectrum for the two frequency bands at the middle of their tuning range ($V_C=1.4V$). Since the output buffer is used for both frequency bands, it has no frequency-selective $LC$ networks and introduces distortions. The harmonic content of the output comes mainly from the buffer nonlinearity, but these distortions do not affect the VCO phase noise performance. In both frequency bands, the second harmonic is the largest, but it stays 15dB lower than the fundamental tone, which is sufficient for proper phase noise measurement.

Fig. 2.12 shows the measured output power variations across the tuning ranges. The output power for the high-frequency band is lower (between -1dBm and 0dBm) than the output power of the low-frequency band, and the reasons are two: 1) the buffer gain at higher frequencies is lower; and 2) the signal amplitude is lower at the high-frequency band. The output power at the
high-frequency band remains nearly constant across the tuning range. On the other hand, the low-frequency band display a drop in output power level when the control voltage $V_C$ is above 1.9V. The reason for this drop is not in the output buffer, but in the VCO core. Since the varactor bias $V_{VAR}$ is fixed at 2.4V, the PN-junction varactor is forward biased for part of the period when the VCO generates large voltage swing. The mild operation in forward bias causes losses, swing reduction, and therefore the output power decreases.

The design goal for the test chip was to prove the proposed concept. Second, but not less important, was to achieve as good phase noise performance as possible in the two frequency bands. Another important issue was for the generated frequency to be within the range of the GSM/PCS/DCS specification in order to face the challenge of fulfilling the phase noise specification. With that in mind, the tuning range was kept close to the specified range, as it is known that a broader tuning range worsens the noise performance [138]. The rest of the needed capacitor value was implemented with MIM capacitors instead of a varactor, because the MIM capacitors had a better quality factor on the given silicon process. The fixed MIM capacitors can also be utilized for digital coarse-tuning of the VCO frequency to compensate temperature.
2.6. Test chip validation

A signal source analyzer (HP4352S) was used for the phase noise measurement. The measured phase noise is shown in Fig. 2.13 for the two frequency bands and it reaches -142dBc/Hz at an offset of 3 MHz. The presented above phase noise result is measured at the middle of the tuning range ($V_C=1.4V$) where the VCO gain is significant and causes noise AM-PM conversion. The best VCO phase noise has been measured at $V_C=0V$, where this effect is minimized.

The test chip was fabricated in IBM-5AM SiGe technology, which has a 4-μm thick aluminum layer for high quality inductors. The quality factor of the inductors was approximately 10 and 12.5 for the 800-MHz and 1.8-GHz bands, respectively. The chip was measured using on-wafer probing. A photograph of the VCO chip is shown in Fig. 2.14, where the active VCO area is 1.4mm × 1mm, excluding the degeneration inductors and the buffer.
A comparison between the reported here VCO with other state-of-art dual-band VCOs is presented in Table 1-1 (Subchapter 1.4.6). The relative comparison between different dual-band concepts shows the competitiveness of the proposed solution. The proposed solution eliminates the $Q$-factor deteriorating switches in regular dual-band VCOs, which leads to an improved VCO phase noise, and it offers flexibility for dual-band frequency planning. On the other hand, the design of 4th-order VCO becomes more complex; it requires careful theoretical investigation as presented in Chapter 2 and Chapter 3; and it potentially occupies larger silicon area than a single-band VCO. A method to reduce the silicon area occupied by the 4th-order VCO is presented in Chapter 3.

2.7. Summary and contributions

The material presented in this chapter was published in the IEEE Transactions of Circuits and Systems – II [P.1] (except for some derivation and measurement details, as well as for the graphically-based design presented in 2.5). The material from [P.1] is reused with the kind permission of IEEE, © 2007 IEEE. The 4th-order resonator is recognized by the IEEE community as important circuit technique for realizing a dual-band oscillator, and it was referred by other journal publications and conference proceedings (9 citations according to Scopus by March 2012). This work was financially supported by IBM Microelectronics.

The contributions of the work presented in this chapter are:

1. Proposed is a dual-band VCO architecture that avoids the use of $Q$-factor deteriorating switches by utilizing a 4th-order resonator.

2. The specifics of the 4th-order resonator are thoroughly analyzed: given are design equations for the passive components in the $LC$ tank; various design issues are discussed; $Q$-factor evaluation of the proposed resonator is compared against a 2nd-order $LC$ tank.
Chapter 3

Dual-Band VCO using Tapped Inductor

3.1. Motivation and target specification for a design example

Fig. 3.1. Dual-band VCO based on 4th-order resonator and tapped inductor: (a) block diagram; (b) frequency plan.

The use of 4th-order resonance tank eliminates the need of MOS switches present in the dual-band switched-resonator concept, but the proposed in Chapter 2 approach requires four inductors that occupies large silicon area. The four separate inductors are connected in series and one possible solution to reduce the silicon area is to combine the four inductors into a single tapped inductor (Fig. 3.1(a)). The tapped inductor could have geometry similar to the one presented in [33] and [155]. The introduced magnetic coupling in such an inductor makes the design flow of the resonator more complicated as the two frequency bands interfere with each other. In addition, the physical dimensions of the inductor have a big influence on the angular frequency selection and on the oscillator design itself.

This chapter analyzes the theory of the 4th-order resonator using a tapped inductor and it gives design equation for the dual-band VCO design. The guidelines derived from the theory are demonstrated using a design example, which targets the GSM and WCDMA standards according to the frequency plan presented in Fig. 3.1(b). The WCDMA frequency range is covered by the low-frequency band of the VCO (2.0–2.6 GHz), while the GSM standards are covered by the high-frequency band (6.0–8.0 GHz) followed by frequency dividers. The selection of this frequency plan is harmonized with the requirements of each standard and with the specifics of the dual-band VCO based on 4th-order resonator. The dual-band VCO typically...
consumes larger current from the power supply when it operates at the high-frequency band, since the impedance $|Z_{eq1}(\omega)|$ is usually bigger than the impedance $|Z_{eq2}(\omega)|$ in real resonators (higher negative-$G_m$ is required to start oscillations at the high-frequency band compared to the low-frequency band as shown in Fig. 2.4, Fig. 3.11, and Fig. 3.12). A VCO covering the GSM standard is allowed to consume large current because of the stringent phase noise specifications. In addition, the phase noise of the high-frequency VCO band can be improved using frequency dividers. On the other hand, the phase noise requirements in the WCDMA standard are relaxed, but the power consumption is an issue since the transceiver can operate for many time slots. Thus, in the frequency planning presented in Fig. 3.1(b) the GSM standard is covered by the high-frequency VCO band followed by frequency dividers, while the WCDMA frequency range is generated in a power-efficient manner directly by the low-frequency VCO band.

3.2. Fourth-order resonator using single inductor

3.2.1. Transformation of tapped resonator to simplified fourth-order tank with one magnetic coupling

Fig. 3.2. Transformation of the 4th-order resonator using a single inductor to the basic structure

Fig. 3.2(a) shows the 4th-order resonator in which the four inductors are magnetically coupled. The impedances $Z_{eq1}$ and $Z_{eq2}$ seen from the two negative-$G_m$ stages now depend also on the magnetic couplings between the coils. As shown in Fig. 3.2(b), the initial circuit can be transformed to a new equivalent circuit having only two inductors, one magnetic coupling between the inductors, and two capacitors. It can be shown that the inductive components of the new equivalent circuit shown in Fig. 3.2(c) can be expressed as

\[ L_a = L_1 + L_4 + 2 \cdot k_{14} \sqrt{L_1 L_4} = 2 \cdot L_4 (1 + k_{14}) , \]  

\[ L_b = L_2 + L_3 + 2 \cdot k_{23} \sqrt{L_2 L_3} = 2 \cdot L_3 (1 + k_{23}) . \]
3.2. Fourth-order resonator using single inductor

\[ k_{ab} = \frac{k_{12} + k_{13}}{\sqrt{(1+k_{14}) \cdot (1+k_{23})}} , \]  

(3.3)

where it is assumed that \( L_1 = L_4 \) and \( L_2 = L_3 \) in order to obtain a differential resonator. The capacitors connected to the resonance tank remain unchanged (\( C_a = C_1/2 \) and \( C_b = C_2/2 \)). The equivalent impedances \( Z_{eq1} \) and \( Z_{eq2} \) have the general form

\[ Z_{eq1} = h_1 \frac{s \left( s^2 + \omega_{2a}^2 \right)}{\left( s^2 + \omega_a^2 \right) \left( s^2 + \omega_b^2 \right)} ; \quad Z_{eq2} = h_2 \frac{s \left( s^2 + \omega_{2b}^2 \right)}{\left( s^2 + \omega_a^2 \right) \left( s^2 + \omega_b^2 \right)} , \]  

(3.4)

which can be expressed in terms of resonance tank components as

\[ Z_{eq1} = \frac{s^3 \cdot C_b L_a L_b \left( 1-k_{ab}^2 \right) + s \cdot \left( L_a + L_b + 2k_{ab} \sqrt{L_a L_b} \right)}{s^4 \cdot C_a C_b L_a L_b \left( 1-k_{ab}^2 \right) + s^2 \cdot \left( C_a \left( L_a + L_b + 2k_{ab} \sqrt{L_a L_b} \right) + C_b L_b \right) + 1} , \]  

(3.5)

\[ Z_{eq2} = \frac{s^3 \cdot C_a L_a L_b \left( 1-k_{ab}^2 \right) + s \cdot L_b}{s^4 \cdot C_a C_b L_a L_b \left( 1-k_{ab}^2 \right) + s^2 \cdot \left( C_a \left( L_a + L_b + 2k_{ab} \sqrt{L_a L_b} \right) + C_b L_b \right) + 1} . \]  

(3.6)

The derivation of (3.5) and (3.6) assumes ideal components in order to obtain tractable expressions. The expression for the impedances has the same characteristics as the ones without magnetic coupling – the impedances have two parallel resonances and one series resonance. The parallel resonance frequencies are the same for both impedances, whereas the series resonances are different. Using (3.5) and (3.6), the series resonances \( \omega_{2a}^s, \omega_{2b}^s \), and the sum of the two parallel resonances are:

\[ \omega_{2a}^s = \frac{L_a + L_b + 2k_{ab} \sqrt{L_a L_b}}{C_b L_a L_b \left( 1-k_{ab}^2 \right)} , \]  

(3.7)

\[ \omega_{2b}^s = \frac{1}{C_a L_a \left( 1-k_{ab}^2 \right)} , \]  

(3.8)

\[ \omega_1^s + \omega_2^s = \frac{C_a \left( L_a + L_b + 2k_{ab} \sqrt{L_a L_b} \right) + C_b L_b}{C_a C_b L_a L_b \left( 1-k_{ab}^2 \right)} , \]  

(3.9)

where \( h_1 = 1/C_a \) and \( h_2 = 1/C_b \) in equation (3.4). It follows from equations (3.7)-(3.9) that the relation between the resonance frequencies (2.13) (\( \omega_1^2 + \omega_2^s = \omega_{2a}^s + \omega_{2b}^s \)) also holds for the 4th-order resonator even in the presence of the magnetic coupling \( k_{ab} \). This is an important property of the investigated circuit, which allows us the reuse the criteria (2.25) (\( \omega_2^s > \omega_1^2 + \omega_2^s > -\omega_1 \cdot \omega_3 \)) for assuring dual-band operation.
3.2.2. Minimum spacing between the $\omega_1$ and $\omega_3$

This subchapter evaluates how close the two frequencies $\omega_1$ and $\omega_3$ can be placed. The feasibility of the component realization in the resonance tank depends in a complex way on the selection of the $\omega_1$ and $\omega_3$. However, the angular frequencies $\omega_1$ and $\omega_3$ are typically set by the desired applications. This analysis helps the initial frequency plan of the VCO and it makes sure that the selected $\omega_1$ and $\omega_3$ are feasible for implementation. An auxiliary parameter $\alpha$, which is a function of $\omega_3/\omega_1$ and convenient for derivation, is defined as:

$$\alpha = \frac{\left(\omega_3^2 - \omega_1^2\right)^2}{\omega_3^2 \cdot \omega_1^2} = \left(\frac{\omega_3}{\omega_1} - \frac{\omega_1}{\omega_3}\right)^2.$$  \hspace{1cm} (3.10)

The component ratios $\lambda_L$ and $\lambda_C$ are defined as $\lambda_L = \sqrt{\frac{L_a}{L_b}}$ and $\lambda_C = \sqrt{\frac{C_a}{C_b}}$. The defined parameter $\alpha$ is a monotonic function of $\omega_3/\omega_1$ (since $\omega_3 > \omega_1$), and therefore $\alpha$ can be used in the derivations when evaluating the spacing between the two frequencies. By using (3.10) and the denominator of (3.5) or (3.6), the parameter $\alpha$ can be expressed as a function of the component ratios:

$$\alpha = \left[\frac{\lambda_C \left(\lambda_L + \frac{1}{\lambda_L} + 2k_{ab}\right) + \frac{1}{\lambda_C \cdot \lambda_L}}{1 - k_{ab}^2}\right] - 4$$ \hspace{1cm} (3.11)

The numerator of (3.11) shows that $\alpha$ has a minimum with respect to the capacitive ratio $\lambda_C$ given that $\lambda_L$ and $k_{ab}$ are constant. Thus, for a given tapped inductor (given $\lambda_L$ and $k_{ab}$), there is a capacitive ratio that leads to a minimum of $\alpha$, which corresponds to a minimum of $\omega_3/\omega_1$. The ratio $\lambda_{C,\min}$ at which minimum of $\omega_3/\omega_1$ is obtained, and the respective value of $\alpha_{\min}$ are:

$$\lambda_{C,\min} = \frac{1}{\sqrt{\lambda_L^2 + 2k_{ab} \cdot \lambda_L} + 1}$$ \hspace{1cm} (3.12)

$$\alpha_{\min} = 4 \cdot \left(\frac{1}{\lambda_{C,\min}^2 - \lambda_L^2 \cdot \left(1 - k_{ab}^2\right)} - 1\right).$$ \hspace{1cm} (3.13)

Fig. 3.3(a) shows graphically $\lambda_{C,\min}$ from (3.12) for different inductor geometries ($\lambda_L$ and $k_{ab}$), while Fig. 3.3(b) shows the corresponding $(\omega_3/\omega_1)_{\min}$ from (3.13), where the parameter $\alpha_{\min}$ is replaced with $(\omega_3/\omega_1)_{\min}$ using the definition of $\alpha$ (3.10). In Fig. 3.4(a) is demonstrated $(\omega_3/\omega_1)_{\min}$ when the capacitor ratio is swept in a range for few inductor geometries, which clearly indicates a minimum. A comparison between inductor with and without magnetic coupling is made in Fig. 3.4(b). The graphs presented in Fig. 3.3 and Fig. 3.4 use data that are
3.2. Fourth-order resonator using single inductor

not based on actual inductor geometries, but they show the behavior of the resonator for different inductors. These graphs can be used for initial guidelines for the VCO frequency planning and for the tapped inductor design ($\lambda_L$ and $k_{ab}$). In addition, two important conclusions can be drawn from this analysis: 1) If the two desired oscillations frequencies are closely spaced, then big $\lambda_L$ and small $\lambda_C$ should be used in the resonator (shown in Fig. 3.3(a) and (b)); 2) The magnetic coupling $k_{ab}$ between the coils separates $\omega_3$ from $\omega_1$ (Fig. 3.4(b)).

The minimum of the $\omega_3/\omega_1$ ratio occurs when the two series-resonance frequencies are equal i.e. $\omega'_2 = \omega''_2$, which can be verified by substituting (3.12) in (3.7) and (3.8). However, it can be shown that the condition for oscillation at $\omega_3$ ($\omega'^{2}_2 < \sqrt{\omega_1 \cdot \omega_2}$, equation (2.24)) is not satisfied if $\omega'_2 = \omega''_2$, and thus the minimum of $\omega_3/\omega_1$ cannot be utilized for dual-band VCOs. In order to have the dual-band operation, the condition (2.25) should be satisfied also here. Using (3.5) or (3.6), the condition (2.25) transforms into a requirement for selecting the inductor and capacitor component ratios such that

---

Fig. 3.3.  (a) $\lambda_C\text{min}$ as a function of the tapped inductor parameters $\lambda_L$ and $k_{ab}$; (b) minimum achievable frequency spacing ($\omega_3/\omega_1$) as a function of $\lambda_L$ and $k_{ab}$.

Fig. 3.4.  (a) ($\omega_3/\omega_1$) ratio versus the capacitor ratio obtained with different $\lambda$ assuming coupling of 0.5; (b) comparison of ($\omega_3/\omega_1$) with and without coupling.
\[ \lambda_C^2 \cdot \lambda_L^2 \cdot \left(1 - k_{ab}^2 \right) > 1. \tag{3.14} \]

The arrangement of the series frequencies \( \omega'_2 \) and \( \omega''_2 \) determines three possible regions of operation defined as:

Region-I: \( \omega'_2 < \omega''_2 \)

Region-II: \( \sqrt{\omega_1 \omega_3} < \omega'_2 < \omega''_2 \). \tag{3.15}

Region-III: \( \omega''_2 < \sqrt{\omega_1 \omega_3} < \omega'_2 \)

In Region-I the frequencies \( \omega'_2 \) and \( \omega''_2 \) are in opposite order, which means that at certain conditions the VCO oscillates at \( \omega_3 \) when Stage-1 is active, and at \( \omega_1 \) when Stage-2 is active. This region has only theoretical value, since the capacitive ratio \( \lambda_C \) is even smaller and provides no visible advantage. In Region-II the two series resonance frequencies are properly placed, but the dual-band condition is not satisfied and the VCO operates at single frequency band regardless of which negative-\( G_m \) stage is active. Region-III is the target region for proper dual-band operation, where the series resonances are properly situated, and the geometric mean of the desired oscillation frequencies (\( \omega_1 \) and \( \omega_3 \)) is between \( \omega''_2 \) and \( \omega'_2 \), i.e. the requirement (3.14) is satisfied.

Fig. 3.5 shows the three regions as well as the minimum attainable \( \omega_3 / \omega_1 \) for the cases with and without magnetic coupling, where the points A and B denotes the borders between the Regions I-III defined by (3.15). Dual-band operation is possible on the right-hand side of B1 and B2, where \( (\omega_3/\omega_1) > (\omega_3/\omega_1)_{\text{crit}} > (\omega_3/\omega_1)_{\text{min}} \). As seen in Fig. 3.5, the magnetic coupling \( k_{ab} \) increases the minimum \( \omega_3/\omega_1 \) ratio from 1.6 to 3.0, which further limits the possibility to put the frequency bands close to each other. In general, an inductor with small \( k_{ab} \) would facilitate the dual-band VCO design.

![Fig. 3.5. Regions of operation based on the series resonance frequencies arrangement with or without magnetic coupling: “A” corresponding to minimum \( \omega_3/\omega_1 \); “B” corresponding to critical \( \omega_3/\omega_1 \).](image-url)
3.3. Tapped-inductor design and modeling

3.3.1. Extraction of inductances and magnetic couplings

The implementation of the VCO using 4th-order resonator with a tapped inductor solely depends on the practical realization of such inductor, as the interdependence between the design parameters ($\omega_1$, $\omega_2$, $\omega_3$, $\lambda_C$, $\lambda_L$, $k_{ab}$) was demonstrated in the previous subchapter. The inductor ratio $L_a/L_b$ cannot be chosen freely, but it depends on the practical geometry. In order to ease the physical layout, the exits of the inductor should be on the opposite sides, or on the same side (see Fig. 3.6(a)). Other realizations having taping ratio different from multiples of 0.5 are also possible, but will face challenges during implementation. An inductor geometry having taping
Fig. 3.7. Tapped inductor geometry with uniform spacing between the windings used by FastHenry for extracting inductances and magnetic couplings (NT=4; TR=1.5)

Table 3-I: Tapped inductor parameters with various turns and taping ratios (W=7.5μm, IR=35μm)

<table>
<thead>
<tr>
<th>NT</th>
<th>TR</th>
<th>L₁</th>
<th>L₂</th>
<th>Lₐ</th>
<th>Lₜ</th>
<th>kₕₐ</th>
<th>λₖ</th>
<th>(Cₖₕ/Cₕₐ)ₘᵟₜ</th>
<th>(ωₖ/ωₜ)ₘᵟₜ</th>
<th>(Cₖₕ/Cₕₐ)ₖᵟᵣ</th>
<th>(ωₖ/ωₜ)ₖᵟᵣ</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.5</td>
<td>0.158</td>
<td>0.0407</td>
<td>0.299</td>
<td>1.253</td>
<td>0.493</td>
<td>0.489</td>
<td>1.72</td>
<td>6.00</td>
<td>0.18</td>
<td>10.4</td>
</tr>
<tr>
<td>4</td>
<td>1.0</td>
<td>0.283</td>
<td>0.190</td>
<td>0.884</td>
<td>0.574</td>
<td>0.474</td>
<td>1.240</td>
<td>3.72</td>
<td>3.22</td>
<td>1.19</td>
<td>3.86</td>
</tr>
<tr>
<td>4</td>
<td>1.5</td>
<td>0.486</td>
<td>0.089</td>
<td>1.527</td>
<td>0.169</td>
<td>0.431</td>
<td>3.006</td>
<td>12.6</td>
<td>2.16</td>
<td>7.36</td>
<td>2.28</td>
</tr>
<tr>
<td>5</td>
<td>0.5</td>
<td>0.187</td>
<td>0.648</td>
<td>0.357</td>
<td>2.180</td>
<td>0.486</td>
<td>0.405</td>
<td>1.56</td>
<td>6.92</td>
<td>0.13</td>
<td>13.4</td>
</tr>
<tr>
<td>5</td>
<td>1.0</td>
<td>0.341</td>
<td>0.401</td>
<td>1.074</td>
<td>1.234</td>
<td>0.473</td>
<td>0.933</td>
<td>2.75</td>
<td>3.77</td>
<td>0.68</td>
<td>4.87</td>
</tr>
<tr>
<td>5</td>
<td>1.5</td>
<td><strong>0.599</strong></td>
<td><strong>0.190</strong></td>
<td><strong>1.899</strong></td>
<td><strong>0.574</strong></td>
<td><strong>0.442</strong></td>
<td><strong>1.819</strong></td>
<td><strong>5.91</strong></td>
<td><strong>2.60</strong></td>
<td><strong>2.66</strong></td>
<td><strong>2.83</strong></td>
</tr>
<tr>
<td>5</td>
<td>2.0</td>
<td>0.790</td>
<td>0.089</td>
<td>2.695</td>
<td>0.169</td>
<td>0.393</td>
<td>3.994</td>
<td>20.1</td>
<td>1.92</td>
<td>13.5</td>
<td>1.99</td>
</tr>
<tr>
<td>6</td>
<td>1.0</td>
<td>0.400</td>
<td>0.648</td>
<td>1.271</td>
<td>2.180</td>
<td>0.471</td>
<td>0.763</td>
<td>2.30</td>
<td>4.27</td>
<td>0.45</td>
<td>5.91</td>
</tr>
<tr>
<td>6</td>
<td>1.5</td>
<td>0.717</td>
<td>0.401</td>
<td>2.288</td>
<td>1.234</td>
<td>0.446</td>
<td>1.362</td>
<td>4.07</td>
<td>2.97</td>
<td>1.48</td>
<td>3.45</td>
</tr>
<tr>
<td>6</td>
<td>2.0</td>
<td>0.961</td>
<td>0.190</td>
<td>3.313</td>
<td>0.575</td>
<td>0.410</td>
<td>2.401</td>
<td>8.74</td>
<td>2.26</td>
<td>4.80</td>
<td>2.41</td>
</tr>
</tbody>
</table>

This subsection explores different tapped inductor geometries in order to find an approximate structure permitting the desired ωₖ/ωₜ ratio. Since only λₖ and kₕₐ are needed in this step, a simplified inductor model excluding substrate losses (Fig. 3.6(b)) is used. The inductances L₁–L₄ and the magnetic couplings kᵢⱼ are obtained using 2.5-D electromagnetic simulator [49], for inductor geometries similar to the one presented in Fig. 3.7.

Table 3-I summarizes the extracted inductor parameters (Lₐ, Lₜ, kₕₐ, and λₖ) for different number of turns (NT) and different taping ratios (TR). The last columns of Table 3-I give the ratio 0.5, 1.5 and so on is preferred, since a differential capacitor bank can for C₁ and C₂ can be implemented on both sides of the inductor.
calculated \( \omega_3/\omega_1 \)\(_{\text{min}} \) and \( \omega_3/\omega_1 \)\(_{\text{crit}} \) for each inductor geometry. \( \alpha_{\text{min}} \) and \( \lambda_{\text{C, min}} \) are calculated by (3.12)-(3.13) using the obtained \( L_a, L_b, \) and \( k_{ab} \) (respectively \( \lambda_L \)), and then \( \omega_3/\omega_1 \)\(_{\text{min}} \) is obtained from the definition of \( \alpha \) (3.10). The parameters \( (C_b/C_a)_{\text{crit}} \) and \( (\omega_3/\omega_1)_{\text{crit}} \) are respectively critical capacitive and angular frequency ratios for which (3.14) is satisfied. The width of the inductor windings is 7.5 \( \mu m \), which is the maximum allowed by the CMOS process in use, with inter-winding spacing of 2 \( \mu m \) (minimum).

Based on the frequency planning of the design example, a tapped inductor whose \( (\omega_3/\omega_1)_{\text{crit}} \) is 3 or less should be realized. A smaller \( (\omega_3/\omega_1)_{\text{crit}} \) would be beneficial in supressing the unwanted resonance (\( \omega_3 \) for the LF band, \( \omega_1 \) for the HF band). Furthermore, an exact realization of \( \lambda_{\text{C, min}} \) would be difficult for implementation and it will be sensitive to layout parasitic capacitances. Thus, a good safety margin for \( (\omega_3/\omega_1)_{\text{crit}} \) should be provided by the inductor itself.

As shown in Table 3-I, the best inductor candidate is having 5 turns and taping ratio of 1.5. Other realizations also satisfy the initial requirement of \( (\omega_3/\omega_1)_{\text{crit}} \) being less than 3, but they have either big \( C_a / C_b \) ratio (NT = 4; TR = 1.5), or will require placing the capacitor bank on the same side on the inductor (NT = 6; TR = 2.0). The achievable \( (\omega_3/\omega_1)_{\text{crit}} \) jumps with big steps from one inductor topology to another, which gives a hint that a fine adjustment of the inductor parameters should be seek by varying other parameters using the selected NT and TR. Thus, the further investigation is based on inductor having NT=5 and TR=1.5.

Table 3-II summarizes the tapped inductor parameters obtained by varying the inner inductor radius (IR) while keeping fixed the winding width, the number of turns, and the taping ratio. The results presented above shows that a fine adjustment of \( (\omega_3/\omega_1)_{\text{crit}} \) can be achieved. Fine adjustment can be achieved also for decreasing width of the winding (results not presented here), but with the expense of \( Q \)-factor degradation. A smaller inner radius also provides smaller \( (\omega_3/\omega_1)_{\text{crit}} \) for the selected topology. A side benefit when selecting smaller inner radius

<table>
<thead>
<tr>
<th>IR (um)</th>
<th>( L_1 ) (nH)</th>
<th>( L_2 ) (nH)</th>
<th>( L_a ) (nH)</th>
<th>( L_b ) (nH)</th>
<th>( k_{ab} )</th>
<th>( \lambda_L )</th>
<th>( (C_b/C_a)_{\text{min}} )</th>
<th>( (\omega_3/\omega_1)_{\text{min}} )</th>
<th>( (C_b/C_a)_{\text{crit}} )</th>
<th>( (\omega_3/\omega_1)_{\text{crit}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>35</td>
<td>0.599</td>
<td>0.190</td>
<td>1.899</td>
<td>0.574</td>
<td>0.442</td>
<td>1.819</td>
<td>5.91</td>
<td>2.60</td>
<td>2.66</td>
<td>2.83</td>
</tr>
<tr>
<td>40</td>
<td>0.661</td>
<td>0.218</td>
<td>2.102</td>
<td>0.666</td>
<td>0.457</td>
<td>1.177</td>
<td>5.78</td>
<td>2.67</td>
<td>2.50</td>
<td>2.98</td>
</tr>
<tr>
<td>45</td>
<td>0.723</td>
<td>0.246</td>
<td>2.309</td>
<td>0.760</td>
<td>0.470</td>
<td>1.743</td>
<td>5.68</td>
<td>2.73</td>
<td>2.37</td>
<td>3.07</td>
</tr>
<tr>
<td>50</td>
<td>0.787</td>
<td>0.276</td>
<td>2.520</td>
<td>0.857</td>
<td>0.482</td>
<td>1.715</td>
<td>5.60</td>
<td>2.79</td>
<td>2.26</td>
<td>3.16</td>
</tr>
<tr>
<td>60</td>
<td>0.917</td>
<td>0.336</td>
<td>2.953</td>
<td>1.057</td>
<td>0.503</td>
<td>1.672</td>
<td>5.48</td>
<td>2.89</td>
<td>2.09</td>
<td>3.23</td>
</tr>
</tbody>
</table>
is a reduced silicon area, respectively decreased substrate losses allowing high frequency of operation.

Despite the achieved \(\omega_3/\omega_1\)\textsubscript{crit} < 3 for the inductor having IR=35\,\mu m, the safety margin for \(\omega_3/\omega_1\)\textsubscript{crit} is small and may cause undesired behavior when all components are replaced with their actual model – inductor with all parasitic components included, finite \(Q\)-factor of the capacitors, and frequency limitations of the negative-\(G_m\) stages. As shown in Fig. 3.4(b) and Fig. 3.5, a decrease of the magnetic coupling \(k_{ab}\) gives additional margin for \(\omega_3/\omega_1\)\textsubscript{crit} for the same inductor geometry. A close inspection of \(k_{ab}\) defined by (3.3) suggests its reduction: by maximizing \(k_{14}\) and \(k_{23}\), and by minimizing \(k_{12}\) and \(k_{13}\). From topology point of view, this suggestion translates to a design guideline for keeping the minimum allowed spacing between the \(L_1\) and \(L_4\) winding, and between the \(L_2\) and \(L_3\) winding (maximizing \(k_{14}\) and \(k_{23}\)). Increasing of all other winding spacing will result in decrease of \(k_{12}\) and \(k_{13}\), which in fact comes to increasing only the spacing between the \(L_1-L_4\) winding set and the \(L_2-L_3\) winding set (denoted with S12). An inductor structure realizing both guidelines (smaller \(k_{ab}\)) is demonstrated in Fig. 3.8. A twisted-inductor approach could bring \(k_{ab} \approx 0\) [121], but it would eventually require two inductors, or complex tapped-inductor structure.

Table 3-III summarizes the extracted with FastHenry inductor parameters when the non-uniform spacing S12 is increased in steps of 2 \(\mu m\) for inner radius of 35 \(\mu m\), 40 \(\mu m\), and 45 \(\mu m\). The number of turns, taping ratio, and width are kept constant following the conclusions drawn from Table 3-I and Table 3-II. As seen from Table 3-III, increased non-uniform spacing
3.3. Tapped-inductor design and modeling

Table 3-III: Tapped inductor parameters with various number of turns and taping ratios (W=7.5 μm)

<table>
<thead>
<tr>
<th>IR</th>
<th>S12</th>
<th>L_1</th>
<th>L_2</th>
<th>L_a</th>
<th>L_b</th>
<th>k_ab</th>
<th>λ_l</th>
<th>(C_b/C_a)_{min}</th>
<th>(ω_b/ω_1)_{min}</th>
<th>(C_b/C_a)_{crit}</th>
<th>(ω_b/ω_1)_{crit}</th>
</tr>
</thead>
<tbody>
<tr>
<td>μm</td>
<td>nH</td>
<td>nH</td>
<td>nH</td>
<td>nH</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>35</td>
<td>2</td>
<td>0.57</td>
<td>0.18</td>
<td>1.85</td>
<td>0.56</td>
<td>0.46</td>
<td>1.82</td>
<td>5.98</td>
<td>2.64</td>
<td>2.63</td>
<td>2.93</td>
</tr>
<tr>
<td>4</td>
<td>0.59</td>
<td>0.18</td>
<td>1.92</td>
<td>0.56</td>
<td>0.42</td>
<td>1.85</td>
<td>6.00</td>
<td>2.52</td>
<td></td>
<td>2.83</td>
<td>2.76</td>
</tr>
<tr>
<td>6</td>
<td>0.62</td>
<td>0.18</td>
<td>2.00</td>
<td>0.56</td>
<td>0.39</td>
<td>1.89</td>
<td>6.04</td>
<td>2.42</td>
<td></td>
<td>3.01</td>
<td>2.63</td>
</tr>
<tr>
<td>8</td>
<td>0.64</td>
<td>0.18</td>
<td>2.08</td>
<td>0.56</td>
<td>0.37</td>
<td>1.92</td>
<td>6.09</td>
<td>2.34</td>
<td></td>
<td>3.18</td>
<td>2.52</td>
</tr>
<tr>
<td>10</td>
<td>0.66</td>
<td>0.19</td>
<td>2.15</td>
<td>0.57</td>
<td>0.35</td>
<td>1.95</td>
<td>6.15</td>
<td>2.28</td>
<td>3.34</td>
<td></td>
<td>2.43</td>
</tr>
<tr>
<td>40</td>
<td>2</td>
<td>0.63</td>
<td>0.21</td>
<td>2.05</td>
<td>0.65</td>
<td>0.47</td>
<td>1.78</td>
<td>5.84</td>
<td>2.71</td>
<td>2.47</td>
<td>3.04</td>
</tr>
<tr>
<td>4</td>
<td>0.66</td>
<td>0.21</td>
<td>2.12</td>
<td>0.65</td>
<td>0.44</td>
<td>1.81</td>
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<td></td>
<td>2.65</td>
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</tr>
<tr>
<td>6</td>
<td>0.68</td>
<td>0.21</td>
<td>2.20</td>
<td>0.65</td>
<td>0.41</td>
<td>1.84</td>
<td>5.88</td>
<td>2.49</td>
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<td>2.81</td>
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</tr>
<tr>
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<td>0.70</td>
<td>0.21</td>
<td>2.28</td>
<td>0.66</td>
<td>0.39</td>
<td>1.87</td>
<td>5.92</td>
<td>2.41</td>
<td></td>
<td>2.97</td>
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</tr>
<tr>
<td>10</td>
<td>0.72</td>
<td>0.21</td>
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<td>0.66</td>
<td>0.36</td>
<td>1.90</td>
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<tr>
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<td>2.25</td>
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<td>0.48</td>
<td>1.75</td>
<td>5.74</td>
<td>2.78</td>
<td>2.33</td>
<td>3.14</td>
</tr>
<tr>
<td>4</td>
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<td>2.33</td>
<td>0.74</td>
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<td>5.74</td>
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<tr>
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<td>0.74</td>
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<td>2.41</td>
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<td>1.80</td>
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<tr>
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<td>0.76</td>
<td>0.24</td>
<td>2.49</td>
<td>0.75</td>
<td>0.40</td>
<td>1.82</td>
<td>5.78</td>
<td>2.47</td>
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<td>2.57</td>
<td>0.75</td>
<td>0.38</td>
<td>1.85</td>
<td>5.82</td>
<td>2.40</td>
<td></td>
<td>2.94</td>
<td>2.60</td>
</tr>
</tbody>
</table>

improves significantly the safety margin for (ω_b/ω_1)_{crit}: the required ratio is 3, the ratio achieved with uniform spacing is 2.83 (Table 3-II), which is reduced down to 2.43 with non-uniform winding spacing. The margin between 2.43 and 3 is considered sufficient for the design example to provides secure operation on the two bands, and to allow freedom when designing the switched-capacitor banks. The C_b/C_a required by the selected inductor geometry is also feasible for realization.

3.3.2. Modeling of the substrate losses

A complete model of tapped inductor including losses is essential for the successful design and implementation of the dual-band VCO. The simplified model involving only inductances and magnetic coupling was important for the selection of the inductor topology, but further refinement is needed in order to account for the resistive losses and for the substrate losses. The electrical model of the selected inductor from Table 3-III is given in Fig. 3.9. The inductances

![Fig. 3.9. Complete model of the tapped inductor](image-url)
and the magnetic couplings are obtained with FastHenry. The network modeling the substrate losses is obtained as follow:

\[
C_{ox1} = \frac{l_1}{2l_{tot}} C_{tot}; \quad C_{ox2} = \frac{l_1+l_2}{2l_{tot}} C_{tot}; \quad C_{CT} = \frac{l_2}{l_{tot}} C_{tot}; \quad (3.16)
\]

where \(l_1\) is the length of the wire for \(L_1(L_4)\), \(l_2\) is the length of the wire for \(L_2(L_3)\), \(l_{tot}\) is the total length of the inductor winding, \(C_{tot}\) is the total capacitance towards the substrate. The substrate resistance \(R_{sub}\) seen at one end of the inductor is modeled based on the procedure outlined in [82], where the substrate resistance associated with a primary winding of a transformer is:

\[
R_{subP} = \frac{\rho}{2\pi l_{MP}} \ln \left[ 2 \coth \left( \frac{\pi}{8} \left( \frac{W_p + 6H_{ox} + T}{H_{sub}} \right) \right) \right], \quad (3.17)
\]

where \(R_{OP}\) is the outermost radius of the primary winding; \(R_{IP}\) is the innermost radius of the primary winding; \(W_p = R_{OP} - R_{IP}\) is the complete width of the primary transformer winding; \(\rho\) is the substrate resistivity; \(H_{ox}\) is the transformer alleviation from the substrate; \(T\) is the conductor thickness; \(H_{sub}\) is the substrate thickness; and \(l_{MP} = \pi (R_{OP} + R_{IP})\).

The transformer parameters modeling the resistive substrate loss are calculated as \(R_{sub1} = R_{sub2} = 4 \cdot R_{subP}\), and \(R_{subCT} = 2 \cdot R_{subP}\). Since the modeling in [82] assumes that the two winding are differentially driven, a small modifications of (3.17) is adopted in the tapped inductor modeling. The equations used for calculating the substrate resistors are

\[
R_{sub1} = \frac{\rho}{2\pi l_{M,1T}} \ln \left[ 2 \coth \left( \frac{\pi}{8} \left( \frac{(OR_{1T} - IR) + 6H_{ox} + T}{H_{sub}} \right) \right) \right], \quad (3.18)
\]

\[
l_{M,1T} = \frac{\pi}{2} (OR_{1T} + IR) \quad (3.19)
\]

\[
R_{sub2} = \frac{\rho}{2\pi l_{M,2T}} \ln \left[ 2 \coth \left( \frac{\pi}{8} \left( \frac{(OR_{2T} - IR) + 6H_{ox} + T}{H_{sub}} \right) \right) \right], \quad (3.20)
\]

\[
l_{M,2T} = \frac{\pi}{2} (OR_{2T} + IR) \quad (3.21)
\]

where the geometry parameters \(OR_{1T}, OR_{2T}\), and \(IR\) are visualized in Fig. 3.7. Equation (3.18) is identical to (3.17) and it computes the substrate resistors \(R_{sub1}\) connected to the 1L and 1R inductor ports. Equation (3.20) has a similar form, but the outer radius \(OR_{2T}\) corresponds to the dimension of the inductor’s inner windings. A typical differential inductor model has only \(R_{sub1}\) on each inductor side, while the tapped inductor model has an additional \(R_{sub2}\). Thus, the adopted modeling of the substrate losses for the tapped inductor is a slightly pessimistic. The
goal of the slightly pessimistic modeling is to make sure that the negative-$G_m$ stages are designed to guarantee oscillations even with increased inductor losses.

Another possible approach for tapped inductor modeling is reported in [35].

### 3.3.3. Electrical models of the selected inductor geometry

<table>
<thead>
<tr>
<th>Band</th>
<th>$L_1, L_4$ (pH)</th>
<th>$r_{s1}, r_{s4}$ (Ω)</th>
<th>$L_{2}, L_{3}$ (pH)</th>
<th>$r_{s2}, r_{s3}$ (Ω)</th>
<th>$k_{14}$</th>
<th>$k_{23}$</th>
<th>$k_{12}, k_{34}$</th>
<th>$k_{13}, k_{24}$</th>
<th>$R_{sub1}$ (Ω)</th>
<th>$C_{ox1}$ (fF)</th>
<th>$R_{sub2}$ (Ω)</th>
<th>$C_{ox2}$ (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LF</td>
<td>607.1</td>
<td>0.809</td>
<td>192.6</td>
<td>0.375</td>
<td>0.598</td>
<td>0.544</td>
<td>0.270</td>
<td>0.318</td>
<td>637</td>
<td>42.35</td>
<td>831</td>
<td>61.62</td>
</tr>
<tr>
<td>HF</td>
<td>589.9</td>
<td>1.366</td>
<td>184.5</td>
<td>0.635</td>
<td>0.614</td>
<td>0.570</td>
<td>0.284</td>
<td>0.332</td>
<td>637</td>
<td>42.35</td>
<td>831</td>
<td>61.62</td>
</tr>
</tbody>
</table>

The electrical model shown Fig. 3.9 is used in the VCO simulations. The inductor model parameters for the two frequency band are summarized in Table 3-IV. Two different inductor models are used for each frequency band, since the model in Fig. 3.9 is valid in a narrow frequency range. This procedure has been selected in favor of a single broadband model, which would further complicate the tapped inductor modeling. The extraction of the series resistors $r_{s1}, r_{s4}$ is obtained with FastHenry, which accounts for the increased ohmic resistance of the winding caused by the skin effect. The substrate-related model components are derived based on the process specific parameters as outlined in 3.3.2. The estimated inductor $Q$-factor is 16.8 at 2GHz (simulated between the 1L and 1R inductor ports), and 10.5 at 6GHz (simulated between the 2L and 2R ports).

### 3.4. Conditions for oscillations using root-locus diagram

Similarly to Subchapter 2.3, the root-locus method verifies the proper dual-band operation when all parasitic components are included into the resonance tank (as previously mentioned, the parameter $(\omega_3/\omega_1)_{crit}$ obtained for the tapped inductor is based on simplified models). Since the equivalent circuit becomes a lot more complicated than the one in Subchapter 2.3, a derivation of a polynomial would not bring additional design insights. Instead, the root-locus is obtained numerically using a procedure that is described in Chapter 5, which is used for the Time-Varying Root-Locus. Briefly, the equivalent circuit is represented in the form $Y(s) = G + s \cdot B$, and QZ method is used for computing the roots when varying the negative conductance.

Fig. 3.10 shows the equivalent circuit used for evaluating the root-loci for the two bands. The tapped inductor is represented with its model from Fig. 3.9 and Table 3-IV. The capacitor $C_{ox1} = 2.979pF$ and $C_{ox2} = 5.928pF$ are the equivalent capacitances realized by the switched
Fig. 3.10. Equivalent circuit for evaluating the root-loci for: (a) low-frequency band; (b) high-frequency band

Fig. 3.11. Root-loci for the LF band with varied negative conductance: (a) low-frequency root; (b) high-frequency root

Fig. 3.12. Root-loci for the HF band with varied negative conductance: (a) low-frequency root; (b) high-frequency root

capacitor banks for the two bands described in 3.6.1. The resistors $r_{o1} = 344.5\, \text{m}\Omega$ and $r_{o2} = 176.4\, \text{m}\Omega$ model the finite $Q$-factor of the two capacitor banks. Both $Q$-factors are almost identical as the two banks are involved in the frequency generation for both frequency bands. The $Q$-factors are approximately 76.1 and 25.3 simulated at 2GHz and 6GHz respectively.

Fig. 3.11 and Fig. 3.12 show the obtained root-loci when varying the negative conductance generated by the cross-couple pairs. When the low-frequency cross-coupled pair is active (Fig. 3.11), the root that is close to 2 GHz crosses first the imaginary axis at a value of $|G_m| \approx 1.90$
mS, whereas the root close to 6GHz needs at least 44.9 mS to enter the positive part of the s-plane.

The wide range of $G_{m1}$, for which only one root pair is in the RHP, guarantees oscillations and secured operation at the low-frequency band. With high-frequency cross-coupled pair active (Fig. 3.12), the high-frequency root crosses first the $j\omega$ axis at $|G_{m2}| \approx 17.5$ mS, which assures that the high-frequency band also operates properly. The range 17.5-24.5 mS for $G_{m2}$ secures that only one complex-conjugated pair has positive real part and the undesired multi-tone oscillations are avoided.

### 3.5. Adaptive frequency tuning of the oscillator

The frequency tuning of the tapped-inductor VCO is achieved in the traditional way by replacing the tank capacitors $C_{o1}$ and $C_{o2}$ with varactors, or with switched capacitors. The two tank capacitors in the 4th-order resonator gives a freedom to control $C_{o1}$ and $C_{o2}$ separately, thus a selection of appropriate frequency control strategy is required. This subchapter investigates the different possibilities for frequency control, and their effect on the oscillator behavior.

The simplest method for frequency control is to vary the tank capacitors proportionally. This method keeps the oscillator behavior unchanged since the frequency ratios $\omega_3/\omega_1$ and $\omega_2/\omega_1$ remain constant. The impedance seen from the negative-$G_m$ stage, however, increases with the oscillation frequency, which is also typical for standard LC oscillators. This method reduces the frequency control complexity and it can be directly integrated with the existing PLL to use only one control voltage or frequency-control-word (FCW).

In order to evaluate other frequency control strategies, here are investigated the extreme cases in which one of the capacitor bank is swept from its minimum capacitance value till its maximum capacitance value (minimum denoted with “0”, maximum denoted with “1”), while the other one is kept constant (at its minimum, or at its maximum capacitance value). The evaluation considers the ratio $\omega_3/\omega_1$ and the impedance seen from the negative-$G_m$ stage, but other important parameters such as $Z(\omega_3)/Z(\omega_1)$ can be evaluated too. The extreme cases including the standard control strategy can be summarized as:

<table>
<thead>
<tr>
<th>Strategy</th>
<th>$C_1$</th>
<th>$C_2$</th>
<th>Region</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>max - min</td>
<td>max - min</td>
<td>AB</td>
</tr>
<tr>
<td>#2</td>
<td>1</td>
<td>max - min</td>
<td>AC</td>
</tr>
<tr>
<td>#3</td>
<td>max - min</td>
<td>0</td>
<td>CB</td>
</tr>
<tr>
<td>#4</td>
<td>max - min</td>
<td>1</td>
<td>AD</td>
</tr>
<tr>
<td>#5</td>
<td>0</td>
<td>max - min</td>
<td>DB</td>
</tr>
</tbody>
</table>

Table 3-V: Frequency control strategies
Fig. 3.13. 4th-order resonator behavior for different frequency control strategies for the high-frequency band: (a) $\omega_3 / \omega_1$ ratio; (b) $Z(\omega_3) / Z(\omega_1)$ impedance ratio seen from the Negative-Gm stage

Fig. 3.14. 4th-order resonator behavior for different frequency control strategies for the low-frequency band: (a) $\omega_3 / \omega_1$ ratio; (b) $Z(\omega_3) / Z(\omega_1)$ impedance ratio seen from the Negative-Gm stage

Fig. 3.13 and Fig. 3.14 show the angular frequency ratios $\omega_3 / \omega_1$ and the corresponding impedance ratio $Z(\omega_3) / Z(\omega_1)$ visualizing the frequency control strategies for the two frequency bands. The data for the plots are obtained with Spectre simulations including the complete inductor model and extracted capacitor banks. Fig. 3.13 shows that only the AB strategy alone covers the entire tuning range. However, the complete tuning range can be achieved also by combining strategy #2 and #3 (A-C-B line), or #4 and #5 (A-D-B line), but the properties of the 4th-order resonator are different.

When operating on the ACB line, or above the AB line, the ratio $\omega_3 / \omega_1$ is bigger and respectively the equivalent impedance at resonance is bigger. The impedance ratio $Z(\omega_3) / Z(\omega_1)$ has similar to $\omega_3 / \omega_1$ shape i.e. the conditions for assuring single frequency generation are relaxed when operating above the AB line. Similarly, if the oscillator operates below the AB line, there are more chances for the VCO to start oscillations at the unwanted frequency ($\omega_1$). In general, an operation above the AB line should be the preferred choice to reduce power consumption given that the VCO swing is kept constant.
3.5. Adaptive frequency tuning of the oscillator

Fig. 3.15. Simplified sketch of the frequency control strategies for the high-frequency band

Table 3-VI: Cadence simulation results for K, L, and M (~ 6.5GHz)

<table>
<thead>
<tr>
<th>Point</th>
<th>Region</th>
<th>$C_1$</th>
<th>$C_2$</th>
<th>Fosc (MHz)</th>
<th>Vpp (V)</th>
<th>Idd (mA)</th>
<th>$\mathcal{L}$ @ 1MHz (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>K</td>
<td>AC</td>
<td>31 / 31</td>
<td>15 / 31</td>
<td>6498</td>
<td>1.229</td>
<td>25.9</td>
<td>-119.9</td>
</tr>
<tr>
<td>L</td>
<td>AB</td>
<td>17 / 31</td>
<td>17 / 31</td>
<td>6490</td>
<td>1.231</td>
<td>28.5</td>
<td>-120.9</td>
</tr>
<tr>
<td>~M</td>
<td>~DB</td>
<td>7 / 31</td>
<td>19 / 31</td>
<td>6589</td>
<td>1.211</td>
<td>30.9</td>
<td>-121.7</td>
</tr>
</tbody>
</table>

Similar conclusion can be drawn for the lower frequency band, with the similar plots shown in Fig. 3.14. The frequency-control-strategy effect on the equivalent impedance is less visible at the low-frequency bands, and usually the lower band is less prone to the unwanted oscillations at $\omega_2$.

As discussed above, the use of different frequency control strategies leads to different properties of the resonator at a given frequency. This is opposite to traditional $LC$ oscillators, where the properties of resonance tank are fixed for a given frequency. The flexibility of frequency control in the 4th-order resonator creates a possibility to utilize a tradeoff between power consumption and phase noise, i.e. to make the frequency control adaptive to the application’s specifics. In Fig. 3.15 are shown the frequency control strategies for the high-frequency band, and three possible operating points $K$, $L$ and $M$ for an oscillation frequency of 6.5 GHz. Point $K$ lies on the AC control line, point $L$ lies to the AB line, and point $M$ corresponds to the DB line as defined in Fig. 3.13. It is obvious that for these three points the oscillator will have different behavior since the resonator has different properties. To evaluate the phase noise behavior of the oscillator, the voltage swing is kept nearly constant, and the SpectreRF simulation results are summarized in Table 3-VI.

The capacitor $C_2$ is connected between the resonance node and ground for the HF band, and it has the highest value for point $M$ as listed in Table 3-VI. Since the oscillator phase noise is
proportional to $10 \log_{10} \left( \frac{1}{q_{\text{max}}^2} \right)$ [63], where $q_{\text{max}} = C \cdot V_{\text{max}}$, $C$ is the tank capacitor, and $V_{\text{max}}$ is the maximum voltage swing, the phase noise should be the lowest at point $M$ given that $V_{\text{max}}$ is kept constant. The simulated VCO phase noise is summarized in Table 3-VI for a voltage swing of $\sim 1.2\,\text{V}_{\text{PP}}$, which confirms reduced phase noise and increased current consumption below the AB line. However, as the operation moves towards the DB line, it is likely that the oscillation will start at $\omega_1$ instead of $\omega_3$, and that is why the actual $M$ point cannot be reached in this design example.

The described feature of the 4th-order tank can be utilized for adaptive adjustment for achieving the desired phase noise performance with minimum power consumption. Low-power applications should target operation above the AB line, whereas high-performance applications should target operation below the AB line. Such an adaptive frequency tuning does not exist in the standard $LC$ oscillators, since the power consumption and the phase noise in 2nd-order oscillators are fixed for a given $LC$ tank, frequency of operation, and voltage swing.

### 3.6. Electrical design of the VCO building blocks

#### 3.6.1. Switched-capacitor banks

The switched-capacitor banks used for frequency tuning utilize unit-cells MOM capacitors, whose simulated $Q$-factor is 126.7 and 31.7 at 2GHz and 8GHz respectively. The parasitic capacitance of the MOM capacitor towards the substrate reduces the $C_{\text{on}}/C_{\text{off}}$ ratio of the switched-capacitor bank down to approximately 9. The structure of the switched-capacitor bank shown in Fig. 3.16 is utilized for both frequency bands. This structure allows obtaining maximum $Q$-factor for a given $C_{\text{on}}/C_{\text{off}}$ ratio [147]. The pull-up resistors bias the MOS switch $M_{\text{SW}}$ in the minimum capacitance state when $M_{\text{SW}}$ is turned off, and pulls down the source and drain potentials to zero in order to provide the minimum channel resistance of $M_{\text{SW}}$ in on-state. The selected pull-up / pull-down resistor loads the resonator negligibly and occupies small silicon area.

The switched capacitor banks for both frequency bands are made with equal capacitance-

![Six-bit binary-weighted differential switched capacitor bank](image)

**Fig. 3.16.** Six-bit binary-weighted differential switched capacitor bank
3.6. Electrical design of the VCO building blocks

to-transistor-size ratio, since they both take part in the resonator regardless of the selected frequency band. This approach eases the physical design of the VCO, as well as making the consequent evaluation straightforward. An eventual optimization with respect to different capacitance / MOS size ratio could provide certain benefits, but it is outside of the scope of this design example. Each unit capacitor is switched by a minimum-channel-length MOS device with size $W/L = (18/0.04) \ \mu m$. The capacitor bank design provides switched-capacitance $Q$-factor of 77 and 25, simulated at 2-GHz and 6-GHz respectively (2 GHz and 6 GHz are the low-frequency ends of the two frequency bands when the $M_{SW}$ is in on-state). The $C_{on}/C_{off}$ ratio of the banks is $\sim 2.09$ (the simulated single-ended capacitance for the LF band is $C_{on}/C_{off} = (2.979 / 1.425) \ \text{pF}$, and $C_{on}/C_{off} = (5.928 / 2.826) \ \text{pF}$ for the HF band). The minimum $C_{on}/C_{off}$ ratio is limited by the required frequency bands that the VCO should cover. Better $Q$-factor of the bank can be achieved if the frequency range is reduced by making larger MOS switch, which would reduce the $C_{on}/C_{off}$ ratio.

3.6.2. Negative-$G_m$ cells

The structures of the negative-$G_m$ cells are shown in Fig. 3.17. A simple cross-coupled pair $M_{HB,1}$ and $M_{HB,2}$ provides the negative resistance for the high-frequency band (Fig. 3.17(b)). Low-voltage high-speed MOS devices are selected for the HF band, because the needed negative $g_m$ is large ($>17\text{mS}$, as shown in Fig. 3.12). With the given transistor sizes, the cells provides up to 45 mS in start-up conditions (see Fig. 3.18(b)), which satisfy the root-locus criteria for safe operation. The needed $g_m$ can be adjusted using the digitally programmable current source in a wide range depending on the desired voltage swing and oscillation frequency.

The negative-$G_m$ cell for the low-frequency band (shown in Fig. 3.17(a)) uses small-size high-voltage devices, because the voltage amplitude can go higher than the supply voltage with moderate bias currents. The negative-$G_m$ cell can be completely shut-downed by tying the gate

![Fig. 3.17. Negative-$G_m$ cell for: (a) LF Band; (b) HF Band](image-url)
voltage terms to ground with additional enable logic. This design feature prevents the transistors $M_{LB,1}$ and $M_{LB,2}$ to enter the triode region when the VCO operates at the high-frequency band. With the given transistor sizes, the cell provides $2.5–4.5$ mS in start-up conditions (see Fig. 3.18(a)), which satisfy the root-locus criteria presented in Fig. 3.11.

### 3.6.3. Programmable bias and $\textit{LC}$ filter

The structure of the controllable current mirror is shown in Fig. 3.19. It consists of long channel-length MOS transistors ($M_1$) that are “enabled” by a minimum-channel-length device ($M_2$) in a cascade configuration. The $M_2$ transistor should have low on-resistance, while the size of the $M_1$ transistor is optimized for good phase noise performance. This configuration is essentially the one proposed by Andreani in [7]. Since this configuration is used in the HF band, where the power consumption is big, the VCO current determines the large size of the transistor. The programmability of the current mirror allows fine regulation of the generated voltage swing in the VCO. The current mirror MOS transistors operate mostly in triode region, where the flicker noise up-conversion is minimized. The digital control $I_{\text{CM}<4:0>}$ determines the degeneration resistance used for the cross-coupled pair that generates the needed negative conductance for proper VCO operation.

The bias circuitry used for the LF band is essentially the same as the one shown in Fig. 3.19, but with added additional $\textit{LC}$-filtering network in order to improve the oscillator phase.
3.6. Electrical design of the VCO building blocks

3.6.4. Output buffer

The schematic of the output buffer is shown in Fig. 3.21, which has a two-stage pseudo-differential structure. The first stage of the buffer is a CMOS inverter, whose input is dc-biased to $V_{DD}/2$ through the biasing network formed with $R_{b1}$, $R_{b2}$, $R_{g,L}$, and $R_{g,R}$. The high-ohmic resistive biasing provides minimal loading for the resonator. The 1.1-V buffer power supply is separated from the VCO power supply to reduce interferences and to allow measurement of the drained currents from each block. The first stage of the buffer is built with minimum-channel-length devices to assure fast switching for high input frequencies. The size of the open-drain transistor is optimized for low phase-noise floor using SpectreRF. The biasing of the drains is supplied externally (“VDD_OD”) with a 0.6 V voltage source. The bias-tee has a realistic

![Fig. 3.21. Schematic of the output buffer used for both frequency bands](image)
model for the use in simulations. The input impedance of the spectrum analyzer or other measurement device is assumed 50Ω. All simulations presented below are done with two output buffers connected to the VCO outputs.

The same buffer structure is used for the two bands. The pseudo-differential structure has no synchronization between the two branches, but that is not critical in the design example since the buffer is used only for measuring phase noise where small imbalances are not critical.

Even with moderate VCO swing, the CMOS inverter \( M_{n,L} - M_{p,L} \) transforms the sinusoidal input signal into nearly a square wave, which consequently drives the open-drain MOS transistors. Fig. 3.22 shows the time-domain waveforms of the CMOS inverter obtained for two different input frequencies, which are the minimum LF-band VCO frequency and the maximum HF-band VCO frequency. Due to the limited switching speed of the CMOS inverter, its output at 8-GHz input frequency approaches sinusoidal waveform, which gives a rise of power consumption and generated noise.

Fig. 3.23 shows the simulated noise performance of the buffer as a standalone block. The phase noise gets worse for higher input frequencies and lower voltage swings. Both effects decrease the switching speed of the inverter and produces higher current consumption for the

---

**Fig. 3.22.** Internal buffer waveforms at: (a) \( f_{in} = 2 \text{GHz} \); (b) \( f_{in} = 8 \text{GHz} \).

---

**Fig. 3.23.** Buffer phase noise performance for different input swings: (a) \( V_{pp}=1.25\text{V} \); (b) \( V_{pp}=1.50\text{V} \).
buffer. The phase noise of the buffer is governed by flicker noise, which is generated inside the buffer, with $M_{n,L}$ ($M_{n,R}$) being the biggest noise contributor. The performance of the buffer is summarized by Fig. 3.24, where the buffer phase noise at 1MHz offset is shown as a function of the input frequency and the input voltage swing (Fig. 3.24(a)). The corresponding current consumption is shown in Fig. 3.24(b).

The phase noise of the buffer can be improved by increasing the sizes of the transistors in the CMOS inverter in order to increase the switching speed. However, this will limit the upper frequency range of the buffer itself due to increased capacitive load. When compared to the resulting VCO phase noise, the buffer phase noise at 1MHz offset is 10-20 dB smaller, which means that the buffer does not deteriorate the system performance and it should provide reliable measurement environment.

### 3.7. Simulation results of the tapped inductor VCO

Fig. 3.25(a) shows the simulated VCO phase noise for three different frequencies at the LF band.
CHAPTER 3: DUAL-BAND VCO USING TAPPED INDUCTOR

Fig. 3.26. Simulated phase noise at 1-MHz offset and the respective power consumption for: (a) LF band; (b) HF band.

band (at the minimum oscillation frequency, at the maximum oscillation frequency, and in the middle of the tuning range). Fig. 3.25(b) shows the VCO phase noise performance at HF band obtained in similar conditions. The oscillator phase noise at 1-MHz frequency offset is demonstrated in Fig. 3.26 for the two bands with given power consumption for specific points of the tuning range.

The phase noise for both bands displays significant flicker noise at the upper part of the tuning range. This effect is clearly visible in Fig. 3.26(b), where the flicker noise contribution at 1MHz offset rises quickly for VCO frequencies above 7 GHz. The reason for the flicker noise increase is the limited speed of the output buffer, and especially the CMOS inverter in the first buffer stage (Fig. 3.21), which is not able to switch quickly. The limited speed of inverter increases the buffer current and respectively the generated noise.

As described in section 3.6.3, a programmable LC-filter is implemented for the low-frequency-band bias circuitry in order to improve the oscillator phase noise [69]. Fig. 3.27(a) shows the simulated phase noise for different values of the filtering capacitor compared against the oscillator phase noise when the additional MOS switch in Fig. 3.20 is enabled. Fig. 3.27(b) shows the respective FoM. As shown in the plots, the phase noise improvement is around 2 dB

Fig. 3.27. LC-filter effect on the phase noise and FoM for the LF band for 1.5-Vpp voltage swing
at the lowest oscillation frequency, but the phase noise improvement vanishes at the higher end of the LF band.

The phase noise and FoM optimum in Fig. 3.27 is achieved with “FILT=0” corresponding to the minimum switchable capacitance in the LC-filter. The obtained result suggests that the total capacitance connected to the common node of the cross-coupled pair is higher than needed for achieving proper noise filtering. This artifact is caused by the large MOS switch that shortens the filtering inductor, which introduce a significant capacitance to the sensitive common node. To verify this conclusion, a set of simulations were performed in which the MOS switch is removed and the value of the switched filtering capacitor is increased by a factor of 1.5. The simulated phase noise and FoM are demonstrated in Fig. 3.28(a) and (b). Now the phase noise is improved over the entire frequency range of the LF band and FoM has clear minimum. Fig. 3.28(b) demonstrates how the FoM optimum is achieved with different capacitance value (“FILT”) depending on the VCO frequency. For instance the FoM optimum at 2 GHz is achieved for “FILT=15” (all filtering capacitance are “on”), and the FoM optimum at 2.7GHz is achieved for “FILT=0” (all filtering capacitance are “off”). The FoM optimum can be achieved at a given oscillation frequency by adjusting the filtering capacitor through FILT. With well-centered design, the digital signal FILT can be tied to the digital signal adjusting the oscillation frequency, thus no additional complexity would be required for the PLL system.

The MOS switch that was placed in the test chip for test purposes does not allow evaluation of the FoM optimum as presented in Fig. 3.28. However, this switch is not needed in real VCO design, and the full benefit of using LC-filter can obtained. The restriction for obtaining the FoM optimum posed by the large MOS switch was not observed in the design phase of this VCO example.
3.8. Physical design and measurements

The dual-band VCO utilizing tapped inductor presented in this chapter was implemented on silicon using 45-nm CMOS process of Texas Instruments. Fig. 3.29 shows a photograph of the chip that occupies an active area of $700\mu m \times 400\mu m$. The tapped inductor is placed in the middle of the chip. The switched capacitor banks and negative-$G_m$ stages for two bands are placed on each side of the inductor. Special care was taken in the physical design of the switched capacitor banks in order to preserve their $Q$-factor. The simulations presented in the previous subchapters include the layout parasitic components (capacitances and resistances) caused by the layout interconnects.

The test chip was fabricated on the Texas Instruments 45-nm CMOS process. It uses custom-made JTAG interface that controls the frequency tuning, the bias settings, and all relevant digital circuitry needed for proper operation of the VCO itself. Since the project with Texas Instruments finished before the chip measurement, and other unforeseen events, Texas Instruments did not provide a software and board to control their JTAG interface. Thus, the measurement and the verification of the presented design were not possible at TUT.

3.9. Summary and contributions

The development of the theoretical limitations posed by tapped-inductor dual-band VCO (Subchapters 3.2-3.5) was financially supported by the Academy of Finland (under Project no. 129077, “Hybrid Analog-Digital Signal Processing for Communications Transceivers”) and Tampere Graduate Programme in Information Science and Engineering (TISE). The development of design example on CMOS process was supported by Texas Instruments. Part of this development has been patented by Texas Instruments [76]. The theoretical investigations
3.9. Summary and contributions

presented in this chapter are published in the IEEE Transactions of Circuits and Systems – II [P.7]. The material from [P.7] is reused with the kind permission of IEEE, © 2012 IEEE.

The contributions of the work presented in this chapter are:

1. Proposed is a tapped inductor that replaces the four inductors used for building the fourth-order resonator, and thus the occupied silicon area is reduced. Furthermore, the implications involved with the design of the tapped fourth-order resonator are analyzed.

2. Proposed is an irregular inductor structure that fulfills the derived design recommendations.

3. Developed is a design example, which demonstrates the theoretical derivations for building a dual-band VCO based on tapped inductor. The design example covers the frequency bands of the WCDMA and the four GSM bands.
Chapter 4

A Wideband Low Phase-Noise LC-VCO with Programmable $K_{VCO}$

4.1. Introduction

The recent trend to integrate various communication standards in a handheld terminal demands the use of a wideband Voltage-Controlled Oscillator (VCO). The wideband VCO should support certain reprogramming capabilities to meet stringent phase noise requirements for certain standards, or to relax the performance and to save power in other standards. It is well known that phase noise performance of a wideband VCO is deteriorated by the large VCO Gain ($K_{VCO}$), which increases the noise sensitivity of the VCO [138]. Combined digital and analog tuning is a common way to achieve simultaneously a small VCO gain and to cover a large tuning range. However, in a wideband oscillator the VCO gain realized with a varactor varies significantly throughout the tuning range and needs to be adjusted. Programmable $K_{VCO}$ capabilities may also be used to cover the requirements of different communication standards.

Different methods have been introduced in [112], [125] and [166] to cope with nonlinear varactor characteristics and to achieve constant VCO gain. In [166], two varactor sections work in parallel with different control voltages to achieve a temperature independent tuning characteristic. A linear varactor characteristic is achieved in [125] and [112] using multiple identical varactor sections biased with different voltages. The linear characteristic provides less noise up-conversion [70] and equalizes the phase noise performance across the analog tuning range, but generally gives worse phase noise results and requires more current if compared to the conventional solution [112]. This chapter presents a reliable method to program the VCO gain according to the transceiver needs and the communication standard in use. The programmable $K_{VCO}$ concept can be applied to any differential VCO topology. An overview of other $K_{VCO}$ linearization techniques and comparison with state-of-the-art CMOS VCOs for is given in Subchapter 4.5.
CHAPTER 4: A WIDEBAND LOW PHASE-NOISE LC-VCO WITH PROGRAMMABLE KVCO

4.2. VCO topology and building blocks

4.2.1. Double-cross-coupled oscillator

The programmable $K_{VCO}$ scheme is implemented in a double cross-coupled topology shown in Fig. 4.1. The double cross-coupled oscillator utilizes two bias inductors ($L_{TOP}$ and $L_{BOT}$) that helps to reduce the power consumption for a given voltage swing [165], [166]. The central-tapped inductor $L_{MAIN}$ of 0.83-nH is optimized for high quality-factor at the frequency range of operation. The relatively small inductance allows using a capacitor bank with small $C_{max}/C_{min}$ ratio. The low-$Q$ inductors $L_{TOP}$ and $L_{BOT}$ provide high impedance for the switching NMOS and PMOS transistor pairs, which prevent quality factor degradation caused by the transistors entering the triode region [69]. The capacitor $C_{FILT}$ provides an ac-ground and filters out noise from the power supply and the regulator. The error amplifier and the regulating PMOS transistor form a bias control loop (BCL) that stabilize the bias point of the oscillator for varying supply voltage.

The following subchapters provides a detailed description of the VCO building blocks: the switched capacitor bank is described in 4.2.2, the bias-control loop and the error amplifier are described in 4.2.3, the power selection mode circuitry is given in 4.2.4, and finally the output buffer is demonstrated in 4.2.5.
4.2. VCO topology and building blocks

The capacitor $C_{TOT}$ in Fig. 4.1 represents the total capacitance of the resonance tank and comprises of a nine-bit coarse-tuned capacitor bank, a varactor block for continuous tuning, and parasitic capacitances. Fig. 4.2 shows the differential coarse-tuned capacitor structure used in the test chip, which provides low series resistance and maximizes the $C_{\text{max}}/C_{\text{min}}$ ratio [147]. The coarse-tuned high-$Q$ MIM capacitors are switched with large minimum-channel-length transistors resulting in $C_{\text{max}}/C_{\text{min}} \approx 2$.

4.2.3. Bias control loop and error amplifier

The error amplifier used in the bias control loop is shown in Fig. 4.3. A single-stage amplifier structure is chosen for its simplicity and robust operation. The gain of the error amplifier is achieved with an NMOS differential pair $M_1$-$M_2$ with active-load PMOS transistors $M_3$-$M_4$. The biasing of the error amplifier is realized with transistors $M_{B,1}$-$M_{B,4}$ and $R_B$. The biasing is slightly dependent on the power supply, but it was verified with simulations that the supply dependence is insignificant for the proper operation of the BCL. The error amplifier consumes at most 180 $\mu$A when $V_{DD} = 2.5$V, and less than 100 $\mu$A when $V_{DD} = 1.8$V, which is
only a small fraction of the current consumed by the VCO core. The 15-pF $C_{fb}$ capacitor provides frequency compensation of the amplifier to improve the system stability. The inverting amplifier input is connected to a reference $dc$ voltage, which is used for comparing the voltage from the inductor center-tap that is fed to the non-inverting amplifier input. The negative feedback stabilizes the bias point of the oscillator, since the $dc$ voltage on the central tap is proportional to the current injected into the oscillator core. The reference voltage $V_{REF}$ controls the amount of current fed to the cross-coupled pairs, which is also used for the power selection mode of the VCO.

The stability of the bias control loop is investigated using phase margin of the open-loop gain determined by the error amplifier, the regulating transistor $M_{REG}$, and the VCO core itself. Fig. 4.4(a) shows the test-bench utilized for simulating the open loop gain. The two cross-coupled pairs are replaced by a resistive divider $R’-R”$, and an auxiliary unity-gain block connects the center-tap of $L_{MAIN}$ to the error amplifier. The unity-gain block creates a negative feedback providing the necessary $dc$ operating point of the error amplifier and it has a very low bandwidth (BW ~ 1Hz). The negative feedback is effectively broken for frequencies above the 1-Hz bandwidth of the auxiliary block, which allows simulating the open-loop gain of the bias control loop. The open-loop gain of the system is defined as a small-signal gain from the inverting input of the amplifier to the node between $R’$ and $R”$. The identical resistors $R’$ and $R”$ model the operation of the two cross-coupled pairs, and their value is varied to investigate the stability of the bias control loop under different VCO currents. Another destabilizing factor is a varying power supply ($V_{DD}$), which also changes the system stability.
Fig. 4.4(b) shows the magnitude and phase of the system’s open-loop gain for two worst-case scenarios: 1) the highest loop gain under possible $V_{DD}$ and VCO current conditions, and 2) the lowest loop gain under possible $V_{DD}$ and VCO current conditions. The highest open-loop gain is reached with maximum $V_{DD}$ (=2.5V) and with minimum VCO current (=3mA). The smallest gain is achieved with minimum $V_{DD}$ (1.8V which provides enough headroom for $M_{REG}$ to function properly) and with maximum VCO current (=6mA). Increasing $V_{DD}$ injects more current into the error amplifier and creates more gain from the amplifier stage. On the other hand, small VCO current corresponds to big $R' + R''$, which increase the voltage gain produced by the PMOS regulating transistor ($g_{m,REG}(R' + R'')$). The highest-gain case has a phase margin of 58.2 degrees, and the lowest-gain case displays a phase margin of 65.4 degrees i.e. the good phase margin assures stability in all operating conditions.

The open-loop gain at low frequencies is between 42.3 dB and 49.4 dB depending on the power supply and on the VCO current. The contribution of the error amplifier to the total loop gain is 29.4 dB (32.5 dB), while the transistor $M_{REG}$ adds another 18.8 dB (20.9 dB) to the combined loop gain. The two 15-pF MOS capacitors assure the system stability. The loop gain diminishes for frequencies above few MHz, which means that a noise in the power supply line is attenuated within this bandwidth, thus providing a clean power supply to the test oscillator.

4.2.4. Power selection mode

The power-mode selection of the oscillator is realized by the circuit shown in Fig. 4.5. The power mode selection scales down the voltage reference $V_{REF}$ supplied to the error amplifier from an external reference voltage. The digital signal $LP$ (low power) selects whether the resistor divider $R_1$-$R_2$ is active or not. The transistor $M_{LP}$ is switched on and the CMOS transmission gate in parallel to $R_1$ is disabled when the low-power mode is selected ($LP = '1'$). The reference voltage supplied to the error amplifier is scaled down by a factor of 0.8 ($R_2/(R_1+R_2) = 0.8$) and the bias control loop injects less current into the oscillator. The nominal power mode is selected with $LP = '0'$ – $M_{LP}$ is turned off and the transmission gate is enabled,
which forces the external $V_{\text{REF}}$ to be applied directly to the input of the error amplifier. The functionality can be preserved even without the transmission gate, but the resistor $R_1$ would generate additional noise in the nominal power mode where the oscillator phase noise is critical.

The possibility to select different power modes addresses the issue for adaptive adjustment of the oscillator performance depending on the VCO phase noise requirement for the selected communication standard. The low-power mode can be enabled in applications where the VCO phase noise is not critical in order to save power. The low-power signal should be disabled in cases where the phase noise performance is critical.

More complex configuration of power selection using resistor dividers could be adopted to make the voltage swing constant throughout the oscillator tuning range by scaling $V_{\text{REF}}$. The coarse-tuning frequency-control-word can be used for switching on and off resistor sections in a binary fashion. A simple state machine powered up at the start-up can do the calibration, in a similar way as in [10].

The reference voltage $V_{\text{REF}}$ is supplied externally in order to allow easy testing, and nominally, $V_{\text{REF}}$ is equal to 0.8 V. $V_{\text{REF}}$ can be obtained from internal bandgap that is typically present in any integrated circuit. However, the internal reference voltage may generate significant noise, which will degrade the oscillator noise performance [165]. The bandgap noise could be filtered out with large off-chip capacitors, but this topic goes beyond the target of the test chip. The reference voltage is supplied externally with low-noise laboratory voltage source for increased testing flexibility and to avoid the described above noise issues.

The test oscillator was measured also in high-power mode with no additional hardware: the external voltage $V_{\text{REF}}$ is increased from 0.8 V up to 1.0 V. In both nominal-power and high-power mode, the digital signal $L_P$ is set to logical ‘0’. The VCO phase noise performance depending on the power mode is presented in 4.4.2.

### 4.2.5. Output buffer

The output buffer implemented on the test chip is shown in Fig. 4.6. The buffer is intended only for phase noise measurement, thus high input impedance and 50-Ω driving capabilities are required. In addition, the buffer should have low phase noise floor not to compromise the oscillator phase noise. An open-drain pseudo-differential structure is selected that is similar to the open-drain buffer described in subchapter 3.6.4. Compared to the buffer presented in 3.6.4, the single CMOS inverter is replaced by two CMOS inverters to reduce the resonator loading. The CMOS inverters produce almost square-waves at their outputs, which is further squared by the open-drain stage over the 50-Ω load (Fig. 4.7(a)). The node-voltages approach more a square wave when the buffer is driven with lower input frequency and with larger voltage
4.2. VCO topology and building blocks

Fig. 4.6. Open-drain buffer: (a) block diagram; (b) electrical schematic.

Fig. 4.7. Buffer operation with 1.5-Vpp sinusoidal input: (a) node-voltage waveforms with 4 GHz input frequency after the first \( v_{in1} \) and the second inverter \( v_{in2} \), and on the 50Ω load \( v_{out} \); (b) simulated buffer phase noise for 3, 4, and 5 GHz input frequency.

swing, both reducing the power consumption and buffer phase noise (Fig. 4.7(b)).

The two identical buffer sections consume less than 4.5 mA from 1.5-V power supply when driven with 5-GHz sinusoid with amplitude of 1.5 Vpp, and 3 mA when driven with 3-GHz sinusoid in similar condition. The buffer has a separate power supply pin for testing purposes and in order to separate its power consumption from the oscillator. The buffer phase noise is less than \(-150\) dBc/Hz at 1 MHz frequency offset for the entire VCO frequency range (Fig. 4.7(b)), which is 20 dB lower than the VCO phase noise and allows reliable measurement (the VCO phase noise performance is presented in Fig. 4.13).
4.3. **KVCO programmability**

The KVCO programmability of the test chip is realized by sectioning the analog tuning block, which uses PMOS accumulation mode varactor. The gates of the PMOS varactors are biased to ground through a resistor, thus avoiding any contribution of an additional biasing circuit to the phase noise and to the pushing figure. The varactor block in Fig. 4.8(b) comprises of three separate sections to realize the programmability. The first section is continuously controllable with $V_{A1}$ and alone provides the minimum VCO gain. The second section is equally sized to the first section and can be digitally switched on or off. When the second section is activated, $V_{A2}$ becomes equal to $V_{A1}$ and the first and the second section together achieve twice bigger tuning range, respectively a twice higher $K_{VCO}$. In a similar manner operates the third
4.4. Experimental results

Fig. 4.10. Phase Noise at 1MHz offset as a function of the VCO Gain setting measured at around 3.6-GHz and 4.0-GHz VCO frequency.

section, controlled by $V_{A3}$, which is twice smaller than the first two sections. Thus, a digitally programmable VCO gain is realized, which can be used for $K_{VCO}$ equalization across the frequency range. Fig. 4.8(a) shows the digital control of the varactor sections. When the second or the third section is not operational, the corresponding voltage $V_{A2}$ or $V_{A3}$ is grounded with an MOS switch ($M_{A2}-M_{A3}$), which brings the varactor CV curve to a flat region (point E in Fig. 4.9). Because of the flat CV curve, noise on the control voltage line, or common-mode noise from the oscillator do not up-convert into phase noise [70]. Thus, the VCO gain can be traded for better phase noise in applications where a large $K_{VCO}$ is not required. A flat CV curve could be obtained also for controlled voltages bigger than 1V, but this varactor region is not desired due to: 1) lower varactor Q-factor; 2) separate bias voltage would be needed, which would add noise and instabilities.

The phase noise dependence on the VCO gain is shown in Fig. 4.10 for two oscillation frequencies and different varactor settings. The points A-D are the steepest points from the varactor tuning curve shown in Fig. 4.9. The VCO phase noise goes down with small VCO gain, and at least 2dB lower VCO phase noise can be obtained in scenarios where smaller VCO gain can be used. With control voltage being zero, the measured phase noise was independent from the VCO gain setting because of the flat tuning curve, with phase noise of -128.0 and -127.2 dBc/Hz at 1-MHz offset from 3.6-GHz and 4.0-GHz carriers respectively.

4.4. Experimental results

The measured VCO gain programmability and its effect on the VCO phase noise are presented in Fig. 4.9 and Fig. 4.10 for proving the programmable $K_{VCO}$ concept. This subchapter presents test-chip details and supplementary measurement results.
4.4.1. Test-chip and measurement setup

The test chip was fabricated on a standard 130-nm CMOS technology with six metal layers. The chip was measured using on-wafer probing for the RF output signals. The power supply and the other low-frequency control signals were supplied through bonding wires. A signal source analyzer (HP4352S) was used for the phase noise measurement. The VCO was followed by an external frequency divider-by-2 for the measurement, and the 6-dB gain from the divider is taken into account in the phase noise. The VCO and the regulator consume 6mA or less from a 1.8-V power supply across the tuning range. A photograph of the VCO chip is shown in Fig. 4.11. The active VCO area is 700\(\mu\text{m} \times 400\mu\text{m}\).

Fig. 4.12(a) shows the measured VCO frequency range as a function of the coarse-tuning frequency-control-word (FCW), and Fig. 4.12(b) shows the respective VCO current consumption for the different power modes. The VCO oscillation frequency is almost independent from the power mode, as the voltage-dependent transistor parasitic capacitances are significantly smaller than the switched capacitors. The lowest oscillation frequency is achieved when all course-tuned are switched-on with FCW = 511, and the highest frequency is
4.4. Experimental results

Fig. 4.13. Measured VCO Phase Noise for two VCO central frequencies

achieved with FCW = 0. The resonance tank impedance is the smallest with FCW = 511, which requires more bias current to achieve the desired amplitude. The VCO consumes at most 6 mA in nominal power mode (including the error amplifier). The VCO current consumption nearly doubles at high-power mode, or it gets approximately 30% less in low-power mode.

4.4.2. VCO phase noise performance

The measured phase noise is shown in Fig. 4.13 for two VCO frequencies (~ 3.6 GHz and ~ 4.0 GHz). The frequency range from 3.6 GHz to 4.0 GHz corresponds to the frequency range of the quad-band GSM standard before frequency division by 4 and frequency division by 2. The measured VCO phase noise in the 3.6–4.0 GHz frequency range is bounded by the two curves presented above. The best VCO phase noise is measured at the lowest VCO frequency ($L = –127.5$ dBc/Hz @ 1MHz offset; $f_{osc} = 3.31$ GHz), and the worst phase noise is measured at the highest VCO frequency ($L = –120.7$ dBc/Hz @ 1MHz offset; $f_{osc} = 4.83$ GHz).

Fig. 4.14 shows the VCO phase noise at two oscillation frequencies depending on the selected power mode. Both the flicker noise and the white noise are high in low-power mode, but the power consumption is reduced. When injecting more current in the high-power mode, the far-away phase noise improves with few dB compared to the nominal-power mode, while the close-in phase noise remains almost constant.
4.4.3. Pushing figure

Fig. 4.15 shows the measured voltage supply ($V_{DD,OSC}$), which is stabilized by the bias control loop with $V_{DD}$ varying from 1.6 V up to 2.4 V. This measurement was possible since the test chip provides an access point between the regulating transistor $M_{REG}$ and the $L_{TOP}C_{FILT}$ filter shown in Fig. 4.1. In addition, this external connection makes it possible to measure directly the VCO phase noise performance without the BCL. Fig. 4.15 shows that the BCL makes the oscillator local supply stable for voltages above 1.7 V, which provides around 200 mV voltage headroom for the transistor $M_{REG}$. The local stabilized power supply ($V_{DD,OSC}$) slightly depends on the VCO oscillation frequency and it varies within a 30-mV range from the lowest to the highest oscillation frequency. The slope of the stabilized voltage is due to the finite gain of the error amplifier and the channel length modulation of the regulating transistor $M_{REG}$.

Fig. 4.16 shows the measured VCO frequency and the corresponding pushing figure with and without BCL than confirms a proper supply regulation. The unregulated VCO frequency goes down when the local power supply is raised due to the larger voltage swing and increased supply current going through the oscillator core. The VCO frequency gets stabilized as soon as
4.4. Experimental results

Fig. 4.16. (a) Measured VCO frequency with and without BCL; (b) VCO pushing figure with and without BCL.

the BCL provides a stable local power supply for the oscillator with $V_{DD}$ above 1.7 V (the stabilization of the BCL is shown in Fig. 4.15). The effect of the BCL voltage stabilization is seen in the pushing figure, which drops from -30 MHz/V down to -0.70 MHz/V, thus making the VCO frequency insensitive to power supply variations. Since the voltage stabilization is not perfect due to the finite gain of the error amplifier, the pushing figure does not go to zero.

Fig. 4.17 shows the measured VCO frequency pushing across the tuning range: Fig. 4.17(a) showing the pushing at the lowest oscillation frequency, and Fig. 4.17(d) showing the pushing

Fig. 4.17. Pushing figure across the VCO tuning range: (a) FCW=511 ($f_{osc} \sim 3.30$ GHz); (b) FCW=255 ($f_{osc} \sim 3.82$ GHz); (c) FCW=127 ($f_{osc} \sim 4.22$ GHz); (d) FCW=0 ($f_{osc} \sim 4.75$ GHz).
at the highest oscillation frequency. The switched capacitor bank is completely on with FCW = 511 introducing large voltage-independent capacitor into the resonance tank that shadows the voltage-dependent parasitic capacitors of the cross-coupled pairs, thus resulting in very small deviation of the oscillation frequency. Similarly, the switched capacitor bank is completely off with FCW = 0 making the voltage-dependent parasitic capacitors having a great influence on the oscillation frequency, respectively on the frequency pushing. Nevertheless, the VCO pushing figure does not exceed 1 MHz/V in its worst case thanks to the voltage stabilization provided by the BCL.

4.4.4. VCO gain variation depending on the power mode

Fig. 4.18(a) shows a comparison of the analog tuning range achieved in different power modes, and Fig. 4.18(b) shows the corresponding VCO gain. The large amplitude over the resonance tank averages the varactor capacitance, thus making the achievable tuning range smaller [70], [97]. The averaging effect reduces the VCO gain, which should be compensated in the design phase by placing a bigger varactor. On the other hand, the increased VCO gain in low-power mode contributes to higher noise up-conversion (Fig. 4.18(b)). Thus, the phase noise performance of the VCO in low-power mode is first governed by the smaller voltage swing over the resonator, and second by the increased noise conversion, and this effect is clearly seen from Fig. 4.14.

The proposed here programmable VCO gain helps to achieve a constant VCO gain over large frequency range using robust digital control. The same varactor control can be used to adjust the needed VCO gain when the VCO power mode is switched from nominal to low-power, or vise versa.

![Fig. 4.18. VCO gain variation for the different power modes: (a) analog tuning range; (b) corresponding VCO gain.](image-url)
4.5. Comparison with state-of-art CMOS VCOs

Table 4-I: Comparison with the state-of-the-art Low-Noise Wideband CMOS VCOs

<table>
<thead>
<tr>
<th>Ref</th>
<th>Year</th>
<th>Frequency (GHz)</th>
<th>%</th>
<th>Pdc (mW)</th>
<th>Phase Noise (dBc/Hz)</th>
<th>FOM</th>
<th>PFTN</th>
<th>LIN / TEMP / PROGRAMM</th>
</tr>
</thead>
<tbody>
<tr>
<td>[109]</td>
<td>2004</td>
<td>2.80 – 4.55</td>
<td>47.6</td>
<td>27</td>
<td>-142.0 @ 3MHz*</td>
<td>-183.3</td>
<td>3.2</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[165]</td>
<td>2004</td>
<td>1.46 – 1.81</td>
<td>21.4</td>
<td>10</td>
<td>-134.0 @ 900kHz</td>
<td>-189.8</td>
<td>2.0</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[10]</td>
<td>2005</td>
<td>1.14 – 2.46</td>
<td>73.3</td>
<td>8.1</td>
<td>-109.0 @ 100kHz</td>
<td>-181.1</td>
<td>8.5</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[148]</td>
<td>2006</td>
<td>1.75 – 2.12</td>
<td>19.0</td>
<td>2.25</td>
<td>-120.0 @ 600kHz</td>
<td>-185.8</td>
<td>-1.6</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[93]</td>
<td>2008</td>
<td>4.63 – 6.00</td>
<td>26.4</td>
<td>1.80</td>
<td>-124.8 @ 1MHz</td>
<td>-196.2</td>
<td>11.2</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[110]</td>
<td>2008</td>
<td>4.90 – 5.65</td>
<td>14.2</td>
<td>1.40</td>
<td>-132.9 @ 3MHz</td>
<td>-195.7</td>
<td>5.57</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[132]</td>
<td>2009</td>
<td>2.15 – 2.62</td>
<td>19.7</td>
<td>0.365</td>
<td>-117.3 @ 1MHz</td>
<td>-190.0</td>
<td>1.29</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[163]</td>
<td>2009</td>
<td>2.93 – 3.62</td>
<td>21.1</td>
<td>1.65</td>
<td>-122.0 @ 1MHz</td>
<td>-191.0</td>
<td>2.77</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[78]</td>
<td>2010</td>
<td>3.39 – 4.16</td>
<td>20.4</td>
<td>0.225</td>
<td>-116.9 @ 1MHz</td>
<td>-194.4</td>
<td>7.26</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[151]</td>
<td>2010</td>
<td>3.03 – 3.67</td>
<td>19.1</td>
<td>18.48</td>
<td>-114.7 @ 400kHz</td>
<td>-180.8</td>
<td>-7.7</td>
<td>n / n / n</td>
</tr>
<tr>
<td>[125]</td>
<td>2002</td>
<td>2.25 – 2.50</td>
<td>10.5</td>
<td>11.25</td>
<td>-129.0 @ 3MHz</td>
<td>-176.6</td>
<td>-16.9</td>
<td>y / y / n</td>
</tr>
<tr>
<td>[112]</td>
<td>2004</td>
<td>2.36 – 2.46</td>
<td>4.4</td>
<td>3.2</td>
<td>-126.0 @ 3MHz</td>
<td>-179.0</td>
<td>-22.0</td>
<td>y / n / n</td>
</tr>
<tr>
<td>[166]</td>
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<td>1.55 – 1.95</td>
<td>22.9</td>
<td>16.25</td>
<td>-134.0 @ 900kHz</td>
<td>-187.4</td>
<td>1.0</td>
<td>n / y / n</td>
</tr>
<tr>
<td>[68]</td>
<td>2007</td>
<td>3.10 – 5.20</td>
<td>50.6</td>
<td>9.22</td>
<td>-119.0 @ 1MHz</td>
<td>-179.3</td>
<td>2.0</td>
<td>n / n / y</td>
</tr>
<tr>
<td>[79]</td>
<td>2007</td>
<td>5.72 – 6.02</td>
<td>5.1</td>
<td>12.5</td>
<td>-115.0 @ 1MHz</td>
<td>-179.6</td>
<td>-20.3</td>
<td>y / y / y</td>
</tr>
<tr>
<td>[84]</td>
<td>2008</td>
<td>0.92 – 1.85</td>
<td>66.8</td>
<td>10.8</td>
<td>-127.1 @ 1MHz</td>
<td>-181.6</td>
<td>2.3</td>
<td>y / y / y</td>
</tr>
<tr>
<td>[167]</td>
<td>2009</td>
<td>3.10 – 4.20</td>
<td>30.1</td>
<td>12.0</td>
<td>-110.6 @ 1MHz</td>
<td>-172.3</td>
<td>-13.2</td>
<td>y / n / n</td>
</tr>
<tr>
<td>[2]</td>
<td>2010</td>
<td>10.68 – 12.40</td>
<td>14.9</td>
<td>48.3</td>
<td>-103.9 @ 1MHz</td>
<td>-168.8</td>
<td>-22.1</td>
<td>n / y / n</td>
</tr>
<tr>
<td>This work</td>
<td>2007</td>
<td>3.31 – 4.83</td>
<td>37.3</td>
<td>10.5</td>
<td>-127.5 @ 1MHz</td>
<td>-187.7</td>
<td>7.1</td>
<td>n / n / y</td>
</tr>
</tbody>
</table>

* - from 1.8GHz carrier

Table 4-I summarizes the performance of the presented VCO and compares it with the state-of-the-art CMOS VCOs. The table is an expanded version of the one presented in [P.2] and it is separated in two parts. The upper part of the table lists state-of-art wideband CMOS VCOs in the frequency range of 1–6 GHz, while the lower part of the table includes the performance of VCOs having linearized $K_{\text{VCO}}$, temperature compensated $K_{\text{VCO}}$, or $K_{\text{VCO}}$ programmability. High-performance VCOs based on higher-order resonators are summarized in Subchapter 1.4.6. The last column of Table 4-I flags the circuit solution used for influencing the $K_{\text{VCO}}$. In order to make fair comparison, the commonly used Figure-of-Merit (1.2) and the Power-Frequency-Tuning-Normalized (1.3) introduced in [67] is used. Since the tuning range can be traded for phase noise performance, observing these two figures makes clearer view of how balanced the VCO is in terms of the two parameters.

The table above demonstrate that excellent FoM (>185) and PFTN (>0) has been achieved in recent years by wideband CMOS VCOs, but these extreme performance metrics are usually achieved in low supply voltages combined with some technique for phase noise reduction. However, the absolute numbers for phase noise are not as impressive as their FoM or PFTN, and thus they may not necessarily meet the practical transceiver requirements. It is indicative
that the VCOs employing certain $K_{\text{VCO}}$ linearization or programmability technique have visible lower performance metrics because of the extra losses and noise contributed by the additional circuitry. Above all, circuit solutions that address linearized tuning range suffer the most, which is mainly due to additional biasing and resistive network needed to build the distributed biasing.

Table 4-I shows that the work presented here achieves very low phase noise for its wide tuning range. In addition, the VCO has balanced FoM and PFTN performance despite the programming $K_{\text{VCO}}$ capabilities offered by the additional circuitry. The performance of the reported VCO is competitive with the latest VCO developments.

4.5.1. Latest development of $K_{\text{VCO}}$ programmability and linearization

After [P.2] was published, the topic of varactor linearity enhancement and VCO Gain programmability continued to be an interesting research topic. The goal of this subchapter is to summarize the latest development related to the work presented above.

The varactor linearization have continued to develop the idea to superimpose varactor CV curves with shifted bias [112] in order to obtain a linear varactor characteristic over certain voltage range. In [66] is proposed a method for calculating the bias voltage and the sizes of the varactor section to obtain truly-linear analog tuning. Instead of using different bias voltage for each varactor section, in [87] the control voltage applied to the varactor sections is shifted by an MOS diode, thus the control voltage for each varactor section is lower by approximately the MOS threshold voltage. References [108] and [152] propose voltage level shifters instead of the diode-shifting solution. In [19] is proposed a variation of the distributed bias idea, where the varactor sections are softly switched. A practical solution requiring no additional hardware is proposed in [34], where transistors having different threshold voltages are employed as varactors with shifted CV curves. Some CMOS processes offer those transistors without additional cost and this solution is virtually free, although perfect linearization with two sections is difficult to realize.

A $K_{\text{VCO}}$ suppression technique is proposed in [117] along the wide frequency tuning range of a VCO. The $K_{\text{VCO}}$ suppression technique relies on a secondary magnetically-coupled coil in series with a bank of switched capacitors in an arrangement providing frequency tuning with opposite polarity. The proposed technique falls in the category of the programmable $K_{\text{VCO}}$ since the secondary capacitor bank is controlled digitally with the same control bus as the main capacitor bank. Similar idea to [P.2] is presented in [1] with varactor sections directly controlled by the coarse-tuning bits. The varactor sections are connected to a dedicated bias voltage ([P.2] uses ground) when they are deactivated, which introduces additional noise, biases the varactors in the middle of the analog tuning range, and thus increase the oscillator phase noise. The
above-mentioned problem is solved in [68] by biasing the inactive section to ground or the power supply (similar to [P.2]). In [79] the varactor programmability is combined with varactor linearization using superposition that results in nine controllable varactor sections. Similar idea for achieving constant $K_{VCO}$ is presented in [27] where a differential varactor configuration is used in the basic cell to reduce the AM-PM conversion. Reference [84] goes even further in the $K_{VCO}$ programmability by implementing the approach in [P.2] in addition to the pseudo-exponential coarse-tuned capacitor bank. The pseudo-exponential capacitor bank uses non-binary-weighting for the coarse capacitor to achieve linear VCO tuning. In [104] the non-binary-weighted approach is applied also for sizing the varactor sections. Varactor programmability targeted to minimizes the frequency drift cause by temperature effects and process corners in demonstrated in [2].

4.6. Summary and contributions

The presented in this chapter was published in the IEEE Wireless and Communication Letters [P.2], and it was referred by other IEEE journal and conferences proceeding (18 citations according to Scopus by March 2012). The material from [P.2] is reused with the kind permission of IEEE, © 2007 IEEE. The work was financially supported by Infineon Technologies AG. The VCO presented here was integrated by Infineon Technologies into their WCDMA transceiver ([173], [174]).

The contributions of the work presented in this chapter are:

1. Introduced is a programmable $K_{VCO}$ concept, which can be used to trade phase-noise performance with analog tuning range. The concept is applicable to equalize the $K_{VCO}$ along the entire tuning range of a VCO.

2. The proposed programmable $K_{VCO}$ concept has found number of implementations among the academic and industrial community. Furthermore, the performance of the demonstrated VCO is referred as a state-of-art by the latest publications in the field.
Chapter 5
Time-Varying Root-Locus of Large-Signal LC Oscillators

5.1. Introduction

The development of large-voltage-swing state-of-art oscillators necessitates continuous improvement of methods for their analysis. An overview of the different methods for oscillator phase-noise analysis is presented in Subchapter 1.5.1–1.5.4. The standard application of the root-locus methods including its large-signal variations is summarized in Subchapter 1.5.5.

This chapter presents a Time-Varying Root-Locus (TVRL) approach for a steady-state analysis of large-signal LC oscillators. The proposed TVRL is a Semi-Symbolic CAD algorithm, which analyzes the entire oscillator architecture and requires neither circuit simplifications [5], [6], [7], [21], [50], [51], [69], nor feedback-loop-breaking operations [122], [123]. It uses the numerical SpectreRF Periodic Steady-State (PSS) method to obtain the time instants for computing the roots. The nodal matrix for each time instant is formed with only the complex frequency $s$ as a symbol, and the roots are computed with the QZ-method to analyze the sub-period oscillator behavior. The TVRL analysis is demonstrated on GHz-range cross-coupled oscillator, which helps analyzing phase noise improvement in circuit design and confirmed by SpectreRF on a 130-nm CMOS process.

5.2. Time-Varying Root-Locus Algorithm

The Time-Varying Root-Locus computes the roots trajectories for one oscillation period ($T_0$). The obtained trajectories are used for analysis of the large-signal oscillator behavior. Fig. 5.1 shows the CAD algorithm developed for the root computation, which is based on:

1. Circuit Periodic Steady-State (PSS) analysis – the SpectreRF PSS analysis is used to obtain the steady-state solution of the circuit within the oscillation period. The use of SpectreRF guarantees precise results of the complete and complex oscillator topologies with foundry-dependent model parameters. A comprehensive review on the different PSS
methods can be found in [119]. The PSS shooting method is used in this work with options: \( \text{harms}=5, \text{errpreset}=\text{moderate}, \text{maxstep}=2\text{ps}, \text{steadyratio}=0.2, \text{method}=\text{gear2only} \). The circuit node-voltages obtained from the PSS analysis are saved for the next step of the algorithm. In addition, the oscillator phase noise is computed with SpectreRF for further investigations.

2. **Linearization of Active Devices** – an active-device linearization is performed with Spectre simulator based on the PSS node voltages saved in the previous step. The linearization is done for each active device using DC operating point analysis. The small-signal transistor parameters are stored for composing the admittance matrix of the circuit (Section 5.3.2).

3. **Normalization** – Impedance and frequency scaling is performed for all active and passive components in order to reduce eventual large spread of component values. The component scaling may become essential for improving the accuracy of the root computation in case of large-size and high-\(Q\) circuits (Section 5.3.3).

4. **\(Y\)-matrix formation** – the admittance matrix used for the root computation is created in the form of \(Y(s) = G + sB\) for the consequent QZ computation.

5. **Root computation** – the time-varying roots are computed for all PSS data points within the oscillation period. The root computation is based on QZ method, which operates on the \(G\) and \(B\) matrices (Section 5.3.4).

6. **Error estimate of the computed roots** – an optional step estimating the precision of the obtained roots. The precision evaluation is based on the condition number associated with the computed roots (Section 5.3.5).
5.3. Obtaining TVRL for LC oscillators

5.3.1. Oscillator topology

The TVRL method described here is applied for analyzing the large-signal LC oscillator behavior. Commonly used oscillator topologies in the GHz-range frequencies are based on cross-coupled pairs and LC-resonance tank. Fig. 5.2 shows modifications of double cross-coupled oscillators, abbreviated here as 1L-oscillator (Fig. 5.2(a)) and 1L+2bL oscillator (Fig. 5.2(b)). The double cross-coupled topology consumes approximately two times lower bias current compared to the single cross-coupled topology [7], [63], but it requires higher voltage headroom. The topology using the bias inductors (Fig. 5.2(b)) displays enhanced phase noise performances by exploiting noise-filtering phenomenon and $Q$-factor preservation [69].

The same analysis can be extended for other LC oscillator architectures without modifying the TVRL algorithm.

5.3.2. Component modeling and matrix formation

5.3.2.1. Inductor model

Nodal Analysis is preferred circuit description for CAD simulators of electronic circuits [160], which involves the formation of admittance matrix of the circuit. The presence of complex variable $s$ in the denominator of the matrix elements should be avoided [160]. For example, inductors have $s$ in their admittance denominator, and thus they have to be converted to a type of component, which has $s$ in the nominator. The widely popular Modified-Nodal Analysis (MNA) provides a stamp for including the inductors in the B-matrix and the $1/s$ term is avoided [160] at the expense of increased matrix size. Similarly, the inductors can be replaced by capacitors using a gyrator model [3], which could provide additional degree of


5.3.2.2. MOS transistor model

Due to the nonlinear and time-varying nature of the parameters of the MOS transistors and the corresponding small-signal models, the oscillator $Y$-matrix needs to be formed at each time instant. For achieving precise results, a small-signal model able to represent accurately the MOS behavior in all regions should be used for the root computation. Fig. 5.3 shows the utilized complete quasi-static MOS small-signal model with its model components connected between the transistor terminals [156]. The model in Fig. 5.3 represents the operation of the transistor in all three regions through different values of the model components. For instance, the cutoff region is characterized with $\{g_m \approx 0; g_{ds} \approx 0\}$, the triode region with $\{g_m \approx 0; g_{ds} \gg 0\}$, and the active region with $\{g_m > 0; g_{ds} > 0\}$. The numerical values of the small-signal model components are computed for each time instant, and for each nonlinear device based on the oscillator node voltages applied on the MOS transistor terminals. The utilized model accurately predicts the MOS transistor behavior in the frequency range of oscillator, since it is valid up to $f_T/3$, where $f_T$ is the transistor transit frequency [156]. The parasitic gate/source/drain resistances of the MOS transistor can also be included in the model in Fig. 5.3 in cases where their influence is critical for the oscillator operation. The MOS model expansion does not modify the presented algorithm.

Steady-state oscillations are in general reached when the injected and dissipated energy are in equilibrium. Typically, in large-signal oscillators the active transistors’ operating points travel between the cutoff, the active, and the triode region: energy is injected when they are in active region, and energy is dissipated otherwise. Although the transistors do not necessarily go through all regions of operation, their modeling in all regions represents a more general case for
5.3. Obtaining TVRL for LC oscillators

Fig. 5.4. (a) 1L+2bL oscillator node voltages and (b) drain currents of $M_{n2}$ and $M_{p2}$ for one oscillation period, including the corresponding values of the transistors’ $g_m$ and $g_{ds}$.

Fig. 5.5. (a) $M_{n2}$ time-varying operating point for the 1L+2bL oscillator; (b) $M_{p2}$ time-varying operating point for the 1L+2bL oscillator.

oscillators. Fig. 5.4(a) shows the node voltages generated by the 1L+2bL oscillator with denoted time instants A-H, while Fig. 5.4(b) shows the drain currents of transistors $M_{n2}$ and $M_{p2}$ with the corresponding small-signal parameters for instants C, E, and G. Fig. 5.4 confirms that the active transistors spend a big fraction of $T_0$ in nonlinear region, which is even more prolonged for larger voltages.

In Fig. 5.5(a) is visualized the operating point trajectory of the NMOS transistor $M_{n2}$ corresponding to the oscillator node voltages (Fig. 5.4) generated by the 1L+2bL oscillator. The operating point trajectory of the NMOS transistor $M_{p2}$ is shown in Fig. 5.5(b). The time instants C and G correspond to the cutoff and the triode regions of the transistor i.e. at instant C the transistor $M_{n2}$ operates in triode region, whereas $M_{p2}$ is in cutoff region [64]. In addition, the transistor operating-point trajectories are different for the rising (H-A-B) and for the falling part (D-E-F) of the waveform, which is due to the asymmetry of the $v_{TOP}$ and $v_{BOT}$ node voltage with respect to $v_{outR}$ and $v_{outL}$.

5.3.2.3. Matrix formation

The circuit matrices $G$ and $B$ are formed using the small-signal equivalent circuit of the oscillator. The MOS transistors are replaced with their time-varying quasi-static models, and the
inductors are replaced with their on-chip equivalent π-type circuit. The finite Q-factor of the capacitors in the LC-tank $C_{\omega 1}$ and $C_{\omega 2}$ is modeled with series resistors $r_{\omega 1}$ and $r_{\omega 2}$.

5.3.3. Impedance and Frequency normalization

Frequency and impedance normalization is performed to all circuit components and time-varying model parameters [159] in order to reduce the numerical errors, which could be caused by a large spread of component values:

\[ G_s = G \cdot R_{\text{norm}} \]  \hspace{1cm} (5.1)
\[ L_s = L \cdot \frac{2\pi f_{\text{norm}}}{R_{\text{norm}}} \]  \hspace{1cm} (5.2)
\[ C_s = C \cdot \left(2\pi f_{\text{norm}} \cdot R_{\text{norm}}\right) \]  \hspace{1cm} (5.3)

The normalization frequency $f_{\text{norm}}$ scales all components of $B$, and varying $f_{\text{norm}}$ keeps the components value spread unchanged. The normalization resistance $R_{\text{norm}}$ has the similar effect on G. However, a possible spread decrease in B can be achieved by using $R_{\text{norm}}$ due to the opposite scaling of inductors and capacitors (5.2)-(5.3). The spread of $G$ and $B$ are considered separately, because the two matrices are separately balanced during the QZ computation [4]. A dynamic impedance normalization using optimum $R_{\text{norm}}$ allows performing the TVRL computations with high accuracy and it is explained in Subchapter 5.3.5.

5.3.4. Root computation and root trajectories

The circuit poles are the roots of the characteristic equation $\det(Y(s)) = \det(G + s \cdot B(s)) = 0$, where the circuit matrix $Y(s)$ in our case is obtained by MNA. A positive real root, or positive real part of complex-conjugated root, defines exponentially growing signals in time, whereas negative real poles define exponentially decaying signals in time domain. A review of various methods for computing the roots of the characteristic equation is given in [65], [160]. Briefly

![Fig. 5.6.](image)

(a) Time-varying Root Locus for all roots of the 1L+2bL oscillator (the most negative roots are not shown). The main root is designated with $\lambda_0$; (b) the main time-varying complex-conjugated root
the approaches are: 1) to transform the circuit characteristic equation into a polynomial and to find its roots; 2) to apply matrix methods (direct or iterative) on the circuit matrices \( G \) and \( B \), where the \( G \)-matrix represents the frequency-independent components and \( B \)-matrix represents the frequency dependent ones. The computation algorithm used in this work is a direct QZ matrix method from MATLAB / LAPACK operating on \( G \) and \( B \) to obtain [4], [160]

\[
\lambda_i = \frac{S_{i,i}}{T_{i,i}},
\]

(5.4)

where \( \lambda_i \) is the \( i \)th circuit root / eigenvalue, while \( S \) and \( T \) are quasi-triangular matrices formed by the QZ algorithm [4] such that \( Q \cdot G \cdot Z = S \), \( Q \cdot B \cdot Z = T \), where \( Q \) and \( Z \) are unitary matrices.

The Time-Varying Root Locus is obtained following the procedure sequence outlined in Fig. 5.1 for the 1L+2bL oscillator. The resulting TVRL shown in Fig. 5.6 has 16 roots, few of them forming complex-conjugated pairs. However, only one complex-conjugated pair (\( \lambda_0 \)) crosses to the imaginary axis and travels between the positive and the negative part of the complex plane (Fig. 5.6(a)). This particular root (\( \lambda_0 \)) is in fact the root whose frequency matches closely the main harmonic of the generated signal (\( f_{osc} = 4.21 \) GHz) obtained by the PSS analysis and shown on Fig. 5.6(b). The rest of the complex-conjugated pairs are situated far from imaginary axis (Fig. 5.6(a)) in the LHP. All real roots of the oscillator are negative, which corresponds to the nearly sinusoidal operation and absence of relaxation or triggering phenomena, which are typical for multivibrators [21], [50], [51]. The \( \lambda_0 \) trajectory goes twice per period in the RHP and the LHP, which corresponds to the process of energy injection and energy dissipation. Similar process was observed in multivibrators [51], where \( \lambda_0 \) was called a “breathing” root.

### 5.3.5. Error estimation for the root computation

The impact of the impedance and frequency scaling on the root precision can be evaluated using the condition number \( \kappa \) associated with the computed roots, where small \( \kappa \) indicates a small numerical error [36]. The reciprocal condition number (\( \kappa_0^{-1} \)) associated with the main pole \( \lambda_0 \) is calculated as [4]

\[
\kappa_0^{-1} = \frac{\sqrt{|y_0^H \cdot G \cdot x_0|^2 + |y_0^H \cdot B \cdot x_0|^2}}{||x_0||_2 \cdot ||y_0||_2}
\]

(5.5)

where \( x_0 \) and \( y_0 \) are the left and right eigenvectors corresponding to the main pole \( \lambda_0 \), and \( ||(\cdot)||_2 \) is the two-norm of the two eigenvectors.
Fig. 5.7. (a) Time-varying condition number associated with the main root as a function of the normalization impedance $R_{\text{norm}}$; (b) optimum time-varying normalization impedance $R_{\text{norm, opt}}$ for the 1L+2bL oscillator.

Fig. 5.8. TVRL of the two oscillators operating with voltage swing of 1.0V: (a) oscillator’s output voltage ($\text{out}_L$) and $\text{Re}(\lambda_0(t))$ for the oscillation period; (b) trajectories of $\lambda_0(t)$ on the complex plane.

The precision of the calculated roots could be improved via appropriate impedance scaling as described in Section 5.3.3. Fig. 5.7(a) shows family of curves with the time-varying condition number $\kappa_0(t)$ (5.5) as a function of the scaling impedance $R_{\text{norm}}$. The minima of $\kappa_0(t)$ indicate the optimum normalization impedance $R_{\text{norm, opt}}$, which should be used to compute the roots at given time instant. Fig. 5.7b shows the variation of the optimum normalization impedance along the oscillation period, which is in the range of 20-30$\Omega$ when computing the main complex-conjugated root. The relatively small condition number indicates a high precision in the computations, given that the matrices $G$ and $B$ give an exact representation of the test oscillator.

An iterative normalization finds the optimum $R_{\text{norm}}$ for a given circuit topology and specific time instances. For the particular oscillator under test, the range of $R_{\text{norm, opt}}$ is narrow and it may slightly vary with oscillator voltage swing, thus a fixed $R_{\text{norm}}$ could be used in order to decrease the amount of computations required. In addition, as Fig. 5.7(a) suggests, using sub-optimum $R_{\text{norm}}$, even a decade away from the optimum value, would still result in good root precision. With this reasoning, a constant $R_{\text{norm}} = 20\Omega$, which is slightly different from $R_{\text{norm, opt}}$, has been used to obtain the results presented below. It was experimentally verified the selection of $R_{\text{norm}} = 20\Omega$ no practical influence on the precision of the obtained results.
5.4. Oscillators comparative analysis using TVRL

5.4.1. Oscillator modification comparison

The $\lambda_0$ trajectories for the two oscillator modifications (Fig. 5.2) are plotted in Fig. 5.8 for voltage swing of 1.0 V. The figure shows the resonator voltage ($v_{\text{outL}}$), the real part of $\lambda_0$ with denoted instants of the zero-crossing (‘A’) and the maximum of the voltage swing (‘C’). The behavior of the oscillators can be compared using the $\lambda_0$ trajectories, and in this example, the different trajectories allow to evaluate the effect of the bias inductors on the oscillator performance.

More insights into the two $\lambda_0$ trajectories are gained by simplifying the two oscillators: replacing $M_{n1}$ and $M_{p2}$ with a variable conductance $g_{ds}$, neglecting $M_{n2}$ and $M_{p1}$, and assuming ideal LC tanks (Fig. 5.9(a) and Fig. 5.9(b)). This scenario approximates large-signal condition with $M_{n1}$ and $M_{p2}$ operating in triode region, while $M_{n2}$ and $M_{p1}$ operating in cutoff region. The resulting root-loci with swept $g_{ds}$ are shown in Fig. 5.9(c). Big $g_{ds}$ in the 1L oscillator shortens one of the tank capacitor $2C_O$ forcing $\lambda_0$ to approach $f_0/\sqrt{2}$ (0.707$f_0$). As $g_{ds}$ increases in 1L+2bL oscillator, part of $2C_O$ gets connected to the $L_{\text{BOT}}C_{\text{BOT}}$ tank, while part of the other capacitor $2C_O$ gets connected to the $L_{\text{TOP}}C_{\text{TOP}}$ tank. Thus, the imaginary parts of the roots, originally placed at $f_{\text{BOT}}$ and $f_{\text{TOP}}$ frequency with $g_{ds}$=0, are decreasing. The “vanishing” part of the tank capacitance forces $\lambda_0$ to approach $f_{\text{H}}$, while the other two roots approaches $f_L$ and the origin, where $f_{\text{H}}$ and $f_L$ are root frequencies of the 1L+2bL oscillator obtained with $g_{ds}=\infty$. Since $f_{\text{H}}>f_0$, the bias inductors cause an increase in Im($\lambda_0$) when the 1L+2bL oscillator enters non-linear operation, which is opposite to the behavior of the 1L oscillator. The idealized $\lambda_0$ trajectories explain the roots behavior in Fig. 5.8 as they enter deeper in the LHP and the large-
signal assumptions are valid. The extreme $\lambda_0$ cases for both oscillators ($0.707f_0$ and $f_{H}$) are obtained with large $g_{ds}$ and they cannot be reached in practice.

The real part of the main root $\text{Re}(\lambda_0(t))$ for both oscillators has a maximum at the zero-crossing of the oscillators’ node voltages corresponding to the largest negative conductance generated by the cross-coupled pairs (‘A’). The minima of $\text{Re}(\lambda_0(t))$ corresponds to the extrema of the resonator voltages (‘C’), where one of the cross-coupled transistors is in cutoff region and the other one is in triode region. The transistors’ $g_m$ at ‘C’ is negligible - the cross-coupled pairs do not compensate the $LC$-tank losses, but the transistors in triode region contribute to additional tank losses with their channel on-resistance.

The $\lambda_0$ trajectories have larger variations when both oscillators operate with bigger voltage swing caused by MOS transistors entering deeper into the triode region. $\text{Re}(\lambda_0(t))$ of the 1L oscillator is more negative than $\text{Re}(\lambda_0(t))$ of the 1L+2bL oscillator ($C'$ and $C''$), which confirms that the bias inductors help to minimize the effect of the MOS transistors entering the triode region [69]. On the other hand, the maximum of $\text{Re}(\lambda_0(t))$ for the 1L oscillator ($A'$ and $A''$) is also larger, since larger $I_B$ is supplied to the oscillator to achieve the same voltage swing.

The simulated phase noise improvement obtained with the 1L+2bL oscillator is 6.3dB at 1-MHz frequency offset, which is thanks to the two bias inductors. Although without numerical prediction of phase noise, the obtained TVRL for the two cases suggests this improvement by showing that the negative part of $\text{Re}(\lambda_0(t))$ for the 1L+2bL oscillator is limited by the bias inductors. The limiting of $\text{Re}(\lambda_0(t))$ has two consequences: 1) the $Q$-factor deterioration caused by the MOS operation in triode region is limited; 2) less power is needed to compensate the losses due to $\lambda_0$ going deep into the LHP.

5.4.2. LC-tank $Q$-factor effect on the oscillator’s TVRL

The second example evaluates the effect of the resonator $Q$-factor on the TVRL trajectory. The resonator $Q$-factor is varied using the series resistors $r_{o1}$ and $r_{o2}$, which model the finite $Q$-factor of the integrated capacitors. The TVRL obtained for three $Q$-factors (22.8, 18.3, and 13.1) are shown in Fig. 5.10(a). The resonator voltage swing is kept at 1.0-V by adjusting $I_B$. The respective phase noises at 10-MHz offset are $-147.9$, $-147.3$, and $-146.1$ dBc/Hz i.e. about 2-dB difference is obtained for the extreme $Q$-factors (Fig. 5.10(b)). The $Q$-factor effect on lower offsets is less visible due to other non-linear effects such as flicker noise up-conversion [63].

The TVRL obtained with $Q=13.1$ goes deeper into LHP and $I_B$ is increased to achieve the same voltage swing, which also leads to the most positive $\text{Re}(\lambda_0(t))$. The low $Q$-factor causes
5.5. TVRL computation speed-up

In the following are summarized possible methods to increase the speed of the TVRL computation. The amount of points produced by the PSS algorithm within one period can be huge depending on the simulator settings, thus the process of active-device linearization and the actual root computation for all data points may become a burden. Finding an efficient way to reduce the number of points without affecting the root-locus trajectory is one straightforward way to reduce the computation time. Subchapter 5.5.1 proposes a method for computing the time-varying roots only for specific time instants and skipping time-instants without losing important information for the oscillator behavior.

Second, the active-device linearization in its original form shown in Fig. 5.1 takes a lot of CPU time, which is even more than the actual root computation. Since the device parameters are already computed from SpectreRF during the PSS solution, the SpectreRF simulator can be forced to save the linearized device models with additional simulator settings. The procedure is shown in 5.5.2.

Third, the root computation using QZ method computes all roots, but as shown above, only the main root $\lambda_0$ is analyzed. A selective root computation searching in the region of interest on the complex plane can reduce the computation time especially for large-size circuits (large-size matrices). The procedure is shown in 5.5.3.
CHAPTER 5: TIME-VARYING ROOT-LOCUS OF LARGE-SIGNAL LC OSCILLATORS

Fig. 5.11. Graphical visualization of $\varepsilon$ and $\varepsilon_{\text{PSS, max}}$.

5.5.1. Reducing the number of evaluated points

This subchapter evaluates possible point-selection criteria that decreases the number of the evaluated points and relax the TVRL computational demand. The computed steady-state solution by the SpectreRF PSS analysis is in time-domain, and this solution is used for the transistor linearization. The point selection can be based on the time-varying node voltages, which are available prior performing the actual transistor linearization.

The oscillator node-voltage change $\varepsilon_{j,k}$ (Fig. 5.11) measured between two consecutive instants could serve as a basis for the point selection, where $j$ denote the $j$-th node out of $M$ node voltages, and $k$ denotes the $k$-th instant out of $N$ PSS points within $T_{\text{osc}}$. The parameter $\varepsilon_{\text{PSS, max}}$ is the biggest $\varepsilon$ of all node voltages with the entire PSS data ($\varepsilon_{\text{PSS, max}} = \max(\varepsilon_{j,k}, 1 \leq j \leq M, 1 \leq k \leq N$). The amount of evaluation points is reduced after the point selection and $\varepsilon_{\text{max}}$ becomes the node-voltage change for the selected points, where $\varepsilon_{\text{max}}$ is defined as $\varepsilon_{\text{PSS, max}}$ for the reduced points. In the following, we evaluate two possible selections: point decimation and adaptive selection.

1. **Point decimation** – every $n$th point from the PSS data is evaluated, respectively $n-1$ intermediate points are discarded ($n = 1$ corresponds to the entire PSS data). Potential risk of using point decimation is to skip points where the real part of the roots could be of a critical importance for the root-locus. In harmonic oscillators, the points representing the maximum and minimum of the voltage swing are better evaluated than the zero-crossings, because the rate of the oscillator node-voltages change is slow. Consequently, increasing the decimation factor will decrease the computational time at the expense of lower accuracy in the root-locus.

2. **Adaptive point selection** – this is a selection strategy, in which $\varepsilon_{\text{max}}$ for the selected points does not exceed a predefined limit ($\varepsilon_{\text{max}} \leq k*\varepsilon_{\text{PSS, max}}$, $k \geq 1$). The adaptive selection is done in two steps. In the first step the critical points near zero-crossing and minimum (maximum) of the voltage swing are selected with few neighboring points. Additional time instants corresponding to minimum of $|u_{\text{th}}|$ for the switching MOS transistors are
5.5. TVRL computation speed-up

selected, since they correspond to maximum of the transistor conductance $g_{ds}$, respectively the smallest gain of the transistors. The remaining points are selected in the second step such that the predefined limit $\varepsilon_{\text{max}}$ is not exceeded. The zero-crossing instances of the waveforms are captured to the accuracy of the PSS data, and therefore the evaluation of the minimum and maximum of roots is performed with the available PSS precision. The advantage of using the adaptive selection algorithm is the precise evaluation of important time instants, and does not require as extensive computation as the all-PSS-points approach.

Fig. 5.12(a) shows an evaluation of the amount of points that needs to be evaluated for the point decimation and for the adaptive point selections as a function of the relative-to-PSS error ($k = \varepsilon_{\text{max}} / \varepsilon_{\text{PSS}}$). The computation complexity for the point-decimation and the adaptive selection strategy are similar if $k = 3$. The main difference between the two strategies is that the adaptive selection evaluates more precisely the zero-crossings of the waveform. In equal conditions, the adaptive selection strategy should give more accurate root-locus approximation for lower number of points, and it should be selected when the use of full PSS data is computationally expensive.

The impact of the point selection algorithms is shown in Fig. 5.12(b), where the maximum and the minimum of $\text{Re}(\lambda_0)$ are plotted for different error-control parameter $k$. The values of $\max(\text{Re}(\lambda_0))$ and $\min(\text{Re}(\lambda_0))$ are of special interest, because they correspond respectively to the zero-crossings of the oscillator and to the MOS transistor operation in triode and/or cutoff region. As illustrated in Fig. 5.12(b), the adaptive point-selection algorithm evaluates closely these points even when the error control parameter $k$ varies in a wide range, whereas the point-decimating algorithm has random behavior.

![Fig. 5.12](image-url)

**Fig. 5.12.** (a) Evaluation of the number of points that have to be simulated for the two selection strategies as a function of $k$ for 1L+2bL oscillator with $V_{SW}=1V$; (b) evaluated maximum and minimum of $\text{Re}(\lambda_0)$ depending on the error control for the two selection strategies.
5.5.2. **Active device linearization speedup**

As described in Subchapter 5.2, the TVRL is computed after linearization of the active-device models based on the PSS node voltages and separately-run operating-point simulations. Instead, the small-signal models can be obtained directly from the SpectreRF simulator during the PSS algorithm with the help of additional settings. Those time-varying models are saved in the Cadence result directory and they can be accessed through the Cadence Result Browser, or with custom ocean script. The models correspond exactly to the ones obtained with the procedure outlined in 5.2, as they are also computed based on the same PSS data. However, since this computation is done internally in the SpectreRF simulator avoiding the numerous restarts of the simulator itself, the procedure is time-efficient.

By default, SpectreRF does not save the small-signal device models, nor is an option provided in the graphical user interface of the simulator. The desired command can be inserted as a model file specifying the names of the devices for which the small-signal model should be computed. An example of the model file (“model.scs”) contains a statement “save M1:op”, which tells the simulator to save the small-signal parameters for transistor M1. All devices for which the small-signal model should be computed should be listed. The time-varying small-signal models could be visualized with the Cadence Result Browser, or accessed via ocean script.

It has been verified that the procedure outlined in Subchapter 5.2 produce the same models as the results, which can be obtained here. A very small deviation of the numerical values for the model component is possible, as the PSS node voltages are saved with given precision (the precise value of PSS node voltage is rounded when saved into a file). This speedup procedure became known after [P.3] was published. Nevertheless, this speedup method only enhances the algorithm speed and brings it close to a traditional CAD method. The conclusions derived above remain unchanged.

5.5.3. **Selective computation of the roots of interest**

This subchapter addresses the issues to increase the speed of computing the circuit time-varying roots. The QZ method used above utilizes the entire circuit matrices and computes all oscillator roots, including the infinite ones. As such, the QZ method has numerical problems when it comes to large matrices produces by complex circuits. To overcome this limitation, the QZ method can be replaced with iterative procedure that computes only few roots around given region defined by the user, and with a pre-described precision. Other reasons to support iterative methods for root computation are:
5.5. TVRL computation speed-up

1. Only one pair of roots ($\lambda_0$ being the main complex-conjugated pair) is used in the discussion above to evaluate the oscillator behavior. The rest of the roots computed by the QZ methods are of little importance, except the ones that are in the neighborhood of $\lambda_0$, or positive real roots. As the oscillator is stable and its PSS solution is found with SpectreRF, a positive real root is unlikely to appear in LC oscillators.

2. The oscillation frequency of the oscillator is known from the PSS solution, thus the region of search for $\lambda_0$ can be supplied directly to an iterative method ($\text{Re}(\lambda_0) \sim 0$; $\text{Im}(\lambda_0) \sim 2\pi f_{osc}$). Once the root for the first time instant is found (within the defined precision), the computed solution can be used for initial guess for the second time instant. This is valid assumption, since the PSS algorithm takes enough steps to make the transitions smooth, and the root for the next time instant should be nearby the previously computed one. Thus, the amount of iteration when computing $\lambda_0$ should be minimal.

3. Iterative eigenvalue procedure can operate on sparse matrices, whereas the QZ method requires full matrices. The MNA description in commercial simulators is formed with sparse matrices as well, reducing both computation time and memory requirements.

An evaluation of the speed that can be gained using iterative procedure is done below, where all roots of the 1L+2bL oscillator (Fig. 5.2(b)) are computed with the QZ method, and only the main root is computed using the Implicitly-Restarted Arnoldi Method (IRAM) accessible through MATLAB via “eigs” command. The evaluation is done for increasing size of $G$ and $B$ in order to capture the speed enhancement that can be obtained for large circuits. The size of the matrices is increased by sectioning the resonance capacitor $C_o$ into identical cells that are connected in parallel (Fig. 5.13). The capacitor $C_o$ and the resistor $r_o$ are scaled such that the operation of the resonance tank used by the oscillator remains unchanged and the obtained roots can be compared against the native oscillator.

![Fig. 5.13. Schematic of the resonance capacitor $C_o$ sectioned into identical parallel cells, which is used for increasing the size of the oscillator’s G and B matrices.](image-url)
The IRAM implemented in Matlab cannot be directly used for the generalized eigenvalue problem because it requires specific properties of the $G$ and $B$ matrices, which cannot be always obtained in electronic circuits. For instance, the $B$ matrix is not symmetrical, which is mainly due to the full quasi-static model of the MOS transistors. Furthermore, both matrices may become rank-deficient, which is not permitted by the “eigs” function in Matlab. Instead, the IRAM procedure can be applied to the matrix $B^{-1}G$, whose eigenvalues are the same as the generalized eigenvalue problem. The inversion of $B$ is not required (and not recommended) and can be efficiently realized with the Matlab’s backslash operation (“$\backslash$”), which is based on Gaussian elimination. Thus, the use of selective root computation based on the IRAM method requires additional step before the actual root computation.

Fig. 5.14 shows the comparison of the speed between the QZ method and the IRAM computing only $\lambda_0$. The region of search for $\lambda_0$ in the IRAM is defined as $1/T_{osc}$, which is known from the PSS solution obtained with SpectreRF. The estimation for computation time is based on multiple calculations (~100) within one oscillation period to obtain a reliable average (~20000 calculation points). The absolute numbers in Fig. 5.14 should serve for comparison only, as the speed is highly dependent on the computer architecture.

As shown in Fig. 5.14, the time needed for forming $B^{-1}G$ is rather small, which shifts the computation cost only to the IRAM method. For relatively small matrices ($N<50$), the QZ method needs less time than the iterative method and it computes of all circuit roots at once. In addition, the left and right eigenvectors are available for the computed roots, and immediate assessment of the condition number / root precision can be made with (5.5). Thus, the QZ method remains a good choice for root computation in small-sized and medium-sized circuits.
This is the reason why the QZ method is still used as a computation engine in the following chapters to apply the TVRL method for oscillator analysis.

5.6. Summary and contributions

The material presented in this chapter is published by IEEE Transactions in Computer-Aided Design of Integrated Circuits and Systems [P.3] (except for the speedup methods for the TVRL algorithm summarized in Subchapter 5.5). The material from [P.3] is reused with the kind permission of IEEE, © 2010 IEEE. The research has been financed by Tampere Doctoral Program in Information Science and Engineering (TISE), Tampere, Finland.

The contributions of the work presented in this chapter are:

1. Proposed is a new method (TVRL) for analyzing the large-signal behavior of LC oscillators. The proposed method extends the use of the traditional small-signal root-locus analysis towards large-signal operation. A procedure for obtaining the time-varying small-signal parameters from a CAD tool is given. The computations of roots, error estimations of the computed roots, as well as different speed-up methods are addressed in the chapter.

2. The analysis capabilities of the TVRL method are demonstrated by comparing two modifications of LC oscillator that exhibits different phase noise properties. The trajectory of the main root traveling between LHP and RHP is explained via the physical phenomena that are taking place in the large-signal oscillator operation.
Chapter 6

*LC oscillator comparison using TVRL*

6.1. Introduction

Theoretical studies of phase noise in oscillators have helped in understanding noise phenomena and helped to construct high-performance oscillator topologies [69], [110], mostly as stand-alone blocks, and they are optimized as such. A typical measure of overall oscillator performance is the widely accepted Figure-of-Merit (FoM), which takes into account the oscillator phase noise achieved in given power supply conditions. Although the adopted FoM compares different oscillators, its use may lead to misleading results. For instance, the best oscillator FoM is typically achieved in low-voltage conditions [88], [110], but the oscillator phase noise may not satisfy the specifications. In such cases, the voltage swing is raised until the phase noise goal is met. This solution comes at the expense of extra power consumption; it is limited by the breakdown voltage of the active devices, and drives the oscillator away from its FoM optimum. Second, a VCO in some frequency synthesizer is usually followed by frequency dividers. An increased input voltage swing improves the divider phase noise and it can also reduce their power consumption [75], [133]. Thus, a “sub-optimum” oscillator, which generates large voltage swing, can improve the entire system performance, while the “optimum” oscillator remains a theoretical possibility. Third, in low-voltage oscillators the difference between oscillator voltage supply and, for example, a mobile phone battery of 3.6V becomes significant. A linear regulator compensates this difference, but involves significant power losses. For instance, a 1.2V-operated VCO from a 3.6V-battery utilizes only a third of the total power delivered by the battery, which corresponds to ~4.8-dB loss of FoM performance. A high-efficient switching-type regulator would break this dependence, but they are rarely employed near RF blocks due to their interferences.

Given the reasons above, an “optimum” oscillator from the FoM point of view is a vague design target. Since practical oscillator designs have to consider various specifications, such as oscillation frequency, tuning range, phase noise, power supply condition, etc., a complete oscillator comparison is difficult to make. In addition, the large variety of oscillator topologies
in the literature confirms that different oscillator architectures have specifics that may be beneficial in some cases, and sub-optimum in others.

The goal of this chapter is to evaluate and compare the different oscillator topologies by adding new insights derived from Time-Varying Root-Locus (TVRL) [P.3]. The extended comparison brought by the TVRL method gives more guidelines on which topology could serve better for certain specific cases. Furthermore, the evaluation of the TVRL trajectories in different oscillators helps to refine the treatment of the method by underlining its advantages and limitations.

### 6.2. LC oscillators under evaluation

This chapter compares some of the most popular oscillator topologies used in wireless transceivers: the double-cross-coupled oscillator (“1L”), single-cross-coupled oscillator (“2L”), and Differential Colpitts oscillator (“D-Colpitts”). Cross-coupled topologies are found in the low-GHz range and in high-GHz range applications, whereas Colpitts has larger popularity in the high-GHz range. Cross-coupled topologies have a parasitic node associated with the current mirror, which makes them vulnerable at high frequencies [6]. Since all parasitic capacitances in the Colpitts topology can be associated with one of the tank capacitors, the unpredictable parasitic capacitances accumulate in the resonance tank [6]. Nevertheless, cross-coupled topologies are also popular at high frequencies due to their simplicity of design and the accumulated design expertise from low-GHz-range applications. Other oscillator topologies with improved phase noise are found in the literature [88], [110], but they have not yet gained large popularity. Thus, without apparent loss of generality, this work limits the investigation to the main topologies: 1L, 2L, and D-Colpitts. These topologies exhibit structural modifications, a few of which are covered here.

The evaluated modifications of the 1L oscillator are shown in Fig. 6.1(a) and Fig. 6.1(d). The two bias inductors $L_{\text{TOP}}$ and $L_{\text{BOT}}$ in the 1L+2bL topology improve the oscillator phase-noise performance through noise filtering and $Q$-factor preservation of the resonance tank [69]. The values of the passive components and transistor sizes are taken from previously reported VCO ([P.2]). The switched-capacitor bank is modeled with a finite $Q$-factor capacitor $C_0$ for the purpose of the TVRL investigation. The evaluated bottom-biased 1L and 1L+2bL oscillator have a similar structure, but the bias transistors $M_{p3}$ and $M_{p4}$ are replaced with NMOS transistors having the same W/L aspect ratio.

Fig. 6.1 shows also the evaluated modifications of the top-biased 2L oscillator build with NMOS or PMOS switching pair ((b), (c)), with or without bias inductors ((e), (f)) [69], [6]. The
6.2. LC oscillators under evaluation

transistor sizes and passive components are the same as those used by the 1L oscillator in Fig. 6.1(a) and (d) in order to make a fair comparison. The supply voltage of the 2L oscillators is reduced to 1.5 V in order to keep similar voltage headroom for the current mirror \( M_{p3} \)-\( M_{p4} \). The similar headroom causes comparable current mirror nonlinearities that affect in the same way the oscillators’ TVRL trajectories.

Fig. 6.2 shows the D-Colpitts build with the same passive components as the 1L and 2L topologies. The resonance-tank inductance is doubled (two inductors \( L_{\text{MAIN}} \)) to achieve the same oscillation amplitude with the same switching transistors and similar power consumption. The feedback ratio \( n \) is around 1/3 (\( n \approx C_{fb} / (C_{fb} + 2C_f) \)), which is an optimum value for achieving low phase noise [6]. The bias network is built with NMOS transistors with the same size as the PMOS biasing transistors in Fig. 6.1. The oscillation frequency is adjusted with the tank
capacitance ($C_1$ and $C_2$) to be near 4 GHz. The presence of the feedback capacitors in the D-Colpitts architecture has two effects: 1) the effective tank capacitance is reduced, and correspondingly, the achievable tuning range; 2) a larger MOS transconductance is needed to create the required loop gain for sustained oscillations.

The design issues and the phase noise performance of LC oscillators are compared in several works, among which the work of Andreani performs an analytical comparison based on the ISF theory and draws conclusions about the oscillator operation [5], [6], [7]. The oscillator phase noise is linked to the resonance tank, generated voltage swing, and transistor properties as [6], [7]

$$L_{1L} (\Delta \omega) = 10 \log \left[ \frac{k_B T}{C^2 A_{1L} R\Delta \omega^2} \left(1 + \frac{\gamma_n + \gamma_p}{2}\right) \right],$$  \hspace{1cm} (6.1)

$$L_{2L} (\Delta \omega) = 10 \log \left[ \frac{k_B T}{C^2 A_{2L} R\Delta \omega^2} \left(1 + \gamma_n\right) \right],$$  \hspace{1cm} (6.2)

$$L_{\text{COLP}} (\Delta \omega) = 10 \log \left[ \frac{k_B T}{2 \cdot C^2 A_{\text{COLP}} R\Delta \omega^2} \left(1 + \gamma_n \frac{1-n}{n}\right) \right],$$  \hspace{1cm} (6.3)

where $L$ is the oscillator phase noise, $k_B$ is the Boltzmann constant, $T$ is the absolute temperature, $C$ is the equivalent tank capacitor, $A$ is the amplitude of the resonator voltage, $R$ is the equivalent tank resistance at the oscillation frequency, $\Delta \omega$ is the offset frequency, $\gamma_{n(p)}$ is the channel noise factor for NMOS (PMOS) transistors, where the subscripts (1L, 2L, and COLP) denote the corresponding oscillator.

The 1L oscillator produces double voltage swing for a given bias current in a current-limited regime. Since the noise contributed by the active transistors in the two architectures is

Fig. 6.2. Schematic of the Differential Colpitts
6.3. Obtaining the root trajectories of large-signal oscillators

essentially the same (the multiplying term in (6.1) and (6.2)), an operation with constant bias current results in 6dB lower phase noise displayed by the 1L oscillator \((L_{1L}(\Delta \omega) = L_{2L}(\Delta \omega) - 6dB)\) [7]. However, the maximum FoM achievable for the two oscillators is the same ([7], eq. (44)). The 2L-VCO requires twice as much current to produce the same voltage swing, but needs approximately half of the power supply; thus, the consumed power is almost the same [7]. The derivation of (6.1) assumes that the tank capacitance is connected between the two oscillator nodes, and there is no capacitance connected between the oscillator nodes and ground [7]. A severe departure of (6.1) from the simulated phase noise is shown in [7] when this condition is not satisfied. In practical VCOs, however, the tuning varactor and/or the switched-capacitor bank may contribute to a big portion of the tank capacitance being connected to ground. For instance, the off-state capacitance of a switched-capacitor bank is connected between one of the \(LC\) resonator nodes and ground, i.e. the departure of (6.1) from the simulated phase noise is expected at the high-end of the VCO tuning range. A comparison between D-Colpitts and cross-coupled oscillator is given in [6], [110], where the phase noise of a D-Colpitts is expressed as a function of its design parameters with (6.3). The bias noise is excluded from (6.3), and \(n\) is the feedback ratio formed by the capacitors in the Colpitts oscillator.

A comparison between the phase noise equations (6.1)-(6.3) of the three topologies leads to important conclusions. The 1L and the 2L oscillators produce the same phase noise at a given resonator voltage swing \((A_{1L}=A_{2L})\), assuming similar performance of the NMOS and PMOS transistors \((\gamma_n \approx \gamma_p)\), which explains why they often achieve the same performance in practice. On the other hand, the transistors in the D-Colpitts architecture contribute more noise (the multiplier in (6.3)) compared to its two competitors, which limits the D-Colpitts performance. Other second-order effects, such as velocity saturation and large overdrive, make the phase noise performance of the Colpitts topology even worse [6]. Recently, a further development of the Colpitts topology led to the so-called Class-C oscillator [110], which takes advantage of a second feedback and realizes a Class-C operation to achieve excellent FoM performance. The evaluation of the Class-C topology is outside the scope of this work, as not much experience has been gained in the literature and there are only a few design examples using this topology.

6.3. Obtaining the root trajectories of large-signal oscillators

The TVRL computes the system roots for one oscillation period and evaluates their trajectories [P.6] using steady-state time-domain periodic solution obtained by the Cadence SpectreRF simulator [158]. The circuit is linearized for all instants of the periodic solution and
the roots of the characteristic equation are computed. The active-device linearization is done by SpectreRF. The roots are computed with the QZ method applied to the \( G \) and \( B \) nodal matrices. The behavior of large-signal oscillators is analyzed using the trajectory of the main complex-conjugated root \( \lambda_0 \) [P.3]. The analysis using the \( \lambda_0 \) trajectories highlights the differences between the 1L and the 1L+2bL oscillator in previous chapter. The method explains the phase noise improvement achieved by the 1L+2bL oscillator through the limited swing of \( \lambda_0 \) in the right-half plane (RHP) and in the left-half plane (LHP) for a given voltage swing. The \( \lambda_0 \) trajectory goes deeper into the LHP due to higher resonator loading, which consequently deteriorates the oscillator phase noise. On the other hand, the \( \lambda_0 \) trajectory goes deeper in the RHP with bigger negative conductance, which is related to bigger transistor transconductance, higher device noise, and results in higher phase noise.

The goal in this subchapter is to analyze the behavior of the roots for simplified \( LC \) oscillator models obtained in large-signal conditions. The root trajectory evaluation for the simplified models helps to explain the root behavior of the actual oscillators. The simplified models correspond to real oscillator topologies, where the active transistors are replaced with variable conductances modeling the large-signal nonlinearities of the transistor. Typically, a closed-form root-locus analysis to the analysis of simplified oscillators, but the closed-form analysis often requires 2nd-order polynomial [50], [51], which poses serious limitations to the circuit that can be analyzed. Instead of closed-form root-locus analysis, this subchapter utilizes the QZ computation method for precise root evaluation even for simplified oscillator models, and thus it requires no further simplifications needed to arrive at 2nd-order polynomial.

### 6.3.1. The \( RLC \) tank model

The simplest model of an oscillator is a generic \( RLC \) tank (Fig. 6.3(a)) with a conductance \( g_0 \) (\( g_0 = 1 / R \)) accounting for both the tank losses and the negative conductance created by a cross-coupled pair. The complex-conjugated pole corresponding to the 2nd-order \( RLC \) tank is

\[
\lambda_{1,2} = -g_0/(2C_0) \pm j \sqrt{1/(L_0C_0) - g_0^2/(4C_0^2)}. \tag{6.4}
\]

The magnitude of the root is constant and independent of \( g_0 \) (\( |\lambda_{1,2}| = (L_0C_0)^{1/2} \)). During large-signal operation, the oscillator injects energy into the \( RLC \) tank for part of the period (\( g_0 < 0 \)), whereas it dissipates energy for the rest of the period (\( g_0 > 0 \)) [51]. Varying \( g_0 \) forces the complex-conjugated root to travel in a circle with radius of \( (L_0C_0)^{1/2} \) ([28], Fig. 3.11).

Fig. 6.3(b) shows a more realistic model of a cross-coupled \( LC \) oscillator with differentially-connected capacitors with their mid-point grounded, and conductances \( g_1 \) and \( g_2 \) associated with the cross-coupled pair transistors. The topology in Fig. 6.3(b) is characterized
6.3. Obtaining the root trajectories of large-signal oscillators

Fig. 6.3. Simplified oscillator models and their root-loci with conductance $g$ varied from 0 to $\infty$ for: (a) RLC tank; (b) RLC tank with grounded capacitors and conductances.

by a third-order system having one real pole and a complex-conjugated pair given by the characteristic polynomial

$$P = s \cdot \left( s^2 \cdot C^2 + s \cdot 2gC + g^2 \right) + s \cdot 2C + 2g = 4 \left( \frac{s \cdot C}{2} + \frac{g}{2} \right) \left( s^2 \cdot \frac{L}{2} \cdot \frac{C}{2} + s \cdot \frac{g}{2} \cdot L + 1 \right)$$

where $g = g_1 = g_2$ and $C = 2C_0$. The complex-conjugated pair is identical to (6.4) and its trajectory is defined by a circle in the complex plane. The real pole is $\lambda_3 = -g/C$, which is strictly negative for positive values of $g$.

However, the fully-differential condition $g_1 = g_2$ is satisfied only for the oscillator start-up and near the voltage zero-crossings. During large-signal operation one of the MOS transistors goes into the triode region ($g_1 \gg 0$), the other one goes into the cutoff region ($g_2 \approx 0$), and the cross-coupled pair does not generate negative conductance. The root trajectories of the third-order system can be evaluated by varying $g_1$ corresponding to one MOS transistor operating in the triode region. Since a closed-form solution of an arbitrary third-order polynomial is hard to comprehend [134], the root trajectories are evaluated numerically and we evaluate the extreme cases of $g_1$ ($g_1 = 0$ and $g_1 = \infty$), while keeping $g_2 = 0$. When $g_1 = 0$ the resonance tank consists of the main inductor $L_0$ and the two capacitors forming a complex conjugated pair at $\lambda_{1,2} = \pm j\sqrt{1/(L_0C_0)}$ and a real root at $\lambda_3 = 0$. When $g_1 = \infty$, $g_1$ shortens one of the $2C_0$ capacitors, which doubles the tank capacitance of the RLC tank and moves the complex conjugated pair to $\lambda_{1,2} = \pm j\sqrt{1/(2L_0C_0)}$. Compared to the simple RLC tank (Fig. 6.3(a)), where $g_0 = \infty$ transforms the complex-conjugated pair into one root at the origin and another one at infinity, the grounded RLC tank features root locus trajectory transforming one complex pair into another complex pair with $\sqrt{2}$ lower frequency. The root trajectory in this case does not follow the circle
defined in the simple RLC case. The imaginary part of $\lambda_{1,2}$ drops with MOS transistor entering the triode region during large-signal operation.

### 6.3.2. Single cross-coupled pair with LC filter

The oscillator model shown in Fig. 6.4(a) approximates the large-signal operation of a cross-coupled pair degenerated with an $L_bC_b$ filter. The conductances $g_1$ and $g_2$ are relatively small when the transistors are in the active region, and the resulting two complex-conjugated pairs are determined by the two LC tanks ($\omega_{1,2}=\omega_b=(L_0C_0)^{-1/2}$ and $\omega_{3,4}=\omega_b=(L_bC_b)^{-1/2}$). Negative conductance is applied across the main resonator and forces oscillations at $\omega_0$. During large-signal operation, however, $g_1$ becomes significant, while $g_2$ becomes very small, modeling the triode and the cutoff region respectively. This scenario corresponds to two LC tanks coupled with a conductance, which results in a fourth-order resonator (Fig. 6.4(b)) with complicated dependence of the circuit roots from the passive components. In the extreme case of $g_1$ representing short circuit and $g_2$ representing open circuit, the pole frequencies associated with the fourth-order resonator are [12]

$$
\omega_{L,H}^2 = \frac{L_bC_1 + L_bC_2 + L_bC_1}{2L_bL_aC_1C_2} \pm \frac{\sqrt{(L_bC_1 + L_bC_2 + L_bC_1)^2 - 4L_bL_aC_1C_2}}{2L_bL_aC_1C_2}
$$

where $C_1=C_b+2C_0$ and $C_2=2C_0$. Thus, under a large-signal condition the original pole frequencies $\omega_b$ and $\omega_b$ are transformed into $\omega_L$ and $\omega_H$ given by (6.6). The values of $\omega_b$ and $\omega_b$ are design parameters to achieve respectively the desired oscillation frequency and proper noise filtering ($\omega_b \approx 2\omega_b$) [69], but the frequencies $\omega_L$ and $\omega_H$ are a complex function of the passive components building the two resonators.

In Fig. 6.5(a) are plotted root trajectories with constant $\omega_b$ and $\omega_b$ obtained with different $L_bC_b$ resulting to a set of frequencies $\omega_L$ and $\omega_H$. The main root $\lambda_0$ approaches one of the angular frequency defined by the fourth-order tank (6.6). The approached frequency is usually $\omega_H$ with reasonable tank-component values ($\omega_H > \omega_b$, Fig. 6.5(b)), while $\omega_b$ transforms to $\omega_L$. 

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Fig. 6.4. (a) Simplified model of a cross-coupled oscillator with LC filter; (b) and its large-signal equivalent circuit obtained with $g_1 \approx \infty; g_2 \approx 0$. 

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6.3. Obtaining the root trajectories of large-signal oscillators

The root trajectories shown in Fig. 6.5 could be explained as follows. When $g_1$ increases, part of the tank capacitance ($2C_0$) becomes connected to the filtering network $L_bC_b$ and $\lambda_b$ drops. The “vanishing” part of the tank capacitance forces the imaginary part of $\lambda_0$ to increase. Thus, the presence of $L_bC_b$ filter causes $\text{Im}(\lambda_0)$ to rise from its nominal value as the active devices enter the triode region, which is opposite to the roots behavior in cases without $L_bC_b$.

The root trajectories shown in Fig. 6.5 are obtained with large conductance variations; thus, only part of root-loci can be observable in practice ($\lambda_0$ will never reach $\omega_H$). Another important observation is that high value of $g_1$ does not severely harm the oscillator operation when an $L_bC_b$ filtering is used. The main root $\lambda_0$ goes deep into the LHP in the case without $LC$ filter and its $Q$-factor deteriorates drastically. In contrast, the use of $L_bC_b$ filter limits the excursion of $\lambda_0$ in the LHP and preserves the tank $Q$-factor. The degree of $Q$-factor preservation depends on the specific values used in $L_bC_b$, with bigger $L_b$ inductance corresponding to better $Q$-factor preservation.

6.3.3. Double cross-coupled pair with LC filters

A double cross-coupled-pair oscillator may utilize two LC filters to degenerate both cross-coupled pairs (Fig. 6.1(b)), which is modeled with the circuit in Fig. 6.6(a), where the MOS transistors are replaced with conductances $g_{n1,2}$ and $g_{p1,2}$. The effect of the MOS transistor conductance can be neglect ($g_{n1,2}$ and $g_{p1,2}$) at the oscillator start-up, and the roots are

$$\omega_b \cong (L_0C_0)^{-1/2}; \omega_0 \cong (L_0C_0)^{-1/2}; \omega_l \cong (L_0C_0)^{-1/2}$$

During the maxima of the voltage swing, two of the conductances are large ($g_{n1}$ and $g_{p2}$), whereas the other ones are negligible ($g_{n2} \approx g_{p1} \approx 0$) – the oscillator model reduces to the equivalent circuit shown in Fig. 6.6(b). One of the tank capacitors, $2C_0$, is connected in parallel to the $L_bC_b$ filter and the second $2C_0$ capacitor is in parallel with the $L_bC_0$ filter in the extreme
Fig. 6.6. (a) Model of a double cross-coupled-pair oscillator with LC filter; (b) its simplification with $g_{n1} \approx g_{p2} \approx \infty$ and $g_{n2} \approx g_{p1} \approx 0$; (c) root-loci with $g_{n1}=g_{p2}$ swept from zero to infinity ($g_{n2}=g_{p1}=0$, $L_0=1\text{nH}$, $C_0=1.5\text{pF}$, $L_b=L_t=0.5\text{nH}$, $C_b=C_t=0.75\text{pF}$).

The numerically evaluated root trajectories are presented in Fig. 6.6(c) for a set of passive components in order to demonstrate the effect of the two LC filters. Ideal passive components are used with values such that $\omega_b=\omega_t=2\cdot \omega_0$ ($L_0=1\text{nH}$, $C_0=1.5\text{pF}$, $L_b=L_t=0.5\text{nH}$, $C_b=C_t=0.75\text{pF}$). The imaginary part of $\lambda_0$ increases, due to the fact that part of the tank capacitance is transferred to the filtering network, and $\lambda_0$ reaches $\omega_L$. The poles associated with the LC filters ($\omega_b$ and $\omega_t$) drop in frequency and they head towards $\omega_L$ and the origin. The behavior of $\lambda_0$ is similar to the trajectory presented in Fig. 6.5 for the single cross-coupled-pair topology. Since $\lambda_0$ and the filter poles travel in different directions, the frequency relationship needed to achieve filtering functions ($\omega_b \approx 2\omega_0$, [69]) is not satisfied and the filtering becomes less effective during the maxima / minima of the oscillator waveform.

6.3.4. Differential Colpitts

Fig. 6.7(a) shows a simplified model of the D-Colpitts from Fig. 6.2, where $g_{1,2}$ are the $M_{n1,2}$ drain-source conductances and $g_{3,4}$ are the drain-source conductances of the bias transistors $M_{a3,4}$. The conductances $g_{1}-g_4$ can be neglected when all transistors are in the active region (reducing the model to Fig. 6.7(b)), and the frequencies of the two complex-conjugated
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Fig. 6.7. Large-signal D-Colpitts: (a)-(b) simplified model of large signal conditions; (c) root-loci obtained by varying $g_1$; (d) root-loci obtained by varying $g_3$.

pole pairs are

$$\omega_{1,2}^2 = \frac{1}{L_0 \left( C_0 + 2C_a \right)}; \quad \omega_{3,4}^2 = \frac{1}{L_0 C_0},$$

(6.9)

where $C_a = C_{f1} || C_F || C_{f2}$. If the main transistor $M_{n1}$ goes to the deep triode region ($g_1$=0), its drain-source conductance shortens the feedback capacitor $C_{f1}$. In the extreme case of $g_1=\infty$, the expression of the pole frequencies is again given by (6.9), but $C'_a = C_F || C_{f2}$. Thus, the oscillation frequency $\omega_{1,2}$ decreases, whereas $\omega_{3,4}$ is not affected ($\omega_{3,4}$ is independent of $g_1$). If the bias transistor $M_{n3}$ goes to the deep triode region ($g_3$=0), then the feedback between the two oscillator sections is effectively broken, leading to complex-conjugated roots at

$$\omega_{1,2}^2 = \frac{1}{L_0 \left( C_0 + C_{f1} \right)}; \quad \omega_{3,4}^2 = \frac{1}{L_0 \left( C_0 + C_{f2} || C_F \right)}.$$

(6.10)

A variation of $g_3$ affects both poles, with the main pole going higher in frequency. It is interesting to observe that the main pole follows the part of circuit, which still has a working biasing circuitry. The lower frequency pole ($\omega_{1,2}$) does not provide conditions for oscillations, since the increase of $g_3$ shortens the feedback to the $M_{n1}$ transistor. The behavior of the two cases is demonstrated in Fig. 6.7(c) and (d), where $L_0=1\text{nH}$, $C_0=1.5\text{pF}$, and $C_F=C_{f1}=C_{f2}=0.6\text{pF}$.

However, it should be noted that active transistors in the D-Colpitts topology do not enter as deep into the triode region (shown in Subchapter 6.5) as the transistors in the cross-coupled topologies, and the above behavior can be hardly observed in practice. Furthermore, the change of $g_1$ and $g_3$ is correlated with the drain and source node voltages of $M_{n1}$, which are almost in phase and they force both conductances to increase or decrease at the same time. Since $g_1$ and $g_3$...
move the main pole in different directions (shown in Fig. 6.7(c) and Fig. 6.7(d)), the correlated change of $g_1$ and $g_3$ helps to keep small variations of the main pole under large-signal conditions.

### 6.4. Oscillator start-up

#### 6.4.1. Main root trajectory at start-up as a function of $I_B$

The root-locus method is often used to evaluate the start-up behavior of oscillators [11], [123]. As the roots evaluation using TVRL is based on circuit-description matrices and accounts for the full complexity of the oscillator, the method avoids typical feedback-loop-breaking operations [123]. The complex-conjugated pair with the most positive real part, which crosses the imaginary axis of the $s$-plane, is the one responsible for the oscillations.

The root loci of the 1L and 2L architectures from Fig. 6.1 are plotted in Fig. 6.8(a) with varying $I_B$. The main root $\lambda_0$ goes enters the RHP as the bias current $I_B$ is increased, which corresponds to larger negative conductance generated by the cross-coupled pair(s). The 1L oscillator requires smaller $I_B$ to cross the $j\omega$-axis due to the second cross-coupled pair. However, the second cross-coupled pair slightly increases the parasitic capacitance connected to the resonance tank and $\text{Im}(\lambda_0)$ is decreased. The operation of the 1L and the 2L oscillator can be assumed as small-signal and differential at start-up. The common node of the cross-coupled pair is connected to virtual ground and the impedance connected to this node has no effect on the start-up. This is confirmed in Fig. 6.8(a), where the start-up root-loci for the oscillators employing bias inductors overlap with those without inductors. Therefore, the bias inductors affect mostly the large-signal oscillator operation, and its benefits should be evaluated under such operation.
6.4. Oscillator start-up

The start-up process for the D-Colpitts oscillator is illustrated in Fig. 6.8(b) for different feedback ratio $n$ realized by varying the feedback capacitor $C_F$. The larger feedback ratio increases the loop gain and it requires smaller MOS transconductance $g_m$, with respectively smaller $I_B$ to meet the oscillation conditions. As $C_F$ is decreased to achieve larger $n$, the effective tank capacitance is also decreased, which leads to higher oscillation frequency. The startup behavior of the D-Colpitts oscillator is essentially different from the negative-resistance oscillators, because when using large $g_m$ the root-locus starts returning to the LHP [123].

6.4.2. Proof of sinusoidal operation

The existence of a complex-conjugated pair in a RHP is a necessary condition to start oscillations, but other undesired phenomena might occur [44], [45]. Undesired phenomena could be relaxation oscillations, chaos, or even latch-up. A typical reason for relaxation oscillation is the presence of real pole in the RHP. Chaos and latch-up, on the other hand, might be triggered by specific nonlinearity or hysteresis produced by the active devices. In this subsection we show that these undesired phenomena are avoided and the investigated oscillators produce sinusoidal waveforms.

Fig. 6.9(a) shows the complete root-locus map of the 1L+2bL oscillator obtained at start-up with varying $I_B$, and Fig. 6.9(b) shows the root trajectories at large-signal condition for one oscillation period. In both cases, only the main complex-conjugated pair $\lambda_0$ enters the RHP and all real roots remain in the LHP. Thus, relaxation oscillations cannot be initiated at start-up, neither are they produced under large-signal conditions. Similar plots are obtained for all oscillator topologies presented in Fig. 6.1 and Fig. 6.2.

For further analytical proof, the condition $g_m \cdot r_L \geq 1$ required to obtain relaxation oscillations [44] is investigated, where $g_m$ is the transconductance of the cross-coupled pair
transistor and $r_L$ is the series resistance of the inductor accounting for all tank losses. Note that the condition above implies a real pole in the RHP [44]. Using simulations of the complete $LC$ resonator, we obtained $r_L$ of approximately 3.32Ω. Thus, the transistor $g_m$ should be bigger than 300mS in order to initiate relaxation oscillations. In the start-up root-loci plots shown in Fig. 6.8, the maximum transistor $g_m$ obtained for $I_B = 5\text{mA}$ does not exceed 200mS. Furthermore, an oscillator operation with such a large current is somewhat impractical since the voltage swing reaches the power supply limits and unnecessary distortions are generated. Nevertheless, the above calculation shows a good safety margin that rules out relaxation oscillations.

Latch-up, on the other hand, can be triggered by the nonlinearity of the cross-coupled pair. Fig. 6.10(a) shows a piecewise approximation of the cross-coupled pair nonlinearity used for the analysis of latch-up in [44] and [45]. The piecewise approximation of the nonlinearity is divided into three segments: an inner segment modeled by a small-signal conductance $g_0$, and two outer segments modeled by a small-signal conductance $g_1$. The negative conductance $g_0$ compensates the tank losses in the inner segment of the nonlinearity and initiates oscillations. The positive conductance $g_1$ introduces losses to the resonance tank in the outer segments of the nonlinearity. The oscillator will unavoidably enter the outer segments as the oscillation amplitude grows in the inner segment. Latch-up will occur if the equilibrium points of the outer segment are real, i.e. the equilibrium point lies in the same outer segment, and the oscillator never returns to the inner segment. The possibility for latch-up is studied by evaluating the position of the equilibrium point of the outer segment. Fig. 6.10(b) shows the simulated nonlinearity of the 1L oscillator, and the 2L oscillator using NMOS and PMOS transistors, all biased with $I_B = 2\text{mA}$. 

Fig. 6.10. Cross-coupled pair nonlinearity: (a) simplified piecewise approximation; (b) simulated nonlinearity for the 1L oscillator and 2L oscillator with NMOS and PMOS transistors.
The equilibrium points of the other segments are equal to $\mp ma/(m-1+\alpha)$ [45], where $m = V_0/V_B$, $\alpha = r_c/r$, $r = 1/g_0$, $r_c$ is the inductor series resistance, $V_0$ and $V_B$ are defined in Fig. 6.10(a). The simulated nonlinearity of the 1L oscillator is approximated with $V_0 = 4.14\,\text{V}$, $V_B = 0.31\,\text{V}$, $g_0 = 10.22\,\text{mS}$, and $r_L = 3.32\,\Omega$. The calculated equilibrium point of the outer segments of the 1L oscillator is approximately $36.5\,\text{mV}$, which is a magnitude below $V_B$. The calculations made for the 2L oscillators are based on the 4D model [44], which is specially tailored to 2L oscillators using two identical $L$/$C$ tanks. The equilibrium points of the 4D model in the outer segments are $\pm 0.5/(1+Q^2/\Delta_g)$, where $Q$ is the tank quality factor, and $\Delta_g = g_1/g_0$. The calculated equilibrium point of the outer segments for the 2L-N oscillator is approximately $20.2\,\text{mV}$ with $V_B = 0.245\,\text{V}$, whereas the calculation for the 2L-P oscillator shows an equilibrium point at approximately $14.5\,\text{mV}$ with $V_B = 0.330\,\text{V}$. In all three cases, the equilibrium points of the outer segments are not real, and therefore potential latch-up is avoided. Reference [44] suggests a minimization of Total-Harmonic Distortions (THD) by reducing $\Delta_g$, which can be effectively achieved by employing a current-mirror biasing of the cross-coupled pair. The current-to-voltage transfer function of a cross-coupled pair saturates at $I_B/2$ when ideal current mirror is used [24], which implies $g_1 \approx 0$ and $\Delta_g \approx 0$. Thus, a current mirror biasing reduces THD and greatly omits the possibilities for latch-up by forcing the equilibrium points of the outer segments to be very close to the origin. The nonlinearity needed to obtain bounded oscillations is often embedded within the employed active devices, which limits the possibility for nonlinearity optimization and it requires an examination of the latch-up conditions. A separation of the critical nonlinearity from the oscillator structure is proposed in [46], which allows nonlinearity optimization with the target to avoid undesired oscillator behaviors.

A hysteresis in the nonlinear circuit is another possible reason for triggering a latch-up in oscillators [45]. The simulated nonlinearities shown in Fig. 6.10(b) display no hysteresis. Simulations of the D-Colpitts oscillator also show no hysteresis, because there is no dc feedback that could eventually trigger such behavior. An analysis of Colpitts oscillator using the piecewise approximation approach is not done here, as the negative resistance of the Colpitts oscillator is created by the feedback capacitors, which is frequency dependent and does not require active-device nonlinearity.

SpectreRF transient simulations are performed for each evaluated oscillator in order to confirm that the oscillators generate proper sinusoidal signal. Fig. 6.11(a) shows the start-up envelopes of the 1L oscillator with $I_B = 2\,\text{mA}$ and $I_B = 5\,\text{mA}$. The steady-state oscillations are
demonstrated in Fig. 6.11(b) with THD computed for the first 10 harmonics. As is seen from the plots, sinusoidal signals are produced for a large range of bias currents with sensible distortions (THD of a square-wave signal is above 40%). All the investigated oscillators perform similarly with THD not exceeding 5% even for voltage swings reaching the power supply rails.

6.5. Active-device operating trajectory comparison

The large-signal operation of the LC oscillator forces the transistors to operate both in linear and in nonlinear regions, which is seen as a variation of their bias conditions. The variable bias condition in periodic circuits forms a closed trajectory. Different oscillator topologies force different bias trajectories depending on the active device connection and on the voltage swing. The goal of this subchapter is to compare the bias trajectories of the active devices imposed by the different oscillator topologies. The bias trajectory comparison is done for the same voltage swing generated by the oscillators ($V_{pp} = 1.2$V).

The bias trajectory of the active NMOS transistors in the Top-Biased 2L oscillator (Fig. 6.12(b)) displays an operation in all transistor regions – cutoff, triode, and active region. The sinusoidal differential output is applied to the transistor’ drain and source and thus it forces symmetrical bias trajectory for the rising and the falling part of the waveform. Among the other oscillators, the NMOS transistors of the Top-Biased 2L oscillator enter deepest in the triode region, which corresponds to the most excessive losses and resonator loading. The additional inductor $L_{BOT}$ limits the transistor operation in the triode region and respectively limits excessive losses. The triode operation is limited as an absolute value of the on-resistance, as well as for a reduced part of the period. However, the phase of the $v_{BOT}$ node voltage is delayed
6.5. Active-device operating trajectory comparison

Fig. 6.12. NMOS bias trajectory comparison between: (a) 2L oscillator modifications operating with $V_{PP} = 1.2V$; (b) 1L oscillator modifications operating with $V_{PP} = 1.2V$.

with respect to the resonator voltages. The delayed phase of $v_{BOT}$ causes an asymmetric bias trajectory and asymmetric root-locus during the rising and falling time of the waveform. The asymmetry of the waveform gives a rise to the AM-PM frequency up-conversion [64], [97]. Thus, the phase noise improvement achieved by the biasing inductor $L_{BOT}$ is slightly reduced due to the increased AM-PM noise up-conversion. The effect of the current mirror on the bias trajectory is similar to the effect caused by $L_{BOT}$ (red curve in Fig. 6.12(a)). Although the transistor enters deeper in the triode region compared to the transistors in the modification using $L_{BOT}$, the impedance of the current mirror acts as degeneration and does not allow excessive resonator losses. The node voltage $v_{BOT}$ is delayed with respect to the resonator voltages causing asymmetric operating point and asymmetric root-locus trajectory.

The bias trajectory comparison between the 1L oscillator modifications is shown in Fig. 6.12(b). The main transistors in the 1L oscillator enter deep in the triode and cutoff region. The bias trajectory in the triode region is limited when using bias inductors or current mirror, but both techniques cause asymmetric bias trajectory. The bias trajectory of the basic 1L oscillator may go even into the fourth quadrant when the drain voltage becomes smaller than the source voltage.

In comparison, the bias trajectory for the D-Colpitts is essentially different from the other oscillators obtained for the same voltage swing. Fig. 6.13(a) shows the simulated node voltages and the drain current of $M_{n1}$ for 1.2V voltage swing, and Fig. 6.13(b) shows the corresponding $M_{n1}$ bias trajectory. The drain-source voltage and the drain current of $M_{n1}$ are shifted with respect to the oscillator output $V_{d,n1}$. Points “A” and “B” in Fig. 6.13 are two example instants with equal $V_{ds}$ voltages in the falling and rising part of the output voltage. The $M_{n1}$ drain current has different values for “A” and “B” due to the asymmetry of $V_{ds}$ and $I_d$. The bias trajectory therefore forms a loop with large opening underlining this asymmetry.
As shown in Fig. 6.13(b), the $M_{n1}$ transistor stays mostly in the active region, and only slightly enters the triode and cutoff region. Since the feedback voltage applied to the source of $M_{n1}$ is almost in-phase with the resonator output, only a portion of the output voltage is applied to the transistor as drain-source voltage. The scaled drain-source voltage depends on the feedback ratio $n$. This feature of the Colpitts oscillator helps the active device to operate mostly in the active region for the same voltage swing. This advantage of the D-Colpitts can be utilized in advanced CMOS processes, where the maximum allowed voltages across the transistor limit the oscillator voltage swing. As shown in [90], the specifics of the oscillator topology can allow generation of large voltage swing without driving the transistors into breakdown regions.

### 6.6. Oscillator comparison using power-conversion factor

The analytical derivations of voltage swing as a function of design parameters assume current-limited operation [6], [7], [69]. These derivations become inadequate and depart from actual oscillator behavior as the voltage swing approaches the power supply rails. Reference [20] obtains in analytical form the steady-state oscillations in large-signal $LC$ VCO, but the circuit model and transistor operation is simplified. The nonlinearities involved in the voltage-limited operation make it hard to derive precise analytical expression for the relationship between bias current and generated voltage swing. However, a large-signal operation is desired in low-noise oscillators to achieve low phase noise, especially at low-voltage power supplies.

This subchapter evaluates the abilities of the different architectures to efficiently generate large voltage swings for a given power consumption. This ability is estimated using a power-conversion factor (PCF), which is defined as the ratio $V_{pp}/I_{OSC}$ ($V_{pp}$ is the peak-to-peak resonator voltage for given current $I_{OSC}$ injected into the oscillator core). The evaluation of PCF
is done numerically using the SpectreRF simulator. The power conversion factor has a dimension of impedance and it is proportional to the parallel resistance of the resonator $R_{eq}$ if the oscillator operates in current-limited regime (PCF = $V_{pp}/I_{OSC} \approx (4/\pi)R_{eq}$, [6], [64]) and gets smaller when the oscillator enters the voltage-limited regime. The current $I_{OSC}$ may deviate significantly from $I_B$ ($I_B$ is injected in the current mirror) when the bias transistor $M_{p3}$ enters the triode region due to large signal amplitudes. The current $I_B$ is not taken into account, because it can be avoided in applications where the gate of $M_{p3}$ is voltage-biased.

The obtained PCF for the investigated oscillator modifications is summarized in Table 6-I as a function of the generated voltage swing. Once started, the D-Colpitts generates sufficiently large swing, which prevents the obtaining of reliable PCF for less than 1.0 $V_{pp}$. This is because the active transistors in D-Colpitts architecture operate mostly in the active region (Subchapter 6.5), and relatively large swing is needed to force them to leave the active region such that further voltage growth is bounded. When the cross-coupled oscillators generate small swing (0.6 $V_{pp}$), the transistors also spend a significant part of the period in the active region, and the biasing inductors act only as a generation. This explains why the PCF of the oscillators without bias inductors is bigger than the PCF of the topologies with inductors. However, the oscillator modifications exploiting $L_{TOP}/L_{BOT}$ have nearly independent PCF as a function of the voltage swing, which leads to an efficient use of $I_{OSC}$ for increasing the voltage swing. On the other hand, the other topologies use less silicon area, but increasing their voltage swing is power inefficient. Since the PCF is nearly constant for the topologies using bias inductors, their utilization prevents quality-factor degradation caused by MOS transistors entering the triode region [69].

**Table 6-I: PCF ($V_{pp}/I_{OSC}$) comparison between the evaluated LC oscillators**

<table>
<thead>
<tr>
<th>Topology</th>
<th>0.6 $V_{pp}$</th>
<th>0.8 $V_{pp}$</th>
<th>1.0 $V_{pp}$</th>
<th>1.2 $V_{pp}$</th>
<th>1.5 $V_{pp}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TopB 1L</td>
<td>630.6</td>
<td>553.1</td>
<td>482.0</td>
<td>425.4</td>
<td>366.0</td>
</tr>
<tr>
<td>TopB 1L+2bL</td>
<td>540.5</td>
<td>536.4</td>
<td>530.9</td>
<td>526.1</td>
<td>523.3</td>
</tr>
<tr>
<td>BotB 1L</td>
<td>648.0</td>
<td>599.5</td>
<td>535.0</td>
<td>478.0</td>
<td>413.0</td>
</tr>
<tr>
<td>BotB 1L+2bL</td>
<td>549.6</td>
<td>542.4</td>
<td>536.9</td>
<td>532.3</td>
<td>526.1</td>
</tr>
<tr>
<td>2L, N</td>
<td>318.7</td>
<td>293.4</td>
<td>263.2</td>
<td>236.0</td>
<td>205.2</td>
</tr>
<tr>
<td>2L, N, $L_{BOT}$</td>
<td>261.5</td>
<td>261.8</td>
<td>262.0</td>
<td>262.4</td>
<td>262.0</td>
</tr>
<tr>
<td>2L, P</td>
<td>273.1</td>
<td>263.7</td>
<td>251.4</td>
<td>241.9</td>
<td>230.7</td>
</tr>
<tr>
<td>2L, P, $L_{TOP}$</td>
<td>254.3</td>
<td>256.4</td>
<td>256.9</td>
<td>257.5</td>
<td>257.2</td>
</tr>
<tr>
<td>D-Colpitts</td>
<td>-</td>
<td>-</td>
<td>203.3</td>
<td>220.7</td>
<td>231.4</td>
</tr>
</tbody>
</table>

Similar to 1L modifications, the PCF of the 2L inductor-enhanced topologies remains nearly constant in large-signal conditions, while it drops for the classic architectures, displaying power losses. The power losses are the highest for the 2L-N topology since the cross-coupled pair is grounded, while the PMOS cross-coupled pair in the 2L-P topology is degenerated by a
current mirror. The PCF of the 2L oscillators is nearly half that of the 1L oscillators. The same inductor is used in both topologies, but the oscillator current ($I_{\text{osc}}$) in the 1L architecture passes through the whole resonator, while in the 2L architecture $I_{\text{osc}}$ goes through the half resonator. Thus, for the same inductance and oscillator current the 1L topology generates almost twice as high swing [6], [64].

Compared to the cross-coupled topologies without bias inductors, the D-Colpitts architecture has stable PCF, because the amplifying transistors ($M_{n1}$ and $M_{n2}$) spend most of their time in the active region (Fig. 6.13) and do not load the resonator extensively. Therefore, the behavior of the D-Colpitts under large-signal condition is more stable compared to the other architectures. Thus, the D-Colpitts oscillator should be selected if large signals have to be efficiently generated without extra bias inductors.

6.7. Oscillator comparison using TVRL

The goal of this subchapter is to compare the oscillator modifications using the TVRL method [P.3]. The oscillator TVRL trajectories are analyzed with respect to what is expected from the root trajectories obtained with the simplified oscillator models presented in Subchapter 6.3. The evaluation of the TVRL trajectories and the explanation for their behavior uses the information obtained with SpectreRF for the bias trajectories (Subchapter 6.5), the PCF (Subchapter 6.6), as well as the simulated phase noise. The auxiliary information given by the SpectreRF helps to explain the TVRL trajectories and to verify the conclusions drawn from the TVRL analysis. Furthermore, the TVRL method is used for the analysis of number of oscillator modifications involving more than one complex-conjugated pair, which demonstrates that the TVRL is applicable for the analysis of higher-order oscillators as well.

6.7.1. 1L oscillator modifications

Fig. 6.14 shows the $\lambda_0$ trajectories of the 1L oscillator modifications depicted in Fig. 6.1 and their bottom-biased counterparts obtained for a 1.2-V voltage swing. The TVRL of the classic 1L topologies approximate the behavior of the grounded $RLC$ tank (Subchapter 6.3.1). However, one of the cross-coupled pairs is degenerated with the current mirror, whereas the other one is grounded. Thus, the type of biasing (top-biasing or bottom-biasing) determines which pair would have bigger effect on the root-locus. The NMOS pair is grounded in the top-biasing case (Fig. 6.1(a)) and the NMOS on-resistance has greater impact on the TVRL than the PMOS on-resistance. Although the trajectories obtained with the two biasing cases are similar, $\lambda_0$ of the top-biased architecture goes deeper in the LHP because the on-resistance of the NMOS
Table 6-II: Noise contribution @ 1MHz offset for the 1L oscillator modifications

<table>
<thead>
<tr>
<th></th>
<th>Top-Biased</th>
<th>Bottom-Biased</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1L</td>
<td>1L+2bL</td>
</tr>
<tr>
<td>RESONATOR</td>
<td>13.66</td>
<td>13.32</td>
</tr>
<tr>
<td>M_{n1,n2} (flicker)</td>
<td>0.14</td>
<td>0.23</td>
</tr>
<tr>
<td>M_{n1,n2} (white)</td>
<td>30.73</td>
<td>4.53</td>
</tr>
<tr>
<td>M_{p1,p2} (flicker)</td>
<td>0.53</td>
<td>0.21</td>
</tr>
<tr>
<td>M_{p1,p2} (white)</td>
<td>11.62</td>
<td>4.13</td>
</tr>
<tr>
<td>M_{BIAS} (flicker)</td>
<td>94.59</td>
<td>13.42</td>
</tr>
<tr>
<td>M_{BIAS} (white)</td>
<td>27.13</td>
<td>3.50</td>
</tr>
<tr>
<td>PN1M_{TOTAL}</td>
<td>-120.1</td>
<td>-126.7</td>
</tr>
<tr>
<td>I_{DD} (mA)</td>
<td>2.82</td>
<td>2.28</td>
</tr>
<tr>
<td>FoM</td>
<td>184.6</td>
<td>192.2</td>
</tr>
</tbody>
</table>

transistor is smaller than that of the PMOS transistor. In order to compensate the excessive losses, \( \lambda_0 \) of the top-biased oscillator goes deeper also in the RHP. Following the reasoning outlined in [P.3], the bigger \( \lambda_0 \) swing of the top-biased oscillator both in the LHP and in the RHP suggests high switching-pair-transistor noise. This conclusion is verified by comparing the noise contributors presented in Table 6-II for the different oscillators.

The \( \lambda_0 \) trajectories of the 1L+2bL oscillators shown in Fig. 6.14(a) are not visibly affected by the biasing scheme, which means that the additional inductors isolate the effects of the biasing network. The bias-network isolation suggests also that the bias noise would be hardly perceived by the oscillator. The root trajectories are governed by the sixth-order system (Subchapter 6.3.3), which pulls the imaginary part of \( \lambda_0 \) upwards when the active devices enter the triode region.

The real part of \( \lambda_0 \) obtained for the different 1L modifications are shown in Fig. 6.14(b). \( \text{Re}(\lambda_0) \) is most positive at the oscillator’s zero-crossing, corresponding to all active devices operating in the active region, while \( \text{Re}(\lambda_0) \) is the most negative at the maximum voltage,
corresponding to one active device being in the triode region and the other device in the cutoff region. The cross-coupled pair does not generate negative conductance in the minima of $\text{Re}(\lambda_0)$, but it adds positive conductance corresponding to resonator loading or $Q$-factor degradation. The amount of $Q$-factor degradation can be qualitatively estimated by how deep the TVRL goes into the LHP for the same voltage swing. The topologies utilizing the two bias inductors limit the $Q$-degradation and suggest better achievable phase noise.

Table 6-II gives a detailed phase noise contribution of the main building blocks at 1-MHz frequency offset. Since the $LC$ resonator and the voltage swing are the same, the resonance tank noise contribution is identical, which allows an evaluation of the oscillators rather than concentrating on the otherwise important properties of the resonator. The topologies using bias inductors have lower phase noise than their competitors. The reasons are two-fold: first is the limited $Q$-factor degradation, and second is the additional noise filtering provided by the two inductors. The limited $Q$-factor degradation is confirmed by comparing the noise contribution of the cross-coupled-pair transistors: for example, the $M_{n1,n2}$ contribution in classic 1L topology is $30.73 \cdot 10^{-15} \cdot V^2/\text{Hz}$, which is reduced to $4.53 \cdot 10^{-15} \cdot V^2/\text{Hz}$ for the 1L+2bL modification. The same conclusions can be drawn by comparing the noise contribution of the PMOS cross-coupled pair. The flicker noise contribution of the active devices is not affected as much, and since it is a few magnitudes lower than the other contributors are, it can be said that the cross-coupled-pair flicker noise is not an issue for optimization. The limited $Q$-factor degradation has also another positive side – a lower bias current is needed to achieve the same voltage swing, which additionally helps achieving better FoM.

The noise filtering realized by the bias inductors can be observed by comparing both the white noise and the flicker noise contribution of the bias network ($M_{\text{BIAS}}$). As the bias noise is greater than the other noise sources, its reduction through the bias inductors has a big impact on the overall phase noise. As the noise filtering is a high-order effect, it is not directly observable on the oscillator TVRL shown in Fig. 6.14(a).

The bottom-biased 1L+2bL oscillator has larger phase noise than the top-biased 1L+2bL oscillator. Although the TVRL trajectories of the two oscillator modifications are essentially the same, which also makes the noise contribution of the cross-coupled transistor similar (Table 6-II), the reason for the phase noise difference is traced back to the bias network. The NMOS bias transistor has the same size as the PMOS bias transistor, which corresponds to larger $g_m$ and larger shot noise for the same bias current. Also, since the product $W*L$ is the same, the NMOS transistor displays higher flicker noise. The increased bias white noise and bias flicker noise contribution in the bottom-biased topologies are confirmed by Table 6-II.
6.7. Oscillator comparison using TVRL

Fig. 6.15. Phase noise for the 1L oscillators with a voltage swing of 1.2V

Fig. 6.16. (a) Pole trajectories for the 2L oscillator modifications with $V_{PP}=1.2V$; (b) $\text{Re}(\lambda_0(t))$ of the 2L oscillators.

6.7.2. 2L oscillator modifications

Fig. 6.16(a) shows the $\lambda_0$ trajectories obtained for the 2L modifications operated with a voltage swing of $V_{PP}=1.2V$, while Fig. 6.16(b) shows $\text{Re}(\lambda_0(t))$ with respect to the oscillation period. The 2L-N modification utilizes a grounded NMOS cross-coupled pair, where the MOS on-resistance in large-signal condition is connected in parallel to the $LC$ resonator, and it has a big impact on the TVRL trajectory. The NMOS transistor goes deep into the triode region with large amplitudes, and in turn, the TVRL trajectory goes deep into the LHP, corresponding to excessive energy loss. The inclusion of the bias inductor helps to minimize the losses in the 2L-N-LBOT topology by limiting the TVRL swing in the LHP. Since the degeneration effect is not visible at the zero crossings, the 2L-N and 2L-N-LBOT topologies create the same maximum negative conductance, and TVRL reaches the same $\max(\text{Re}(\lambda_0))$.

The TVRL of the 2L-P oscillator is reduced from both the positive and negative side compared to the 2L-N oscillator. The reduction of the positive TVRL is due to the smaller PMOS $g_m$. The reduction of the negative TVRL is due to the degeneration of the current mirror, which limits the resonator loading. At large voltage swings, however, the voltage headroom over the current mirror is reduced and the $M_{p3}$ transistor may enter the triode region. The
degeneration of the cross-coupled pair is significantly reduced when $M_{p3}$ enters the triode region, which causes an abrupt drop of $\text{Im}(\lambda_0)$ seen in the 2L-P TVRL (the red curve in Fig. 6.16(a)). The abrupt drop of $\lambda_0$ is avoided by using the bias inductor $L_{\text{TOP}}$, which makes the degeneration of the cross-coupled pair almost insensitive to the voltage headroom over $M_{p3}$.

Table 6-III gives a detailed contribution of the oscillator building blocks at 1-MHz offset frequency. Again, the topologies utilizing bias inductors display better phase noise due to $Q$-factor preservation and due to additional noise filtering of the bias network. The $Q$-factor deterioration is directly observed on the TVRL plot, while the noise filtering is not. The $Q$-factor preservation obtained with the bias inductors is confirmed by comparing the noise contributed by the switching pair ($M_{n1,n2} / M_{p1,p2}$) for the cases with and without inductors. The bias noise filtering provides additional benefits for achieving low phase noise. The 2L-P topology has lower white and flicker noise contributed by the cross-coupled pair due to the lower MOS transconductance and lower $K_f$ compared to the 2L-N topology.

The phase noise comparison here validates the conclusions drawn from the TVRL trajectories for the contribution of the cross-coupled pair. However, as was pointed out earlier, high-order effects such as noise filtering should be evaluated separately.
6.7. Oscillator comparison using TVRL

The \( \lambda_0 \) trajectories of the D-Colpitts are shown in Fig. 6.18(a) for three voltage swings, while Fig. 6.18(b) shows the voltage swings and the corresponding \( \text{Re}(\lambda_0(t)) \) for one oscillation period. As outlined in Subchapter 6.5, the active transistors spend a long time in active region, which corresponds to a little variation of their small-signal parameters and in smaller TVRL trajectories compared to the 1L and 2L oscillators. The cancelling effect of the transistor nonlinearities also contribute to the small trajectories, as outlined in Subchapter 6.3.4. The main transistors behave differently during the rise and fall time of the oscillator waveform, because of the asymmetric transistor bias trajectory shown in Fig. 6.13. The asymmetry affects the \( \lambda_0 \) trajectories and it is seen as the maxima of \( \text{Re}(\lambda_0) \) are being shifted from the oscillator zero-crossings. The minima of \( \text{Re}(\lambda_0) \) occurs close to the extrema of the oscillator voltage, but with a phase shift. The asymmetric phase shift depends both on the capacitive feedback ratio and on the voltage swing (Fig. 6.18(b)).

The D-Colpitts phase noise is shown in Fig. 6.19 for three voltage swings and Table 6-IV gives the corresponding noise contribution at 1-MHz offset frequency. Increasing the voltage...
swing in D-Colpitts only slightly improves the oscillator phase noise since as the voltage swing grows, the active transistors $M_{n1}$ and $M_{n2}$ start to leave the active region, resulting in increased white noise. At the same time, the TVRL becomes more asymmetric (Fig. 6.18(a)), which increases the AM-PM conversion of flicker noise. The increased AM-PM conversion is confirmed in Fig. 6.19 and by comparing the bias noise in Table 6-IV.

### 6.8. Analysis of the TVRL specifics in VCOs

This subchapter evaluates the $\lambda_0$ trajectories in Voltage-Controlled Oscillators (VCO) and compares them against the $\lambda_0$ trajectory of an oscillator. The VCO is usually built by adding a varactor block in parallel to the oscillator’s resonance tank $L_OC_O$. The standard 1L oscillator topology in Fig. 6.1(a) is used for evaluating the TVRL specifics in VCOs.

#### 6.8.1. Varactor block and its modeling

The varactor structure employed for this investigation is shown in Fig. 6.20(a) [P.2]. The varactor structure uses differentially-connected PMOS varactors with $dc$-decoupling network $C_dR_d$, where the varactor gate is $dc$-biased to ground with $R_{d1,2}$, and the control voltage $V_C$ varies the potentials of the PMOS drain and source. The small-signal model representing the varactor block for the TVRL computations is shown in Fig. 6.20(b), where $C_{v1,2}$ and $r_{v1,2}$ are time-varying passive components modeling the varactor capacitance and series resistance. The extraction of the time-varying $C_{v1,2}$ and $r_{v1,2}$ is done prior to the TVRL computation, where each varactor is represented with its quasi-static model [156] and additional terminal resistances. The quasi-static model parameters for the varactor are obtained in the same way as the active transistors of the oscillator core [P.3].

The extraction of $C_v$ and $r_v$ is done by computing the varactor impedance $Z_v$ at the gate of the MOS device with its drain, source, and bulk terminals being $ac$-grounded ($V_{DD}$ and $V_C$ are ideal voltage sources). An automatic model extraction composes a varactor circuit description in the form of $Y = G + sB$ and computes the varactor impedance $Z_v$ at a given frequency. The

---

**Table 6-IV: Noise contribution @ 1MHz offset for the Differential Colpitts (VDD=1.5V; $10^{-15}$V$^2$/Hz)**

<table>
<thead>
<tr>
<th></th>
<th>$V_{PP}=1.0\text{V}$</th>
<th>$V_{PP}=1.2\text{V}$</th>
<th>$V_{PP}=1.5\text{V}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{n1,n2}$ (flicker)</td>
<td>0.67</td>
<td>0.97</td>
<td>1.95</td>
</tr>
<tr>
<td>$M_{n1,n2}$ (white)</td>
<td>48.14</td>
<td>50.82</td>
<td>54.37</td>
</tr>
<tr>
<td>$M_{BIAS}$ (flicker)</td>
<td>7.61</td>
<td>11.24</td>
<td>22.64</td>
</tr>
<tr>
<td>$M_{BIAS}$ (white)</td>
<td>45.01</td>
<td>50.98</td>
<td>60.87</td>
</tr>
<tr>
<td>PN1M$_{TOTAL}$</td>
<td>-119.9</td>
<td>-121.2</td>
<td>-122.4</td>
</tr>
<tr>
<td>$I_{DD}$ (mA)</td>
<td>4.89</td>
<td>5.44</td>
<td>6.48</td>
</tr>
<tr>
<td>FoM</td>
<td>183.1</td>
<td>183.9</td>
<td>184.3</td>
</tr>
</tbody>
</table>
6.8. Analysis of the TVRL specifics in VCOs

Varactor block: (a) schematic; (b) small-signal model representing the varactor block in the TVRL computations

![Varactor block](image)

**Fig. 6.20.**

**Fig. 6.21.** Deviation when extracting the varactor equivalent model components $C_v$ and $r_v$. The deviation is normalized for $f_{\text{extr}} = 4\, \text{GHz}$.

Varactor equivalent parameters are

\[
\begin{align*}
    r_v &= \Re(Z_v), \quad (6.11) \\
    C_v &= -1/(2\pi f_{\text{extr}} \cdot \Im(Z_v)), \quad (6.12)
\end{align*}
\]

where $\Re(Z_v)$ and $\Im(Z_v)$ are respectively the real and imaginary part $Z_v$. The computation is done for all data points within the oscillation period. An extraction frequency $f_{\text{extr}}$ of $4\, \text{GHz}$ is used for the initial $r_v$ and $C_v$ modeling, which is close to the oscillation frequency of the investigated VCO. Although the parameters $r_v$ and $C_v$ are frequency dependent, their relative variation over the frequency band of interest is less than 0.1% under various voltage swings and control voltages (see Fig. 6.21). This small variation is further reduced when referred to root computation, since the varactor block is connected in parallel with the tank capacitance $C_0$ and $C_0$ is dominantly determining the oscillation frequency.

An iterative procedure for adjusting $f_{\text{extr}}$ is adopted in order to bring the oscillation and extraction frequency closer. The performance of the iterative procedure is demonstrated in Fig. 6.22. The extraction frequency $f_{\text{extr}}(t)$ is corrected for each consecutive run, depending on the calculated $\lambda_0(t)$ from the previous step. The initial computation (#0) uses constant $f_{\text{extr}} = 4\, \text{GHz}$ and the deviation between $\lambda_0(t)$ and $f_{\text{extr}}(t)$ practically vanishes after 2-3 iterations (Fig. 6.22(a)).
Fig. 6.22. Performance of iterative procedure for adjusting \( f_{\text{extr}} \): (a) deviation between \( f_{\text{extr}} \) and \( \lambda_0 \) depending on the number of iterations; (b) \( \lambda_0(t) \) deviation from its correct value depending on the number of iterations

Fig. 6.22(b) shows that even without any iteration, the error of the computed root \( \lambda_0(t) \) is less than \( 10^{-6} \) GHz, and it goes below \( 10^{-12} \) GHz after the third iteration. Despite the small error when using fixed \( f_{\text{extr}} \), a five-step iterative procedure is used for obtaining precise TVRL trajectories presented below.

6.8.2. Time-varying varactor capacitance and its impact on the TVRL and phase noise

Fig. 6.23(a) and (b) show the equivalent capacitance \( C_{\text{V,eq}} = (C_{V1} \parallel C_{V2}) \) seen by the resonator for various control voltages obtained for 1.2-V \( \text{pp} \) and 1.5-V \( \text{pp} \) voltage swing respectively. The time-varying \( C_{\text{V,eq}} \) depends on the resonator voltage swing, because a scaled and dc-shifted version of the output voltage is applied to the varactor gate. An effective varactor capacitance for each control voltage determines the oscillation frequency, as it is known that the oscillator voltage swing has an effect on the frequency tuning range [70], [96], [97]. Increasing the voltage swing forces \( C_{\text{V,eq}} \) to change quicker between its maximum and minimum value. The large swing introduces variations of the varactor capacitances even for control voltages where the varactor small-signal C-V curve is flat (in the beginning and at the end of the tuning range), which is known as a bias-dependent frequency tuning [97].

The variation of \( C_{\text{V,eq}} \) for different \( V_C \) occurs at different instants along \( T_{\text{OSC}} \), which affects the oscillator phase noise. In the beginning and at the end of the tuning range \( C_{\text{V,eq}} \) varies mostly around the extrema of the voltage swing – \( \pi/2 \) and \( 3\pi/2 \) (0, \( \pi \), and \( 2\pi \) are the voltage zero-crossings). Since the oscillator is less sensitive around \( \pi/2 \) and \( 3\pi/2 \), less noise is transformed to phase noise due to AM-PM conversion. On the other hand, \( C_{\text{V,eq}} \) changes rapidly around \( \pi \) and \( 2\pi \) for \( V_C \) in the range of 0.3-V – 0.7-V, thus producing higher AM-PM conversion. Although the above results are generally known, the added value of the time-
6.8. Analysis of the TVRL specifics in VCOs

Fig. 6.23. Equivalent time-varying varactor capacitance \( C_{V1||V2} \) seen by the main resonator of the 1L-VCO for different \( V_C \) at: (a) \( V_{PP} = 1.2V \); (b) \( V_{PP} = 1.5V \).

varying varactor investigation is the recognition that \( C_{V,eq}(t) \) changes rapidly around the zero-crossing in the middle of the tuning range, thus increasing the noise sensitivity of the oscillator.

The obtained TVRL trajectories of the 1L-VCO are shown in Fig. 6.24(a) for five control voltages. The trajectories look similar to the trajectory of the native oscillator (Fig. 6.14(a)), but their behavior along the frequency tuning range has certain specifics. The \( \lambda_0 \) trajectory would simply move along the imaginary axis of the \( s \)-plane depending on the control voltage \( V_C \) if the varactor capacitance were time-invariant. However, since \( C_{V,eq} \) is time-(voltage-) dependent (Fig. 6.23), the TVRL changes its shape. \( C_{V,eq} \) can be assumed constant only for \( V_C \approx 0V, 0.4V, \) and 1.2V, and it is seen from Fig. 6.24(a) that these TVRLs have almost the same shape, but are shifted in frequency. The \( \lambda_0 \) trajectory for \( V_C=0.2V \) comes closer to the 0-V trajectory in the RHP, but it comes closer to the 0.4-V trajectory in the LHP. The distorted TVRL shape for \( V_C=0.2V \) is due to the time-varying \( C_{V,eq} \), which has a smaller capacitance value around the zero-crossing and larger capacitance around the voltage extrema. Since the same physical effect causes AM-PM phase noise conversion, the AM-PM effect can be evaluated through the TVRL distortion from its nominal trajectory. Similarly, the 0.6-V trajectory comes close to the 1.2-V trajectory in the RHP, and close to the 0.4-V trajectory in the LHP.

Following the discussion above, the AM-PM conversion of flicker noise can be evaluated using the distorted TVRL. As the TVRL trajectory obtained for \( V_C=0.4V \) is nearly the same as the one of the native oscillator (but shifted in frequency), one can conclude that the AM-PM conversion is minimized and good phase noise can be obtained around \( V_C=0.4V \). It was shown in [70] that such an optimum exists and it can be confirmed with SpectreRF simulations. The 1L-VCO phase noise at 10-kHz frequency offset, which is mostly governed by flicker noise, is shown in Fig. 6.24(b), confirming that an optimum close-in phase noise can be obtained in the middle of the tuning range where the TVRL trajectory resembles the trajectory of the native
oscillator. The phase noise optimum is achieved around $V_C=0.6\,\text{V}$, which means that the time-varying intrinsic capacitances of the native oscillator at $V_C=0.4\,\text{V}$ create visible AM-PM conversion, while they are compensated with the varactor capacitance at around $V_C=0.6\,\text{V}$.

The effect of the varactor on the TVRL is similar for all the oscillator topologies presented above when they are used for building a VCO.

### 6.9. Summary and contributions

The comparative study on GHz-range LC oscillators presented in this paper is meant to be used as a guideline for oscillator topology selection. The topology comparison is based on the TVRL method with conclusions that are verified with Cadence SpectreRF simulations. The main focus of this work is on the treatment of the TVRL trajectories in different oscillators provided with links to the physical process that are known from the literature.

The start-up process, phase noise performance, and TVRL trajectories for the investigated oscillator modifications were presented in detail. The TVRL behavior is linked to the physical processes inside the oscillator to demonstrate its analytical capabilities. In addition, the oscillators’ TVRL were first evaluated with simplified large-signal models that help in understanding the processes of the complete oscillators. Subchapter 6.8 outlined the TVRL specifics in VCOs that are linked to the time-varying varactor capacitance, and its cumulative effect on the VCO performance.

2L oscillator topology is more suitable for low-voltage application compared to 1L topology, but it requires higher current consumption. In both 1L and 2L oscillators, the large-signal oscillator operation drives the active devices in the triode region, causing $Q$-factor degradation. The $Q$-factor can be partly preserved by using appropriate biasing scheme or bias...
inductors, where the former is silicon-hungry but provides better phase noise performance. The active transistors in the D-Colpitts topology operate with lower voltages for the same voltage swing, suggesting advantages in high-voltage applications, or high-swing generation with low-breakdown-voltage transistors. The TVRL is found usable in recognizing the AM-PM noise conversions in VCOs.

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The contributions of the work presented in this chapter are:

1. A comparison between various modifications of LC oscillators is made using the TVRL method presented in the previous chapter. The comparison reveals physical phenomena associated with large-signal oscillator. The root trajectories are linked with the behavior of simplified oscillator models for which the root trajectories are described analytically.

2. The TVRL method is applied for the analysis of Voltage-Controlled Oscillators by including the effect of the time-varying (large-signal) varactor capacitances on the root trajectory. The TVRL evaluation in VCOs reveals the optimum point in the analog tuning range that minimizes flicker noise up-conversion.
Chapter 7

Evaluation of Parasitic Components in \( LC \) Oscillators by TVRL

7.1. Introduction

The phase noise performance of low-noise \( LC \) oscillator is mainly limited by the quality factor of the passive components in the resonance tank. In practical applications, however, the parasitic components arising from the physical design also deteriorate visibly the oscillator performance. The undesired effects caused by the parasitic components cannot be estimated accurately by using root-locus analysis based on a closed-form solution of the characteristic equation. The investigation of root trajectories using closed-form equation is typically applied to a second-order characteristic polynomial, but the inclusion of parasitic components increases the polynomial order, thus making the numerical methods the only good choice. The precise numerical simulations obtained with SpectreRF bring important numerical information, but certain design insights are lost.

This chapter utilizes the TVRL method presented in Chapter 5 ([P.3]) to bring visual insights to the designer that would allow easier understanding on the physical processes involved, and would allow performance optimization. The main goals of this investigation are to demonstrate the applicability of the TVRL method for analyzing small parasitic components, and to extend the interpretation of the \( \lambda_0 \) trajectory departures caused by the known effects of parasitic components on the oscillator behavior. The VCO reported in Chapter 4 ([P.2]) is used as a test-bench for this investigation, whose measured phase noise is in good agreement with extracted SpectreRF simulations. The simulated phase noise is used for comparing the parasitic components, whose effect is small enough to be measured reliably.

The small-signal equivalent circuit of the VCO (Fig. 10.1) and the corresponding circuit matrices used for computing the oscillator roots are presented in Appendix A. Subchapter 7.2 describes the oscillator parasitic components evaluated here and discusses the issues related to the computation precision and error growth when the circuit matrices become large. Subchapter
7.3 presents the TVRL trajectories obtained with the evaluated parasitic components, relates the trajectory behavior to oscillator physical processes, and derives conclusions for the oscillator operation.

### 7.2. Parasitic components in LC oscillators

#### 7.2.1. Oscillator with included parasitic components

The analysis capabilities of the TVRL method are demonstrated in cases where small parasitic components can visibly deteriorate the oscillator phase-noise performance. These parasitic components can be due to layout (parasitic resistances and capacitances), or due to modeling uncertainties (for instance gate resistance of MOS devices). The modeling uncertainties are tightly coupled to the actual device layout, where RF performance improvement can be obtained with different MOS transistor layout [74], [144]. The MOS device models and parasitic components are hard to be predicted before the physical design of the oscillator itself, thus they are seen as uncertainties during the electrical design.

Fig. 7.1(b) shows the layout of the VCO reported in Chapter 4, where two critical parasitic components ($C_{bot}$ and $r_L$) that deteriorate the oscillator performance are shown. Both parasitic components arise from the physical design of the VCO, and in general, they should be minimized. The parasitic capacitance $C_{bot}$ shifts the resonance frequency of the filtering.
7.2. Parasitic components in LC oscillators

Fig. 7.2. Error estimation of the main root computation for the different parasitic components

Table 7-I: Computation accuracy for different parasitics

<table>
<thead>
<tr>
<th>par</th>
<th>NG,B</th>
<th>N(λ)</th>
<th>R_{\text{norm, opt}}</th>
<th>R_{\text{norm}}</th>
<th>\kappa^{-1}@R_{\text{norm}}</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{\text{bot}}</td>
<td>19</td>
<td>16</td>
<td>22.0 – 28.0</td>
<td>25</td>
<td>1.113</td>
</tr>
<tr>
<td>r_L</td>
<td>21</td>
<td>16</td>
<td>27.5 – 32.5</td>
<td>30</td>
<td>1.282</td>
</tr>
<tr>
<td>r_{\text{gate}}</td>
<td>25</td>
<td>22</td>
<td>32.5 – 36.5</td>
<td>35</td>
<td>1.475</td>
</tr>
</tbody>
</table>

network and deteriorates the oscillator phase noise. The parasitic resistance r_L represents the interconnect resistance between the main inductor L_{\text{MAIN}} and the VCO capacitor bank, which degrades the tank Q-factor and leads again to worse phase noise.

In addition to the layout-related parasitic components, this chapter evaluates the effect of the MOS gate resistance. This resistance is often included in RF model of MOS device, which is not included in the standard quasi-static model. Realistic in value gate resistor is added to each MOS transistor, which is in the range of 0.5-15Ω and its value depending on the transistor geometry.

7.2.2. Error estimate and optimum normalization resistance

The inclusion of the parasitic component in the small-signal model increases the size of the matrices G and B, which may worsens the computation accuracy of the oscillator poles. As shown in [P.3], the computation accuracy can be improved using the normalization resistance R_{\text{norm}}. Fig. 7.2 and Table 7-I summarize the effects of including the parasitic components on the condition number associated with λ₀. The inclusion of the capacitor C_{\text{bot}} in the G and B matrices does not increase their size, and the optimum R_{\text{norm}} is the same as the one without parasitic components. On the other hand, the parasitic resistances r_L and r_{\text{gate}} increase the size of the matrices and worsen the computation accuracy, which is seen in Fig. 7.2 with the blue and the red line coming above the black line. In both cases, the condition number is slightly increased when computing the main pole, but still the computation precision is good. The root
computation for each parasitic component case is done with the corresponding $R_{\text{norm, opt}}$ listed in Table 7-I.

### 7.3. Oscillator behavior with parasitic components

This subchapter evaluates the parasitic components effect on the TVRL trajectories and on the oscillator phase-noise performance. As the parasitic components affect the oscillation amplitude, the amplitude is being adjusted with the bias current $I_B$ such that it remains constant over the resonator remains at 1.2-Vpp level for all test cases. Each parasitic component is evaluated separately for three different values and compared against the oscillator without parasitics in order to trace the trend of the TVRL trajectory departure. The range of values of the parasitic components is realistic and the range is selected such that it causes visible but small TVRL trajectory departure. In reality the change of some parasitic components might be correlated with other parasitics – for instance changing the MOS transistor geometry affects both the gate resistance and the MOS capacitances [74]. However, a correlated change was not adopted in this investigation in order to clearly distinguish the effect of each component on the TVRL. The goal of such investigation is to give design guidelines before the physical design of the oscillator have started, while a precise TVRL trajectory including all parasitic components can be obtained after extraction of the final layout.

It is generally known that the parasitic components should be minimized during the physical implementation of an RF oscillator to improve its performance. The known effects of the parasitic components facilitate the treatment of the TVRL trajectories and help to understand the source of TVRL departures in deeper details.

The TVRL trajectory for each parasitic component is obtained with the optimum normalization resistance as given in Table 7-I in order to provide maximum computation accuracy. The comparison summarizes the oscillator phase noise obtained with SpectreRF, the TVRL trajectory in the $s$-plane, and the time-domain variation of the main pole with respect to the oscillator swing.

#### 7.3.1. Parasitic capacitance $C_{\text{bot}}$

The parasitic capacitor $C_{\text{bot}}$ is added to the $v_{\text{bot}}$ node in the small-signal equivalent circuit of the oscillator shown in Fig. 7.1(a). Three values are used in this investigation: 50fF, 100fF, and 200fF. The resulting TVRL trajectories for these capacitances are shown in Fig. 7.3(a), where increasing $C_{\text{bot}}$ reduces the $\lambda_0$ trajectory in the LHP and RHP. The time-domain waveform of the oscillator ($v_{\text{outL}}$ and $v_{\text{bot}}$ node) are shown in Fig. 7.4 with respect to the obtained real part of
7.3. Oscillator behavior with parasitic components

The increase of the \( C_{\text{bot}} \) capacitance has two effects on the oscillator performance. First, as the resonance frequency of the biasing network is shifted with \( C_{\text{bot}} \), the degeneration impedance of the cross-coupled pair is reduced and the oscillator produces larger voltage swing. Therefore, \( I_B \) is decreased until the target 1.2-Vpp swing is achieved, which also affects the swing of \( \text{Re}(\lambda_0) \) in the LHP and RHP being the smallest for \( C_{\text{bot}} = 200 \text{fF} \). The most positive \( \text{Re}(\lambda_0) \) is typically achieved around the voltage zero-crossing where the MOS transistor generates the maximum negative conductance, while the most negative \( \text{Re}(\lambda_0) \) is obtained near the maxima/minima of the voltage swing with virtually no negative conductance and maximum resonator loading. As it is described in Subchapter 5.4, the phase noise is reduced by minimizing the swing of \( \text{Re}(\lambda_0) \) in the LHP and RHP, since increased \( \text{Re}(\lambda_0) \) in the LHP correspond to resonator loading, while increased \( \text{Re}(\lambda_0) \) in the RHP denotes excessive generation of negative conductance, and both effects deteriorate the oscillator phase noise.

Second, the time-domain waveform of the \( v_{\text{bot}} \) node shows asymmetric distortions with respect to the zero-crossing of the \( v_{\text{outL}} \) voltage (Fig. 7.4(b)) when \( C_{\text{bot}} \) is increased. Thus, the increase
CHAPTER 7: EVALUATION OF PARASITIC COMPONENTS IN LC OSCILLATORS BY TVRL

Fig. 7.5. Harmonic contents of the output voltage depending on the $C_{bot}$ parasitic capacitance.

Table 7-II: $C_{bot}$ capacitance comparison ($V_{pp}=1.2V$)

<table>
<thead>
<tr>
<th>$C_{bot}$</th>
<th>$I_{DD}$ (mA)</th>
<th>$f_{osc}$ (GHz)</th>
<th>PN, (dBc/Hz) @</th>
<th>100k</th>
<th>1M</th>
<th>10M</th>
<th>100M</th>
</tr>
</thead>
<tbody>
<tr>
<td>no par</td>
<td>3.954</td>
<td>-100.2</td>
<td>-148.9</td>
<td>-168.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50fF</td>
<td>3.949</td>
<td>-97.9</td>
<td>-124.1</td>
<td>-148.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100fF</td>
<td>3.935</td>
<td>-96.2</td>
<td>-124.1</td>
<td>-148.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200fF</td>
<td>3.952</td>
<td>-93.8</td>
<td>-122.2</td>
<td>-146.9</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

of $C_{bot}$ from one hand reduces the swing of Re($\lambda_0$) in the LHP and in the RHP suggest less thermal noise [P.3], but on the other hand introduces asymmetry which rises the AM-PM conversion of flicker noise [64]. The asymmetry caused by the $C_{bot}$ capacitance is confirmed by the harmonic content of the output voltage shown in Fig. 7.5, where the second harmonic increases with 7.3 dB and the fourth harmonic increases as much as 12.5 dB when $C_{bot}$ is increased from zero to 200 fF.

Fig. 7.3(b) shows the simulated with SpectreRF oscillator phase noise, while Table 7-II gives a numerical summary of the obtained results. As it is clear from Fig. 7.3(b), the AM-PM flicker noise up-conversion has dominant effect for low-to-medium frequency offsets, which is vanishing for far-away frequency offset (>10 MHz). The effect of the reduced Re($\lambda_0$) swing becomes visible at 100-MHz offset, where the AM-PM conversion is diminished, and the larger $C_{bot}$ capacitance provides slightly better oscillator phase noise.

The TVRL method in this test scenario shows the sensitivity and the analysis capabilities of the method. The root trajectory clearly highlights the unsymmetrical behavior of the oscillator that cause AM-PM conversion, and also shows the expected better phase noise as soon as the AM-PM effects diminishes.
As Table 7-II shows, increasing the parasitic capacitance $C_{bot}$ reduces the power consumed by the VCO for a given voltage swing. The power consumption is reduced thanks to the decreased degeneration impedance seen by the cross-coupled NMOS pair, which helps to generate the same negative resistance with smaller bias current. Although the reduced power consumption comes at the price of worse phase noise in the $1/f^3$ region, this phenomenon can be utilized in low-power VCO design. Similar effect has been utilized for building high-performance Class-C VCO [110], which converts more efficiency the bias current into a voltage swing.

On the layout shown in Fig. 7.1(b) the auxiliary inductor $L_{bot}$ is placed in close proximity with the NMOS transistors in order to minimize the $C_{bot}$ capacitance, since achieving low phase noise was the primary goal of the reported VCO prototype.

### 7.3.2. Parasitic resistance $r_L$

Fig. 7.6(a) shows the TVRL trajectories obtained with interconnect parasitic resistance of 25mΩ, 50mΩ, and 100mΩ. This resistance represents a $Q$-factor degradation caused by the finite distance between the tank inductor $L_{MAIN}$ and the tank capacitors $C_o$. The respective $Q$-factor of the inductors drops from 29.8 (no parasitic $r_L$) down to 27.9, 26.3, and 23.5 for $r_L$ equal to 25mΩ, 50mΩ, and 100mΩ respectively. The resulting $Q$-factor of the resonator is 16.4, 15.9, and 14.9, which is nominally 16.9. The corresponding node voltages of the oscillator ($v_{outL}$ and $v_{bot}$) are shown in Fig. 7.7 with respect to $\text{Re}(\lambda_0)$, where no significant waveform changes are observed.

The TVRL results obtained here are similar to the $Q$-factor degradation analysis presented in [P.6], where the $Q$-factor of the tank was investigated by varying the $Q$-factor of the tank capacitor. The approach applied here represents more physical reason for this $Q$ degradation. As seen from Fig. 7.6(a), the TVRL trajectories swing slightly deeper into the LHP and RHP when the tank $Q$-factor is deteriorated. In addition, the imaginary part of the $\lambda_0$ trajectory shifts.

![Fig. 7.6.](image)

(a) TVRL trajectories as a function of the interconnect resistor $r_L$; (b) the corresponding simulated phase noise around 10-MHz offset.
down, which suggests lower oscillation frequency. Similar to the discussions in Subchapter 7.3.1, the increased swing of \( \text{Re}(\lambda_0) \) suggests more noise generated inside the oscillator, which respectively leads to worse phase noise. The phase noise of the oscillator is presented in Fig. 7.6(b) with numerical values summarized in Table 7-III. The SpectreRF simulations confirm the observations seen from the TVRL trajectories. The waveform distortions observed in the \( C_{\text{bot}} \) capacitance case are not seen here (comparing Fig. 7.4 and Fig. 7.7), thus the amount of AM-PM noise up-conversion is similar for all \( r_L \) test cases. The output harmonic content is largely independent on the \( r_L \) parasitic resistance having minor reduction of the second and fourth harmonic (in order of 0.5 dB). This harmonic reduction is seen in Fig. 7.6(a) by the slightly reduced enclosing area by the \( \lambda_0 \) trajectory. This second-order effect is due to more symmetrical waveforms (Fig. 7.7) that may slightly reduce the AM-PM conversion of flicker noise. This observation is confirmed by the SpectreRF phase noise obtained at close-in offset frequencies (Table 7-III).

| Table 7-III: Interconnect resistance comparison (\( V_{PP}=1.2V \)) |
|---------------|-------|--------|----------------|----------------|----------------|
| \( r_L \)     | \( I_{DD} \) | \( f_{osc} \) | PN, (dBc/Hz) @ | 100k | 1M | 10M | 100M |
| no par | 3.954 | 4.206 | -100.2 | -126.7 | -148.9 | -168.3 |
| 25mΩ | 4.141 | 4.205 | -100.5 | -126.7 | -148.8 | -168.1 |
| 50mΩ | 4.300 | 4.205 | -100.6 | -126.7 | -148.6 | -168.0 |
| 100mΩ | 4.626 | 4.203 | -100.9 | -126.7 | -148.4 | -167.7 |

The existence of interconnect resistance \( r_L \) directly affects the resonator \( Q \)-factor and it requires additional VCO power consumption to compensate the increased losses (Table 7-III). Thus, \( r_L \) should be minimized as much as possible during the physical design, since it deteriorates the VCO performance and increases the power consumption. In the layout shown in Fig. 7.1(b), the resonance inductor \( L_{\text{MAIN}} \) is placed as close as possible to the capacitor bank in order to minimize \( r_L \) and consequently to improve the oscillator phase noise.
7.3. Oscillator behavior with parasitic components

Fig. 7.8. (a) TVRL trajectories as a function of the MOS gate resistance; (b) the corresponding simulated phase noise around 10-MHz offset.

Fig. 7.9. Time domain waveforms showing the effect of the MOS gate resistances: (a) oscillator node voltage; (b) $v_{bot}$ node voltage; (c) real part of $\lambda_0(t)$.

7.3.3. MOS gate resistance

Fig. 7.8(a) shows the TVRL trajectories obtained with included MOS gate resistance, which is often included in a RF models to represent accurately the high-frequency limitation of the CMOS process. In this investigation, a gate resistor is added to each MOS device. The value of the gate resistance is calculated based on process-specific parameters and depending on the transistor geometry e.g. the gate resistance associated with the PMOS cross-coupled pair is half of the gate resistance for the NMOS cross-coupled pair. The six extra resistors increase the size of the matrices by 6; and $R_{\text{norm}} = 35\, \Omega$ is used in the root computation (Table 7-I).

The effect of the MOS gate resistance is evaluated by scaling all resistance to half their nominal value, their nominal value, and double of their nominal value. Increasing the MOS gate resistance reduces the negative conductance generated by the cross-coupled pairs, and more biasing current is needed to achieve the same voltage amplitude over the resonator. Similarly to the interconnect resistance $r_L$, increasing the gate resistance and keeping the amplitude constant forces the TVRL to swing deeper into the LHP and RHP, thus causing worse phase noise in the $1/f^2$ region. Fig. 7.9 shows the oscillator node voltages ($v_{outL}$ and $v_{bot}$) with respect to Re($\lambda_0$),
showing that the MOS gate resistance has no effect on the waveform asymmetry, and consequently no phase noise change should be observed in the $1/f^3$ phase noise region. No significant deviations are observed in the output harmonics when varying the MOS gate resistance. Fig. 7.8(b) presents the obtained with SpectreRF phase noise confirming the conclusion derived above, and Table 7-IV gives the numerical summary of the experiment.

<table>
<thead>
<tr>
<th>$r_{gate}$</th>
<th>$I_{DD}$ (mA)</th>
<th>$f_{osc}$ (GHz)</th>
<th>PN, (dBc/Hz) @ 100k</th>
<th>PN, (dBc/Hz) @ 1M</th>
<th>PN, (dBc/Hz) @ 10M</th>
<th>PN, (dBc/Hz) @ 100M</th>
</tr>
</thead>
<tbody>
<tr>
<td>no par</td>
<td>3.954</td>
<td>4.206</td>
<td>-100.2</td>
<td>-126.7</td>
<td>-148.9</td>
<td>-168.3</td>
</tr>
<tr>
<td>($r_{gate}$)*0.5</td>
<td>4.048</td>
<td>4.204</td>
<td>-100.1</td>
<td>-126.5</td>
<td>-148.7</td>
<td>-168.1</td>
</tr>
<tr>
<td>($r_{gate}$)*1</td>
<td>4.125</td>
<td>4.202</td>
<td>-100.0</td>
<td>-126.4</td>
<td>-148.5</td>
<td>-167.9</td>
</tr>
<tr>
<td>($r_{gate}$)*2</td>
<td>4.302</td>
<td>4.199</td>
<td>-100.0</td>
<td>-126.2</td>
<td>-148.1</td>
<td>-167.5</td>
</tr>
</tbody>
</table>

The inclusion of the MOS gate resistance requires more VCO power to achieve the same voltage swing (Table 7-IV). This effect is due to the reduced gain of the MOS transistor caused by the finite gate resistance. Thus, a low-power VCO design should seek possibilities to reduce this parasitic component by physical layout or by transistor sizing. A multi-finger transistor configuration is adopted in the layout shown in Fig. 7.1(b), which a common technique for reducing MOS gate resistances at high frequencies.

### 7.4. Conclusions

This chapter evaluates the effect of parasitic components on the performance of LC oscillators using Time-Varying Root-Locus. The chapter described the formation of the circuit-description matrices used in the TVRL computation, and the respective assessment of root computation accuracy. The evaluation shows the link between the obtained root trajectories and physical circuit phenomena caused by parasitic components that are related to practical VCO implementation.

The analysis presented here goes beyond the possibility to analyze oscillators with closed-form root-locus methods, and requires computer-aided tools. The SpectreRF simulator accurately takes all parasitic components into account and gives accurate phase noise result, but due to its numerical nature it is difficult to decouple the complex reasons for a given oscillator behavior. Instead, the oscillator behavior can be analyzed in deeper details when the SpectreRF results are combined with the TVRL trajectories. This paper shows that the amount of TVRL swing into the LHP and RHP gives information about the noise generated into the circuit itself. On the other hand, the asymmetry of the $\lambda_0$ trajectory gives information about the amount of
AM-PM conversion, which becomes a second-order effect being captured by the TVRL method.

7.5. Summary and contributions

The material presented in this chapter form a journal publication printed in the Journal of Low-Power Electronics [P.5]. The material from [P.5] is reused in this chapter with the kind permission of American Scientific Publishers, © 2011 American Scientific Publishers. The research has been financed by Tampere Doctoral Program in Information Science and Engineering (TISE), Tampere, Finland.

The contribution of the work presented in this chapter is:

1. It is demonstrated that the TVRL method is able to analyze oscillator circuits with small parasitic components via the root-locus trajectory. Similar evaluation with handheld analysis is impossible due to circuit size and limited analysis precision.
Chapter 8

Q-factor degradation analysis using TVRL

The phase noise performance of a LC oscillator heavily depends on the $Q$-factor of the resonator through the Leeson’s equation, as described in Subchapter 1.5. However, most of the theoretical phase noise analyses require prior knowledge of the resonator’s $Q$-factor, and they assume that the $Q$-factor is constant and independent from the oscillator operation. It was recognized in [69] that the resonator’s $Q$-factor is degraded under large-signal conditions, but no estimate for the degraded $Q$-factor was given. Reference [127] shows a procedure for estimating the oscillator quality factor, but the proposed procedure still has problems when the positive and negative admittances of a parallel $LC$ tank are perfectly balanced. Subchapter 1.5.1 gives a detailed description of the methods evaluating the effective resonator $Q$-factor.

This chapter describes an extraction of the effective oscillator $Q$-factor in cross-coupled $LC$ oscillators using the TVRL method. The proposed methodology permits to investigate the $Q$-factor degradation mechanisms in $LC$ oscillators, to compare oscillator topologies in terms of $Q$-factor, and it proves the usability of the TVRL concept.

8.1. Preliminaries

8.1.1. Poles of $RLC$ tank

The complex-conjugated pair of the second-order $RLC$ tank shown in Fig. 8.1 is

$$\lambda_{1,2}(t) = -\frac{G_0(t)}{2C_0(t)} \pm j \sqrt{\frac{1}{L_0 C_0(t)} - \frac{G_0^2(t)}{4C_0^2(t)}},$$

where the conductance $G_0(t)$ and the capacitance $C_0(t)$ could be time-varying. The degree of $C_0$ variation is governed by the ratio between voltage-dependent and voltage-independent capacitors, whereas the $G_0$ variation is caused by active device nonlinearities. The inductance $L_0$ used in the oscillator’s resonance tank does not change under large-signal oscillator conditions (as long as $L_0$ is realized by a coil) and it is considered time-invariant in this analysis. Given that the main complex-conjugated pair $\lambda_{1,2}$ is computed (by TVRL) and the value of the
Fig. 8.1.  *RLC* tank and the corresponding complex-conjugated pole with positive imaginary part.

Fig. 8.2.  Pole departure after adding admittance $Y'$ to an *RLC* tank

Inductance $L_0$ is known, the time-varying components of the *RLC* tank are extracted from the pole position $\lambda$ as from the pole position as

$$C_0(t) = \frac{1}{L_0 \cdot |\lambda_0(t)|^2}; \quad G_0(t) = \frac{-2\Re(\lambda_0(t))}{L_0 \cdot |\lambda_0(t)|^2}, \quad (8.2)$$

where $\lambda_0(t)$ denotes one of the complex-conjugated poles from (8.1).

### 8.1.2. Effect of unknown admittance on the pole position of a *RLC* tank

An unknown admittance $Y' = G' + s \cdot C'$ connected in parallel to the *RLC* tank moves the original pole $\lambda$ to a new position $\lambda'$ (Fig. 8.2), where

$$|\lambda'| = \frac{1}{L_0 \cdot (C_0 + C')}; \quad \Re(\lambda') = \frac{-G_0 + G'}{2(C_0 + C')}, \quad (8.3)$$

The unknown admittance $Y'$ could be for instance the effective admittance of a cross-coupled pair in *LC* oscillator. It is assumed that the cross-coupled pair does not possess inductive behavior on the frequency of oscillation, such that the admittance $Y'$ could be represented with equivalent conductance and capacitance, and the resonance tank inductance remains unchanged. Therefore, using the new and the original position of the pole, the resistive and the capacitive part of the unknown admittance can be calculated as:

$$C' = C_0 \left(\frac{|\lambda'|^2}{|\lambda|^2} - 1\right), \quad (8.4)$$
\[ G' = -2\Re(\lambda')\left(C_0 + C'\right) - G_0. \] (8.5)

8.1.3. Resonance tank components in complex oscillator topologies

The resonance tank components can be determined with (8.2) for oscillator using second-order \( RLC \) tank with known \( L_0 \). For complex resonator topologies involving more than one inductor, or unknown \( L_0 \), the effective resonance tank components \((L_0, C_0, \text{and} \ G_0)\) cannot be determined only from the position of the main complex-conjugated pole \( \lambda \). Therefore, an additional calculation is required to determine the tank components. A simple solution is to connect known conductance \( G_{\text{add}} \) in parallel to the \( RLC \) tank, and to compute a new pole \( \lambda'' \). Knowing \( G_{\text{add}}, \lambda, \text{and} \ \lambda' \), the resonance tank components are

\[ G_0 = -G_{\text{add}} \frac{\Re(\lambda)}{\Re(\lambda) - \Re(\lambda')} \quad C_0 = \frac{-G_0}{2\Re(\lambda)} \quad L_0 = \frac{1}{C_0 |\lambda|^2}. \] (8.6)

8.2. Negative and positive admittances created by a cross-coupled pair

8.2.1. Cross-coupled pair admittances

Fig. 8.3 shows the most commonly used cross-coupled pair topologies in \( LC \) oscillators: grounded cross-coupled pair (Fig. 8.3(a)), and cross-coupled pair degenerated with an admittance \( Y_3 \) (Fig. 8.3(b)). The admittance \( Y_3 \) could be the equivalent admittance of a current mirror, an \( LC \) filter, or any bias circuit. \( Y_1 \) and \( Y_2 \) are the admittances between the MOS transistors’ drain and the source terminals. Using the equivalent circuit for the grounded cross-coupled pair shown in Fig. 8.3(a), the currents flowing through the drain terminals are

Fig. 8.3. Cross-coupled pair configurations and their equivalent small-signal circuits: (a) grounded cross-coupled pair; (b) degenerated cross-coupled pair
The differential cross-coupled-pair admittance is \( Y_{cp} = (i_{\text{diff}}/v_{\text{diff}}) \), where \( i_{\text{diff}} = (i_1 - i_2)/2 \) and \( v_{\text{diff}} = (v_1 - v_2) \). If the LC oscillator produce sinusoidal and differential signals, then it can be assumed that \( v_1 = -v_2 \) and \( v_{\text{diff}} = 2v_1 \), which is a good approximation for low-noise LC oscillators with reasonably high tank Q-factor [7]. The assumption above may become less adequate with very large signals, but it is often necessary for closed-form derivations [6], [7]. Using the system equation (8.7) and the definition for \( Y_{cp} \), it can be shown that the differential admittance generated by the grounded cross-coupled pair is

\[
Y_{cp} = \frac{Y_1 + Y_2}{4} - \frac{g_{m1} + g_{m2}}{4}.
\]  

(8.8)

Equation (8.8) has the general form \( Y_{cp} = Y_{cp,\text{pos}} + Y_{cp,\text{neg}} \), which demonstrates that the cross-coupled pair generates both positive and negative admittance. The positive term \( Y_{cp,\text{pos}} \) in (8.8) represents the additional loading introduces by the cross-coupled pair to the resonance tank, whereas the negative term \( Y_{cp,\text{neg}} \) expresses the negative admittance that compensates the resonator losses and initiates oscillations. The resonator loading becomes substantial when one of the transistors enters the triode region corresponding to big \( Y_1(2) \) and small \( g_{m1(2)} \).

Using the same derivation technique and the differential oscillator property, it can be shown that the admittance created by the degenerated cross-coupled pair is: (the derivation is given in Appendix B)

\[
Y_{cp,Y_i} = + \frac{1}{4} \left( \frac{4Y_1Y_2 + Y_1(Y_1 + Y_2) + 2Y_1g_{mb2} + 2Y_2g_{mb1}}{Y_1 + \Sigma g_m + \Sigma g_{mb}} \right),
\]

\[
- \frac{1}{4} \left( \frac{4g_{m1}g_{m2} + Y_1(g_{m1} + g_{m2}) + 2g_{m1}g_{mb2} + 2g_{m2}g_{mb1}}{Y_2 + \Sigma g_m + \Sigma g_{mb}} \right).
\]  

(8.9)

where \( Y_\Sigma = Y_1 + Y_2 + Y_3 \), \( \Sigma g_m = g_{m1} + g_{m2} \), and \( \Sigma g_{mb} = g_{mb1} + g_{mb2} \). The positive and the negative terms of (8.9) have the same physical meaning as the terms in (8.8). If \( Y_3 \) represents a short connection (\( Y_3 = \infty \)), then (8.9) simplifies to (8.8). If \( Y_3 \) represents a ideal bias network (\( Y_3 = 0 \)) and we neglect the body-bias effect for simplicity, then

\[
Y_{cp,Y_i=0} = + \frac{Y_1Y_2}{Y_1 + Y_2 + \Sigma g_m} - \frac{g_{m1}g_{m2}}{Y_1 + Y_2 + \Sigma g_m},
\]  

(8.10)

which results in no loading effect when one of the transistor is in a triode region and the other one in a cutoff region (if \( M_1 \) operates in triode region then \( Y_1 \gg Y_2 \) and \( Y_{cp,\text{pos}} \approx 0 \)). The loading effect should be estimated with (8.9) for any other admittance \( Y_3 \) that is different than the two
extreme cases. The combined effect of $Y_{cp,pos}$ and $Y_{cp,neg}$ can be evaluated by other numerical methods, but the closed-form equation (8.9) allows separating the two terms, and it helps to estimate the additional resonator loading $Y_{cp,pos}$ caused by the cross-coupled pair.

8.2.2. Extraction of the cross-coupled pair admittances using TVRL

The extraction of $Y_{cp}$ given by (8.9) represents the general case for cross-coupled oscillators. The extraction for the other cross-coupled-pair configurations ($g_{mb} = 0$; or $Y_3 = \infty$) are modified version of the extraction procedure requiring fewer or no additional pole computations. The admittance of the cross-coupled pair can be calculated directly with (8.9) if the values of all components are known. The values of $g_{m1}, g_{m2}, g_{mb1}, g_{mb2}, Y_1$ and $Y_2$ are known in the TVRL computation since they are obtained after the MOS device linearization. However, the degeneration admittance $Y_3$ and the equivalent resonator components $G_0$ and $C_0$ are not known in advance, and they should be determined.

The oscillator may become perfectly balanced near the zero-crossings e.g. $g_{m1} = g_{m2} = g_m$; $g_{mb1} = g_{mb2} = g_{mb}$; and $Y_1 = Y_2 = Y$. In this condition, the cross-coupled pair admittance reduces to

$$Y_{cp} = \frac{1}{4} \frac{4Y^2 + 2YY_1 + 4Yg_{mb} - 4g_m^2 - 2Y_3g_m - 4g_mg_{mb}}{Y_3 + 2Y + \Sigma g_m + \Sigma g_{mb}},$$  \hspace{1cm} (8.11)

$$Y_{cp} = \frac{1}{4} \frac{2(Y - g_m)(Y_1 + 2Y + 2g_m + 2g_{mb})}{Y_3 + 2Y + 2g_m + 2g_{mb}} = \frac{Y - g_m}{2}. \hspace{1cm} (8.12)$$

Equation (8.12) shows that the degeneration admittance $Y_3$ does not affect $Y_{cp}$ in the case of perfect balance. Therefore, the extraction of $Y_3$ should avoid a possible balance of the transistor parameters. Even without perfect balance of transistor parameters, the extraction of $Y_3$ using (8.9) near the zero-crossings may cause numerical uncertainties. The extraction procedure below extracts $G_0$, $C_0$ and $Y_3$ in three steps through pole computations: the first computation determines $G_0$ and $C_0$, and the other two computations determine $Y_3$.

8.2.2.1. Pole computation with $g_{m1} = g_{m2} = 0$ and $Y_1 = Y_2 = 0$.

The cross-coupled pair does not contribute any admittance to the resonance tank ($Y_{cp,1} = 0$). The circuit admittance matrix is composed with $g_{m1} = g_{m2} = 0$ and $Y_1 = Y_2 = 0$, and then the main root, $\lambda_1$, is computed. The computed $\lambda_1$ corresponds to $\lambda$ in Fig. 8.2, and thus $G_0$ and $C_0$ are determined by (8.2). Since $Y_{cp,1} = 0$, the extracted $G_0$ and $C_0$ are contributed by the unknown part of the oscillator (resonator, parasitic components, buffer input impedance, etc).
8.2.2.2. Pole computation with \( g_{m1} = g_{m2} = 0; \ Y_1 = Y_1'; \) and \( Y_2 = Y_2' \)

Second and third pole computations (\( \lambda_2 \) and \( \lambda_3 \)) are in fact computations of \( \lambda' \) in Fig. 8.2, where \( \lambda' = \lambda_2 \) if \( Y_1(t) > Y_2(t) \) and \( \lambda' = \lambda_3 \) otherwise, therefore both \( \lambda_2 \) and \( \lambda_3 \) have to be calculated. Instead of the time-varying \( Y_1(t) \) and \( Y_2(t) \), the computation uses fixed \( Y_1 \) and \( Y_2 \) values for all time instants, such that the possible balance around the zero-crossing is avoided (\( Y_1' \neq Y_2' \)). The values for \( Y_1' \) and \( Y_2' \) should be in the vicinity of \( Y_1(t) \) and \( Y_2(t) \) in order to obtain reliable numerical results. The selected values for \( Y_1' \) and \( Y_2' \) are \( Y_1' = \max(Y_1(t)) \) and \( Y_2' = \max(Y_2(t))/10 \), where the desired parameter misbalance (\( Y_1' > Y_2' \)) is realized by the denominator 10. It was experimentally verified that denominator from 2 to 10 lead to a good numerical accuracy. The admittance \( Y_{cp} \) generated by the cross-coupled pair reduces to

\[
Y_{cp,2} = \frac{1}{4} \left( 4Y_1'Y_2' + Y_3' \left( Y_1' + Y_2' \right) + 2Y_1'g_{mb2} + 2Y_2'g_{mb1} \right) / \left( Y_3' + Y_1' + Y_2' + \Sigma g_{mb} \right),
\]

(8.13)

and the degeneration admittance is expressed from (8.13) as

\[
Y_3' = \frac{4Y_1'Y_2' + 2Y_1'g_{mb2} + 2Y_2'g_{mb1} - 4Y_{cp,2} \left( Y_1' + Y_2' + \Sigma g_{mb} \right)}{4Y_{cp,2} - \left( Y_1' + Y_2' \right)}. \quad (8.14)
\]

The admittance matrix is composed with \( g_{m1} = g_{m2} = 0, \ Y_1 = Y_1'; \ Y_2 = Y_2' \), and then the main root, \( \lambda_2 \), is computed. The capacitive and the resistive part of \( Y_{cp,2} (C' \text{ and } G' \text{ in Fig. 8.2}) \) are determined using (8.4) and (8.5) where \( \lambda \) is replaced by \( \lambda_1 \), and \( \lambda' \) is replaced by \( \lambda_2 \). The admittance \( Y_3 \) is computed with (8.14).

8.2.2.3. Pole computation with \( g_{m1} = g_{m2} = 0; \ Y_1 = Y_1'' \); and \( Y_2 = Y_2'' \)

Similarly to the second pole computation, \( Y_1(t) \) and \( Y_2(t) \) are replaced with \( Y_1'' = \max(Y_1(t))/10 \) and \( Y_2'' = \max(Y_2(t)) \) (now \( Y_1'' < Y_2'' \)). \( \lambda_3 \) is computed from the admittance matrix with \( g_{m1}=g_{m2}=0, \ Y_1=Y_1'', \) and \( Y_2=Y_2'' \). The cross-coupled-pair admittance and the degeneration admittance are respectively

\[
Y_{cp,3} = \frac{1}{4} \left( 4Y_1''Y_2'' + Y_3'' \left( Y_1'' + Y_2'' \right) + 2Y_1''g_{mb2} + 2Y_2''g_{mb1} \right) / \left( Y_3'' + Y_1'' + Y_2'' + \Sigma g_{mb} \right), \quad (8.15)
\]

\[
Y_3'' = \frac{4Y_1''Y_2'' + 2Y_1''g_{mb2} + 2Y_2''g_{mb1} - 4Y_{cp,3} \left( Y_1'' + Y_2'' + \Sigma g_{mb} \right)}{4Y_{cp,3} - \left( Y_1'' + Y_2'' \right)}. \quad (8.16)
\]

The capacitive and the resistive parts of \( Y_{cp,3} \) are determined using (8.4) and (8.5), where \( \lambda \) and \( \lambda' \) are replaced by \( \lambda_1 \) and \( \lambda_3 \) respectively. Although the conditions for \( \lambda_2 \) and \( \lambda_3 \) look similar, \( \lambda_3 \) provides a better estimate of \( Y_3 \) when \( Y_1(t) < Y_2(t) \), respectively \( \lambda_2 \) gives a better
8.2. Negative and positive admittances created by a cross-coupled pair

Estimate of $Y_3$ when $Y_1(t) > Y_2(t)$. The extraction procedure determines which pole computation to use for determining $Y_3$ based on the known time-varying values of $Y_1$ and $Y_2$. The cross-coupled pair admittances $Y_{cp,pos}$ and $Y_{cp,neg}$ are estimated from (8.9) after $Y_3$ is computed.

8.2.2.4. Nominal pole computation

This is an optional pole computation for the $Q$-factor extraction in which all circuit components enter the admittance matrix and the computed tank conductance is

$$G_{TOT} = \frac{2\Re(\lambda_{nom})}{L_o |\lambda_{nom}|^2},$$

(8.17)

where $G_{TOT}$ is the total conductance connected in parallel to the resonance LC tank ($G_{TOT} = G_0 + G'$). The sum of the extracted $G_0$, $\Re(Y_{cp,pos})$ and $\Re(Y_{cp,neg})$ should be equal to the total conductance $G_{TOT}$, where $\Re(\cdot)$ denotes the admittance real part. An eventual equality departure display an error of the extraction procedure described above. The error introduced by the extraction procedure is evaluated with

$$\Delta_{EXTR} = \frac{G_{TOT} - \left( G_0 + \Re(Y_{cp,pos}) + \Re(Y_{cp,neg}) \right)}{\max(G_{TOT}) - \min(G_{TOT})},$$

(8.18)

and it represents a relative deviation of the actual resonator conductance to what has been extracted using the proposed method. Equation (8.18) evaluates the accuracy of the extraction procedure presented above.

A verification of the cross-coupled pair admittance given by (8.9) is presented in the Appendix B for a generic cross-coupled LC oscillator. The topology has been selected such that all parameters in (8.9) are known, or they can be determined in straightforward manner. The sum of the calculated admittances contributed by the cross-coupled pair ($Y_{cp,neg}$ and $Y_{cp,pos}$) and the resonance tank conductance $G_0$ follow closely the position of the main complex-conjugate pole as defined by (8.2). The extraction procedure has been verified for various cross-coupled oscillators in different conditions with worst-case extraction error $\Delta_{EXTR}$ (8.18) not exceeding 5%.

8.2.3. Note on the calculation of $Y_{cp,pos}$ and $Y_{cp,neg}$

Equation (8.9) represents a closed-form expression for $Y_{cp,pos}$ and $Y_{cp,neg}$, which allows evaluating the resonator loading caused by the cross-coupled pair. The evaluation of (8.9) should be done with care in case of complex admittances ($Y_1$, $Y_2$, and $Y_3$), because some of terms of $Y_{cp,pos}$ may produce negative conductance, and terms of $Y_{cp,neg}$ may produce positive conductance. These frequency-dependent transformations have been used for increasing the
bandwidth of a capacitor-degenerated cross-coupled pair in high-frequency VCOs [80]. The extraction procedure evaluates all the terms in (8.9) and evaluates their contribution to $Y_{cp,neg}$ and $Y_{cp,pos}$. Once again, such an evaluation is possible thanks to the closed-form solution (8.9).

8.3. Effective $Q$-factor calculation

Fig. 8.4(a) shows the RLC tank model of an LC oscillator with separate passive and active time-varying conductances, where $g_{pass}(\phi)$ is the sum of the equivalent resonator conductance $G_0(\phi)$ and the loading $\Re(Y_{cp,pos}(\phi))$. $g_{act}(\phi)$ denotes the extracted $\Re(Y_{cp,neg}(\phi))$ generated by the cross-coupled pair, $\phi \equiv \omega_ot$, $\omega_o$ is angular oscillation frequency. The time-varying conductance $g_{pass}(\phi)$ is obtained by the extraction procedure above, which computes $G_0(\phi)$ and $Y_{cp,pos}(\phi)$. Similar separation of positive and negative conductances was used also in another $Q$-factor analysis [116]. The time-varying conductance $g_{pass}(\phi)$ is transformed into an effective conductance $g_{eff,T_0}$ that is valid for one oscillation period in order to determine the effective $Q$-factor ($Q_{eff,T_0}$). The transformation assumes that the time-invariant $g_{eff,T_0}$ generates the same amount of noise as the time-varying conductance $g_{pass}(\phi)$ [6], [7]. Here we utilize the result derived with the ISF theory, which gives the link between time-varying noise and time-invariant (effective) noise as [7]:

$$\Gamma_{R_{eff, rms}}^2 \cdot \overline{i_{g_{pass}}^2} = \frac{1}{2\pi} \int_0^{2\pi} \Gamma_{R}^2(\phi) \overline{i_{g_{pass}}^2(\phi)} d\phi,$$

(8.19)

where the time-varying noise generated by $g_{pass}(\phi)$ is

$$\overline{i_{g_{pass}}^2(\phi)} = 4kT \cdot g_{pass}(\phi) \cdot \Delta f,$$

(8.20)
8.3. Effective Q-factor calculation

\[ \Gamma_R(\phi) \] is the ISF function of a conductance connected in parallel to the resonance tank, and \( \Gamma_{R,eff,rms} \) is the effective coefficient describing the portion of the noise contributing to the total phase noise in the ISF phase noise model. It has been shown that for a sinusoidal LC oscillator \( \Gamma_R(\phi) \approx \cos(\phi) \) and \( \Gamma^2_{R,eff,rms} = 1/2 \) [6], [7]. Therefore, the effective conductance \( g_{eff,T_0} \), which generates the same amount of noise as the time-varying \( g_{pass}(\phi) \), becomes

\[
g_{eff,T_0} = \frac{1}{\pi} \int_0^{2\pi} \cos^2(\phi) \cdot g_{pass}(\phi) d\phi. \tag{8.21}
\]

Typical waveforms of oscillator voltage, extracted \( g_{pass}(\phi) \), and integrand of (8.21) are shown in Fig. 8.4(b). The calculation of \( g_{eff,T_0} \) is done numerically, because a closed form expression for \( g_{pass}(\phi) \) is not available. Once \( g_{eff,T_0} \) is found, the effective impedance-based Q-factor of the RLC tank is computed with:

\[
Q_{TVRL} = Q_{eff,T_0} = \left( \omega_o L_o \cdot g_{eff,T_0} \right)^{-1}. \tag{8.22}
\]

The same methodology can be applied to calculate the effective negative conductance \( g_{act,T_0} \) based on the extracted \( g_{act}(\phi) \).

As neither measurement nor simulator can provide explicit information of Q-factor, to validate the Q-factor extraction, it is used the oscillator phase noise considering only the white noise of the VCO elements and not accounting for flicker noise or bias noise (if desired, predictions of bias and flicker noise could be obtained as shown in [6], [7], [54], [63], and [135]). To do so, it is used the ISF phase noise of [7], [63] applied to the RLC circuit in Fig. 8.4(a), as follows

\[
L_{TVRL} = 10 \log_{10} \left( \frac{\Gamma^2_{R,eff,rms} \cdot \left( \frac{i_{g_{pass,eff}}^2}{\Delta f} + \frac{i_{g_{act,eff}}^2}{\Delta f} \right)}{q_{\max}^2 \cdot 2\Delta \omega^2} \right), \tag{8.23}
\]

where \( \frac{i_{g_{pass,eff}}^2}{\Delta f} = 4kT \cdot g_{eff,T_0} \), \( \frac{i_{g_{act,eff}}^2}{\Delta f} = 4kT \cdot \gamma \cdot g_{act,T_0} \), \( q_{\max} \) is the maximum charge swing across the tank capacitor, and \( \gamma \) is the noise factor of the MOS transistor. The “TVRL” subscript in (8.23) denotes that the phase noise is computed based on parameters extracted by the TVRL method. The simplified phase noise model (8.23) is used only as an auxiliary tool to validate the Q-factor extraction via phase noise comparison in the \( 1/f^2 \) phase noise region, since neither measurement nor simulator can provide explicit information for Q-factor.
8.4. Phase noise model refinement using $Q_{TVRL}$

The Leeson phase noise model [94] underlines the most important circuit parameters involved in the oscillator design: the resonator quality factor $Q$, the amplifier noise factor $F$, and the signal power $P_s$. The model does not capture the nonlinear effects arising from the large-signal operation of the oscillators, and some of the parameters are intuitive but hard to determine in practice. Nevertheless, the model has gained large popularity due to its simplicity and ease of use. One of the shortcomings of the Leeson model is the uncertainty of how the loaded $Q$-factor is determined.

The Rael’s phase noise model [135] is based on the Leeson proportionality, and it derives analytically the noise factor $F$ as a function of the circuit parameters for cross-coupled $LC$ oscillators. The derived noise factor $F$ is divided in three terms: the first term modeling the resonator loss; the second term modeling the noise of the switching differential pair, and the third term modeling the noise contributed by the biasing current mirror:

$$F = 1 + \frac{4\gamma \cdot I \cdot R_p}{\pi V_0} + \gamma \frac{4}{9} g_{mbias} \cdot R_p,$$

(8.24)

where $R_p$ is the equivalent resistor in parallel to the $LC$ tank. The derivation of (8.24) accounts the nonlinear nature of the oscillator, and thus it captures frequency conversion effects. The Rael’s phase-noise model allows separate optimization of the switching pair transistors and the biasing network. Despite the analytical expression of $F$, the Rael’s model assumes that the resonator $Q$-factor is known in advance, and remains constant. However, the MOS transistors (cross-coupled pair and bias transistor) enter triode region during the large signal operation of the oscillator and may cause $Q$-factor degradation [69]. The presented above TVRL methodology for extracting the effective $Q$-factor can be used to refine the existing phase noise models.

To illustrate the importance of recognizing the varying $Q$-factor, this subchapter shows an experiment in which the biasing current $I_B$ of the double-cross-coupled oscillator (1L) is swept to obtain different voltage swings. The schematic of the 1L oscillator is shown in Fig. 5.2(a) and Fig. 6.1(a). As described in Chapters 5-7, the TVRL does not account directly for high-order effect such as flicker noise up-conversion and bias noise contribution. Thus, the first two terms of the noise factor from the Rael’s phase noise model are used in the comparison, i.e.

$$F = 1 + \frac{4\gamma \cdot I \cdot R_p}{\pi V_0}.$$

(8.25)

The noise contribution of the bias network and flicker noise is removed from the SpectreRF
Phase noise model refinement using QTVRL

Fig. 8.5. Deviation of the Rael’s phase noise model from the Cadence simulations due to the constant $Q$-factor assumption, and its corrected model including the $Q$-factor deterioration mechanisms.

Phase noise simulations to obtain fair comparison. The estimate of the oscillator phase noise given by the Rael’s model is calculated as

$$L_{\text{RAEL}} = 10 \log_{10} \left( F \cdot \frac{1}{V_0^2} \frac{kT}{C} \frac{\alpha_0}{Q_{\text{eff}} \cdot (\Delta \omega)^2} \right),$$

where

$$F = 1 + \frac{2(\gamma_n/2 + \gamma_p/2) \cdot I \cdot R_p}{\pi V_0},$$

$R_p = Q_{\text{eff}} (2\pi f_{\text{osc}}) L_0$, $\gamma_n = \gamma_p = 2/3$ ($\gamma_n$ and $\gamma_p$ could be higher than 2/3 for short-channel devices, but values of 2/3 do not have to be wildly optimistic [7]). The Rael’s phase noise estimate uses the $Q$-factor derived from with TVRL for the lowest voltage swing, and assumes that it is constant when the bias current is swept. The refined Rael’s phase noise model $(8.26)$ uses $Q_{\text{TVRL}}$ obtained with the procedure described above instead of a constant value.

The phase noise results obtained with the original and with the refined Rael’s model are compared against SpectreRF simulation in Fig. 8.5. As the voltage swing grows with increased $I_B$, the cross-coupled MOS devices spend longer time in the triode region and cause $Q$-factor deterioration. Consequently, the expected phase noise improvement with increased voltage swing is not as big as the model using constant $Q$ predicts. In Fig. 8.5 is also shown the phase noise calculation based on the Rael’s model, but instead of constant $Q$-factor the model utilizes the effective $Q$-factor obtained from the TVRL method. The refined model follows closely the simulated phase noise improvement, since it accounts for the deteriorated $Q$-factor.
8.5. \(Q\)-factor investigation for cross-coupled \(LC\) oscillators

The example shown in Subchapter 8.4 clearly demonstrates the powerful results obtained with TVRL. The obtained effective \(Q\)-factor for the large-signal oscillator brings concrete information to circuit designers about the oscillator operation. The determination of effective \(Q\)-factor allows investigating various circuit techniques used for \(Q\)-factor preservation. In addition, different oscillator topologies can be compared in terms of how the resonator \(Q\)-factor is preserved in large-signal oscillator operation. Subchapter 8.5.1 demonstrates a comparison between 1L and 1L+2bL cross-coupled oscillator, which explains the benefit of using the additional inductors in the oscillator structure. Subchapter 8.5.2 evaluates the effective \(Q\)-factor for top-biased 2L oscillator under topology modifications (grounded cross-coupled pair versus degenerated cross-coupled pair), as well as under design variations. In both 8.5.1 and 8.5.2, the obtained effective \(Q\)-factor is used to predict the phase noise improvement when the voltage swing is increased, which agrees well with the phase noise improvement given by SpectreRF.

8.5.1. Topology comparison (1L versus 1L-2bL oscillators)

The topologies of the two oscillator modifications shown in Fig. 5.2 are compared in terms of the extracted \(Q\)-factor and predicted phase noise improvement for an increased voltage swing. The active and passive components are the same as the ones reported in Chapter 4 [P.2]. Fig. 8.6(a) shows a comparison of the obtained effective \(Q\)-factors in the two oscillators. The extracted \(Q\)-factor of the 1L oscillator reduces from 11.2 down to 6.2 as the voltage swing is increased from 0.8-Vpp to 1.4-Vpp. In the same conditions, the \(Q\)-factor of the 1L+2bL oscillator reduces from 12 to 9.1. As it is seen from Fig. 8.6(a), the two extra inductors provide better quality factor for signals above 0.8-Vpp, which justifies the additional silicon area needed for \(L_{\text{TOP}}\) and \(L_{\text{BOT}}\). The use of \(L_{\text{TOP}}\) and \(L_{\text{BOT}}\) is not beneficial below 0.8-Vpp, because the low

Fig. 8.6. (a) TVRL \(Q\)-factor comparison for the 1L oscillator and the 1L+2bL oscillator; (b) phase noise improvement for increased voltage swing predicted by TVRL for the 1L and the 1L+2bL oscillators, and its comparison against SpectreRF simulations.
amplitudes in the oscillator does not force the cross-coupled transistors into deep triode region, and the $Q$-factor deterioration is minor. This observation explains why the two extra inductors are often omitted in low-power / low-voltage applications. Using the effective $Q$-factor extracted with the TVRL approach, an estimation of how much the phase noise can be improved by increasing the signal amplitude is shown in Fig. 8.6(b). The estimated with (8.23) TVRL phase noise improvement is shown with dashed lines, while the simulated with SpectreRF improvement is shown with solid lines for the two oscillator modifications. The flicker noise contribution and the noise contribution from the biasing network are omitted from the SpectreRF results. The predicted phase noise improvement using TVRL follows closely the actual improvement, which confirms the reliability of the method. The small departure ($<1$dB) of the predicted improvement could be due to the assumptions taken in the analysis. The phase noise improvement predicted by the TVRL does not aim at high precision, but it rather targets to provide useful information to circuit designers instead of precise numerical data. From this point of view, the obtained results shown in Fig. 8.6(b) can be considered as a good verification of the TVRL results.

8.5.2. $Q$-factor deterioration analysis in Top-Biased 2L oscillator using NMOS cross-coupled pair

A second evaluation of the effective $Q$-factor is performed for the top-biased 2L oscillator modifications shown in Fig. 8.7. The oscillator architecture is similar to the double-cross-coupled topologies evaluated above, but the presence of only one cross-coupled pair makes the extraction of $Q$-factor more straight-forward and reliable (the 1L topologies require separate extraction of positive and negative conductance for each cross-coupled pair). The passive

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![Fig. 8.7. Modifications of the 2L Top-Biased oscillator using NMOS cross-coupled pair](image-url)
components and the active transistors are the same as the 1L topologies presented above.

8.5.2.1. Effect of cross-coupled MOS transistor sizes

In the first experiment, the size of the cross-coupled pair transistors $M_{n1}$ and $M_{n2}$ are made 2/3 of the nominal size $(W_{N,nom})$, the nominal size ($W/L = 39 \mu m/0.18 \mu m$), and 4/3 of the nominal size. The biasing current $I_B$ is swept to obtain voltage swing over the resonator ranging from 0.6-$V_{PP}$ up to approximately 1.5-$V_{PP}$. Fig. 8.8(a) shows the obtained effective $Q$-factor using the TVRL extraction method. Better $Q$-factor for given amplitude is obtained by making the size of the MOS transistor smaller. The obtained result has an obvious physical explanation – the value of the MOS on-resistance for given amplitude is proportional to $(W/L)^{-1}$. Thus, a smaller MOS transistor has bigger on-resistance, which leads to a smaller resonator loading and better effective $Q$-factor. The use of smaller transistors on the other hand decreases the negative-resistance at start-up, which is also seen in Fig. 8.8(a) – the amplitude generated by $(2/3) \cdot W_{N,nom}$ with the minimum $I_B$ current is the smallest among the other transistor sizes. Fig. 8.8(b) shows the predicted phase noise improvement by TVRL when increasing the signal amplitudes for the three transistor sizes compared against SpectreRF. The match between the predicted improvement and the SpectreRF simulation is remarkable.

The results presented in Fig. 8.8 bring clear guidelines for oscillator design depending on the specific targets. A low-power oscillator should use bigger cross-coupled pair transistors to generate small voltages. A low-noise high-performance oscillator generates big amplitudes, where the use of small transistors is beneficial in terms of $Q$-factor and phase noise.

8.5.2.2. Effect of the degeneration inductance $L_{BOT}$

The second experiment on the 2L oscillator involves structural changes involving the degeneration network, as shown in Fig. 8.7(a) and (b). The effect of the degeneration inductor $L_{BOT}$ on the effective $Q$-factor and on the phase noise performance is investigated and compared
8.6. Measurement verification

A measurement verification of the proposed $Q$-factor extraction procedure requires a carefully designed test-bench, which would clearly demonstrate the $Q$-factor deterioration via phase noise measurement. The VCO reported in Chapter 4 ([P.2]) is used here as a test vehicle for proving the concept. Since the proposed method accounts only the $Q$-factor deterioration effect on the phase noise, the bias network and the bias-control loop described in Chapter 4 are disabled during the measurement. The supply voltage is fed directly to the oscillator via an external pin connected on the common node of the transistor $M_{\text{REG}}$, $L_{\text{TOp}}$ and $C_{\text{FIL}}$ (see Fig. 4.1). The oscillator topology becomes effectively the one shown in Fig. 8.10(a). The $Q$-factor deterioration for different amplitudes is investigated by varying the power supply from 1.4V up to 2.0V. The phase noise is measured at given oscillation frequency under the varying supply.
conditions. The VCO phase noise is measured at 1-MHz offset, where the flicker noise contribution is minimal. The control voltage $V_A$ for the varactor is set to 1.5V where $K_{VCO}$ is approximately zero and the noise up-conversion effects are minimized.

The SpectreRF simulations are performed for the complete oscillator topology (including the capacitor bank and the varactor block) for varying power supply ($V_{DD} = 1.4V - 2.0V$). The TVRL computation uses the reduced-complexity equivalent circuit in Fig. 8.10(a), where $C_0$ is the effective tank capacitance and $R_P$ models the $Q$-factor of the resonator at given oscillation frequency. The values of $C_0$ and $R_P$ are extracted with SpectreRF from the complete resonator ($L_{MAIN}$, capacitor bank, varactor block, and buffer input impedance). The TVRL computation follows the procedure outlined in Chapter 5. The extraction of effective $Q$-factor follows the steps described in this chapter. The negative and positive conductance contributed by each cross-coupled pair is evaluated separately.

Fig. 8.10(b) shows the extracted with TVRL effective $Q$-factors of the oscillator for different oscillation frequencies. The $Q$-factors of the passive resonance tank are approximately 14.9, 15.0, 15.7, and 16.5 for FCW=511, 319, 255 and 127 respectively. The cross-coupled pair transistors operate in triode region for a part of the period even with $V_{DD}=1.4V$, which explains the $Q$-factor reduction from its native resonator value. Despite this reduction, the effective $Q$-factor remains relatively constant over the wide range of voltage supplies, which is achieved thanks to the bias inductors $L_{TOP}$ and $L_{BOT}$. As it was shown in Fig. 8.6(a) and Fig. 8.9(a), oscillator topologies omitting the bias inductors would suffer even more significant $Q$-factor deterioration in such supply conditions.
8.6. Measurement verification

Fig. 8.11. Comparison between the measured phase noise, the simulated phase noise, and predicted with TVRL phase noise at 4.17GHz for a fixed power supply.

To verify the proposed $Q$-factor extraction method, the measured phase noise $L_{\text{MEAS}}$ of the VCO prototype is compared against the simulated with SpectreRF phase noise $L_{\text{SRF, tot}}$ and the predicted phase noise $L_{\text{TVRL}}$ in Fig. 8.11 for $V_{DD}=1.7$ V and oscillation frequency of 4.17 GHz. The simulated phase noise $L_{\text{SRF, tot}}$ includes all building blocks of the VCO prototype (capacitor bank, varactor block, output buffer), while the TVRL computation utilizes the simplified oscillator model from Fig. 8.10(a). Furthermore, $L_{\text{TVRL}}$ is compared against the simulated phase noise $L_{\text{SRF, wn}}$, where the flicker noise contribution of the cross-coupled pair transistors is removed. As seen from Fig. 8.11, the TVRL provides a good phase noise prediction in the $1/f^2$ region, which, similarly to $L_{\text{SRF, wn}}$, starts to deviate from measurements at close-in offsets since the flicker noise is not accounted for. The verification of the extracted $Q$-factor using TVRL is done for various VCO frequencies, and below we present two typical cases.

Fig. 8.12(a) shows the phase noise results at 1MHz offset obtained by measurement, by SpectreRF simulations, and by using the proposed method under varying supply conditions. An excellent fit between the predicted phase noise using TVRL and the simulated $L_{\text{SRF, wn}}$ is achieved. The flicker noise contribution of the cross-coupled transistors is only in the order of 0.2-0.3dB, which makes the TVRL results sufficiently close to the total VCO phase noise. The goal of the analysis, however, is not to replace the numerical accuracy of SpectreRF, but rather to give information of effective $Q$-factor and to predict the amount of phase noise improvement under various conditions. Fig. 8.12(b) shows the relative phase noise improvement predicted by the TVRL and the improvement obtained with SpectreRF, where all results are normalized to the phase noise values obtained at $V_{DD}=1.6$V. Again, the agreement between prediction and
Fig. 8.12. Comparison between the measured phase noise, the simulated phase noise, and predicted with TVRL phase noise at 3.65GHz: (a) absolute phase noise; (b) relative phase noise improvement.

Fig. 8.13. Comparison between the measured phase noise, the simulated phase noise, and predicted with TVRL phase noise at 4.17GHz: (a) absolute phase noise; (b) relative phase noise improvement.

Numerical simulation are very good. However, the measured phase noise is approximately 1.5dB worse than the simulated phase noise at $V_{DD}=1.4V$ and the deviation gets bigger with larger $V_{DD}$. The worse measured phase noise could be due to: 1) the fully-differential assumptions ($v_1 = -v_2$) being less adequate; 2) increase of $\gamma_n$ and $\gamma_p$ due to larger overdrives; and 3) parasitic layout components not taken into account in the simulations. Despite these uncertainties, the phase noise deviation of 1.5dB is close to the precision of the phase-noise measurement instrument ($\pm 1$dB). The phase noise saturation for larger supply voltages is due to reaching noise floor of the output buffer or the measurement setup. Phase noise measurement at lower than 1-MHz offset would eliminate the noise floor, but on the other hand the increased flicker noise contribution would make the result validation more difficult. However, it should be underlined that the phase noise deviation is between the measurement and the simulations, and since the TVRL method uses the SpectreRF results, the obtained agreement between the two methods validates the proposed procedure.
As a second example, a comparison between the absolute phase noise and the phase noise improvement obtained at 4.17GHz oscillation frequency is shown in Fig. 8.13(a) and Fig. 8.13(b) respectively. The measurement phase-noise floor observed in the previous example is not detected here, which leads to very good agreement between measurements and simulations (the small deviations are well within the measurement accuracy and repeatability). Since the two most-significant bits of the capacitor bank are switched off to achieve the 4.17GHz frequency, the parasitic *pn*-junction diodes associated with the drain-bulk and the source-bulk regions of the switched transistor introduce visible capacitive-to-voltage dependence. The introduced CV dependence increases the flicker noise contribution of the cross-coupled pair transistors, as seen in Fig. 8.13(a). The TVRL method predicts a bit better phase noise than $L_{SRF,wn}$, but the deviation is at most 1dB for the biggest power supply. When the phase noise improvement is considered (Fig. 8.13(b)), the TVRL method gives results that are confirmed both by SpectreRF simulations and by measurements.

The good correlation between the TVRL method, the SpectreRF simulations, and the measurement results presented by the two examples validates the proposed $Q$-factor extraction algorithm. The comparison for other VCO frequencies gives similar results. As the target of the TVRL method is to give relative results that can be used for oscillator comparison, it can be concluded that the goal is met with sufficiently good precision. Precise numerical results of phase noise could be obtained with SpectreRF, which uses device models with their full complexity, but the design insights are lost. Furthermore, the derivation of the effective $Q$-factor presented in this chapter relies on few assumption and circuit simplifications, and thus complete match between SpectreRF and TVRL could not be expected. However, the design-oriented information brought by the TVRL method is indispensable for oscillator analysis and design.

### 8.7. Summary and contributions

An algorithm for extracting the effective $Q$-factor in large-signal LC oscillator is proposed. The algorithm uses the root position to extract negative and positive conductance contributed by cross-coupled-pair transistors. The extraction utilizes an analytical derivation of the conductances produced by different configurations of cross-coupled pairs, and it uses some of the ISF properties to calculate the effective loading seen by the resonator. Since the extraction involves few assumptions, the obtained results give design-oriented information instead of precise phase noise calculation. It was shown how the proposed method could be used to evaluate the amount of $Q$-factor deterioration in LC oscillator, and to compare the oscillator
performance with configuration changes and different transistor sizing. It was demonstrated that the popular Rael phase noise model could be improved when the extracted with TVRL $Q$-factor is used. Finally, the extraction of effective $Q$-factor is validated by simulations and measurement of real VCO prototype.

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The contributions of the work presented in this chapter are:

1. Derived is a general expression of time-varying cross-coupled pair admittance, which can be separated in positive and negative part. The derivation assumes arbitrary degeneration network. The positive admittance accounts for the losses in the cross-coupled pair, whereas the negative admittance represents the active admittance that compensates the losses in the oscillator structure.

2. The two parts of the time-varying cross-coupled pair admittance are extracted using root-locus computations relying on the TVRL method.

3. A time-varying and an effective oscillator $Q$-factor is computed based on the cross-coupled pair admittance separation. It is shown that a better prediction of the oscillator phase noise can be made under varying bias condition using the obtained $Q$-factor. The obtained $Q$-factor is verified with SpectreRF phase noise simulations and phase noise measurements of a VCO prototype.
Chapter 9

Conclusions

The first part of this thesis (Chapters 2–4) introduced two circuit-based approaches for enhancing the performance of fully monolithic VCOs. The first approach showed that the adoption of dual-band or multi-band VCO is a promising solution for covering multiple communication standards. As one main contribution, a dual-band VCO based on fourth-order resonator instead of second-order LC tank was demonstrated in the thesis. The thesis presented equations for designing the fourth-order resonator and analyzed the practical restrictions involved with the dual-band VCO design. As another contribution, a method for reducing the occupied by the fourth-order resonator silicon area was proposed. The reduction of silicon area was based on the utilization of multi-tapped inductor, whose restrictions and design implications were theoretically analyzed in Chapter 3. The second circuit-based approach addressed performance improvement in a well-known LC VCO architecture, that brings benefits when the VCO is tailored to the reprogrammable requirements of the nowadays transceivers. As another contribution, the demonstrated programmable $K_{\text{VCO}}$ concept allows optimization of phase noise by reducing the VCO analog tuning range. The programmable $K_{\text{VCO}}$ concept and its modifications were successfully adopted by the scientific and industrial community. Both circuit-based approaches proposed in the thesis mitigate the fundamental tradeoff between low phase noise and wide tuning range, which was a main objective of the circuit-based approach.

The second part of the thesis (Chapters 5–8) is focused on the theoretical analysis of LC oscillators. As another main contribution, a Time-Varying Root-Locus method was proposed for the theoretical analysis of oscillators, which evaluates the trajectories of the oscillator roots and links the trajectories to physical phenomena in oscillators. The proposed method possesses an adequate numerical precision while keeping a physical meaning of the results. The TVRL was proven useful for comparing LC oscillator structures, and for evaluating the various aspects influencing the oscillator’s behavior (parasitic components, varactors, bias current, etc.). As a further contribution, an extraction of effective $Q$-factor of LC oscillators based on cross-coupled pair was demonstrated. The extraction of effective $Q$-factor utilized the proposed in this thesis
TVRL analysis and a theoretical derivation of a cross-couple-pair admittance. The proposed $Q$-factor extraction was shown to be superior to other methods for $Q$-factor estimation, at it was verified through both simulations and measurements. Respectively, the proposed method was linked to the other design-oriented methods for phase noise analysis, and it could become an auxiliary tool for oscillator characterization. The proposed method fills some of the gaps between the CAD-oriented and the design-oriented methods for oscillator analysis, which was one of the main objective of the theoretical analysis of VCO phase noise in this thesis.

9.1. Future works

The use of dual-band VCO based on fourth-order resonator was proven as a promising solution for the nowadays multi-standard transceivers. Measurement confirmation of the theory and guidelines developed in Chapter 3 is the first step to continue the research in this area. Furthermore, a development of VCO architecture based on the fourth-order resonator that covers the typical gap between the high-frequency and the low-frequency band might be of interest. Combination of dual-band VCO together with some frequency-translation technique may extend the applicability of the VCO towards UWB generators. The existence of two frequency bands would reduce the amount of frequency-translation blocks, such as mixers or frequency dividers, thus reducing complexity and power consumption.

The proposed Time-Varying Root-Locus method is in its initial stage of development and it faces more development possibilities. To name a few, the TVRL could be applied for the large-signal analysis of the fourth-order VCOs presented in Chapter 2 and Chapter 3. Furthermore, the extension of the TVRL method towards quadrature LC oscillators will require more than one main root to be taken into account, which will complicate the root trajectory treatment and its numerical computation. On the other hand, the existence of two or more main roots may help understanding the synchronization between two coupled VCO cores, and may help to estimate the deterioration of the quadrature signal accuracy. Other future target for the TVRL is to link the root trajectories directly with the oscillator phase noise. It was shown in Chapter 8 that the TVRL can be successfully used for extracting effective $Q$-factor of cross-coupled LC oscillator, and thus the TVRL provides indirect link to the oscillator phase noise and to other design-oriented analysis methods. However, the TVRL in its present form cannot compute an absolute value of phase noise. An intermediate step for the phase noise computation might be the computation of root sensitivity against design parameters and noise. Despite the many unknowns facing the TVRL method, these unknowns are also seen as opportunities for further research on the area of oscillators and VCOs.
Appendixes

A. MNA circuit description for the 1L+2bL oscillator

Fig. 10.1 shows the small-signal equivalent circuit for the 1L+2bL oscillator. Each MOS transistor is replaced with its quasi-static model, and inductors are represented by their on-chip π-models.

Fig. 10.1 shows the small-signal equivalent circuit for the 1L+2bL oscillator. The MOS transistors are replaced with their time-varying small-signal model (Fig. 5.3), and the inductors are replaced with their on-chip equivalent π-type circuit. The finite $Q$-factor of the capacitors in the LC-tank $C_{o1}$ and $C_{o2}$ is modeled with the series resistors $r_{o1}$ and $r_{o2}$.

The admittance matrix $Y$ of the Modified-Nodal Analysis contains frequency-independent components, such as resistors and transconductances, and frequency-dependent components, such as capacitors and inductors. The frequency-independent components form the matrix $G$, whereas the frequency-dependent components form the matrix $B$. The admittance matrix is split in two parts for the subsequent pole computation. The matrices $G$ and $B$ are in numeric form, which allows the use of precise and fast eigenvalue computation algorithm. The matrices $G$ and $B$ for the 1L+2bL oscillator have a size of 19, which correspond to 16 nodes in the equivalent circuit, and three inductors (each inductor in MNA increases the matrix size by one). Using the
small-signal representation of the oscillator with the designated nodes in Fig. 10.1, the matrices \( G \) and \( B \) are formed, and their non-zero cells are:

\[
G_{1,1} = g_{ds,n1} + g_{ds,p1} \\
G_{1,11} = -g_{ds,p1} - g_{m,p1} \\
G_{2,3} = G_{5,2} = -r_s^{-1} \\
G_{1,3} = r_s^{-1} \\
G_{6,6} = r_{o1}^{-1} \\
G_{8,2} = -g_{m,n} - g_{ds,n2} \\
G_{9,9} = r_{sb}^{-1} \\
G_{12,12} = R_{1}^{-1} \\
G_{14,14} = g_{ds,p3} + r_{st}^{-1} \\
G_{16,16} = g_{ds,p4} + g_{m,p4} \\
G_{1,17} = G_{9,18} = G_{13,19} = G_{17,3} = G_{18,9} = G_{19,13} = -1;
\]

and

\[
B_{1,1} = c_{gd,n1} + c_{sd,n1} + c_{bd,n1} + c_{jd,n1} + c_{gs,n2} + c_{gd,n2} + c_{gb,n2} + c_{gd,p1} + c_{sd,p1} + c_{bd,p1} + c_{jd,p1} + c_{gs,p2} + \ldots + c_{gd,p2} + c_{gb,p2} + C_{ox1} + C_{o1}; \\
B_{1,2} = -c_{gd,n1} - c_{m,n1} - c_{gd,n2} - c_{gd,p1} - c_{m,p1} - c_{gd,p2}; \quad B_{1,4} = -R_{ox1}; \\
B_{1,6} = -C_{o1}; \quad B_{1,8} = -c_{sd,n1} - c_{m,n1} + c_{mb,n1} - c_{gs,n2}; \\
B_{1,11} = -c_{sd,p1} - c_{bd,p1} + c_{m,p1} - c_{jd,p1} - c_{gs,p2} - c_{gb,p2}; \\
B_{2,1} = -c_{gd,n1} - c_{gd,n2} - c_{gd,p1} - c_{gb,p2} - c_{m,p2}; \\
B_{2,2} = c_{gs,n1} + c_{gs,n2} + c_{gb,n1} + c_{gd,n2} + c_{ad,n2} + c_{bd,n2} + c_{jd,n2} + c_{gs,p1} + c_{gd,p1} + c_{gb,p1} + c_{gd,p2} + c_{ad,p2} + \ldots + c_{bd,p2} + c_{jd,p2} + C_{o1} + C_{o2}; \\
B_{2,5} = -C_{ox2}; \quad B_{2,7} = -C_{o2}; \\
B_{2,8} = -c_{gs,n1} - c_{ad,n2} + c_{m,n2} + c_{mb,n2}; \quad B_{2,11} = -c_{gs,n1} - c_{gb,n1} - c_{ad,p2} - c_{bd,p2} + c_{m,p2} - c_{jd,p2}; \\
B_{2,1} = -C_{ox1}; \quad B_{2,4} = C_{ox1}; \quad B_{3,2} = -C_{ox2}; \\
B_{3,5} = C_{ox2}; \quad B_{6,1} = -C_{o1}; \quad B_{6,6} = C_{o1}; \\
B_{7,2} = -C_{o2}; \quad B_{7,7} = C_{o2}; \\
B_{8,1} = -c_{sd,n1} - c_{ad,n2} + c_{m,n2} + c_{mx,n2}; \quad B_{8,2} = -c_{gs,n1} + c_{m,n1} + c_{mx,n1} - c_{ad,n2}; \\
B_{8,8} = c_{gs,n1} + c_{ad,n1} + c_{ox,n1} - c_{m,n1} - c_{mb,n1} + c_{gs,n2} + c_{ad,n2} + c_{bd,n2} - c_{m,n2} - c_{mx,n2} + C_{b} + C_{b1}; \\
B_{8,10} = B_{10,8} = -C_{b1}; \quad B_{10,10} = C_{b1} + C_{b2}; \\
B_{11,1} = -c_{sd,p1} - c_{bd,p1} - c_{gs,p2} - c_{gb,p2} + c_{m,p2}; \\
B_{11,2} = -c_{gs,p1} - c_{gb,p1} + c_{m,p1} - c_{sd,p2} - c_{bd,p2} - c_{jd,p2};
\]
A. MNA circuit description for the 1L+2bL oscillator

\[ B_{11,11} = c_{gs,p1} + c_{gb,p1} + c_{sd,p1} + c_{bd,p1} - c_{m,p1} + c_{jd,p1} + c_{gs,p2} + c_{gb,p2} + c_{sd,p2} + c_{bd,p2} - c_{m,p2} + c_{jd,p2} + C_1 + C_{j1}; \]
\[ B_{11,2} = B_{12,11} = -C_{i1}; \]
\[ B_{11,14} = B_{14,11} = -C_i; \]
\[ B_{12,12} = C_{i1} + C_{i2}; \]
\[ B_{14,14} = c_{gd,p3} + c_{sd,p3} + c_{bd,p3} + c_{jd,p3} + C_i + C_{i3} + C_{FILT}; \]
\[ B_{14,15} = B_{15,14} = -C_{i3}; \]
\[ B_{14,16} = -c_{gd,p3} - c_{m,p3}; \]
\[ B_{15,15} = C_{i3} + C_{i4}; \]
\[ B_{16,14} = -c_{gd,p3}; \]
\[ B_{16,16} = c_{gs,p3} + c_{gd,p3} + c_{gb,p3} + c_{gs,p4} + c_{gb,p4} + c_{sd,p4} + c_{bd,p4} - c_{m,p4} + c_{jd,p4}; \]
\[ B_{17,17} = -L_i; \]
\[ B_{18,18} = -L_b; \]
\[ B_{19,19} = -L_v; \]

The non-zero element structure of the \( G \) and \( B \) matrices depends on the numbering of the nodes, but in general they are almost symmetric matrices with element near and on the main matrix diagonal. The matrix symmetry is lost in cases where the circuit contains voltage-controlled current sources (losing the symmetry in \( G \)), or trans-capacitances (introduced by the quasi-static MOS models, losing the symmetry in \( B \)).
B. Positive and negative conductance generated by cross-coupled pair

B.1. Degenerated cross-coupled pair and MOS body-bias effect

Fig. 10.2. Small-Signal representation of the cross-coupled transistors including the body-bias effect

Fig. 10.2 shown the equivalent model of the cross-coupled pair degenerated with a finite admittance $Y_3$. The parameters in the equivalent model are: $g_{m1(2)}$ is the MOS transistor transconductance; $g_{mb1(2)}$ is the body-bias effect on the transistor transconductance; and $Y_{1(2)}$ is the admittance connected between transistor drain and source terminal. The system of equations expressing the branch currents is

\[
\begin{align*}
    i_1 &= Y_1(v_1 - v_3) + g_{m1}(v_2 - v_3) - g_{mb1}v_3 \\
    i_2 &= Y_2(v_2 - v_3) + g_{m2}(v_1 - v_3) - g_{mb2}v_3 \\
    i_1 + i_2 &= Y_3v_3
\end{align*}
\]

(10.1)

After summing the first two equations and equalizing it to the third equation, the unknown voltage $v_3$ can be expressed as

\[
v_3 = v_1 \frac{Y_1 + g_{m2}}{Y_1 + \Sigma g_m + \Sigma g_{mb}} + v_2 \frac{Y_2 + g_{m1}}{Y_2 + \Sigma g_m + \Sigma g_{mb}},
\]

(10.2)

where $Y_\Sigma = Y_1 + Y_2 + Y_3$, $\Sigma g_m = g_{m1} + g_{m2}$, and $\Sigma g_{mb} = g_{mb1} + g_{mb2}$. Substituting (10.2) into the first equation in (10.1) gives the expression for $i_1$

\[
i_1 = v_1 \left( Y_1 - \frac{Y_1 + g_{m1} + g_{mb1} + g_{m2}}{Y_1 + \Sigma g_m + \Sigma g_{mb}} (Y_1 + g_{m2}) \right) + v_2 \left( g_{m1} \frac{Y_1 + g_{m1} + g_{mb1} + g_{m2}}{Y_2 + \Sigma g_m + \Sigma g_{mb}} (Y_2 + g_{m2}) \right) = \frac{v_1}{D} \left( g_{m1} Y_2 + g_{m2} + g_{mb1} g_{m2} + g_{m1} \Sigma g_{mb} \right)
\]

\[
+ v_2 \left( -g_{m1} Y_2 + g_{m2} + g_{mb1} Y_1 - Y_1 \Sigma g_{mb} \right)
\]

where $D = Y_\Sigma + \Sigma g_m + \Sigma g_{mb}$, and the above expression for $i_1$ simplifies to
### B. Positive and negative conductance generated by cross-coupled pair

\[
i_1 = v_1 \frac{Y_1(Y_2 + Y_3) + Y_1g_{mb2} - g_{m1}g_{m2} - g_{mb1}g_{m2}}{Y_\Sigma + \Sigma g_m + \Sigma g_{mb}} + v_2 \frac{Y_1g_{m1} - Y_2 + g_{m1}g_{m2} + g_{m1}g_{mb2} - g_{mb1}Y_2}{Y_\Sigma + \Sigma g_m + \Sigma g_{mb}}
\]  
(10.3)

Similarly, substituting (10.2) into the second equation in (10.1) gives \(i_2\):

\[
i_2 = v_1 \left( \frac{g_{m2} - (Y_2 + g_{m2} + g_{mb2})(Y_1 + g_{m2})}{Y_\Sigma + \Sigma g_m + \Sigma g_{mb}} \right) + v_2 \left( \frac{Y_2 - (Y_2 + g_{m2} + g_{mb2})(Y_2 + g_{m1})}{Y_\Sigma + \Sigma g_m + \Sigma g_{mb}} \right) = v_1 \frac{Y_1Y_2 + Y_3g_{m2} + g_{m1}g_{m2} + g_{m1}g_{mb2} - Y_1Y_2}{Y_\Sigma + \Sigma g_m + \Sigma g_{mb}}
\]

which simplifies to

\[
i_2 = v_1 \frac{-Y_1Y_2 + Y_3g_{m2} - Y_1g_{mb2} + g_{m1}g_{m2} + g_{m2}g_{mb1}}{Y_\Sigma + \Sigma g_m + \Sigma g_{mb}} + v_2 \frac{Y_2(Y_1 + Y_3) + Y_2g_{mb1} - g_{m1}g_{m2} - g_{mb1}g_{m2}}{Y_\Sigma + \Sigma g_m + \Sigma g_{mb}}
\]  
(10.4)

Using the definition for \(Y_{cp}\) \(\left( Y_{cp} = \frac{i_{diff}}{v_{diff}} \right)\), equations (10.3)-(10.4), and exploiting the differential property of the oscillator \(\left( v_1 = -v_2 \right)\), the equivalent admittance created by the cross-coupled pair is

\[
Y_{cp} = \frac{(i_1 - i_2)/2}{2v_1} = + \frac{4}{4} \frac{Y_1Y_2 + Y_3(Y_1 + Y_2) + 2Y_1g_{mb2} + 2Y_2g_{mb1}}{Y_\Sigma + \Sigma g_m + \Sigma g_{mb}} - \frac{4}{4} \frac{1}{Y_\Sigma + \Sigma g_m + \Sigma g_{mb}}
\]  
(10.5)

Equation (10.5) gives the expression for the positive and negative conductance created by the cross-coupled pair with finite degeneration and body-bias effect.

#### B.2. Verification of (10.5)

The simplified oscillator test-benches shown in Fig. 10.3 are used for verifying equation (10.5) derived for the cross-coupled pair admittance, where the conductance of the resonance tank is \(R_p\), and the contribution of the cross-coupled pair is calculated with (10.5). The calculated conductance is compared against the total conductance associated with the main complex-conjugated pole. The component values used for the verification are: \(R_p = 2k\Omega\); \(L_0 = 0.83\text{nH}\); \(C_o = 1.5\text{pF}\); \(R_{deg} = 100\Omega\); \(C_{deg} = 100\text{fF}\); and \(L_{deg} = 1.69\text{nH}\).
Fig. 10.3. Simplified oscillator topologies used for verification of the derived cross-coupled pair admittances: (a) grounded cross-coupled pair; (b) RC / RLC de-generated cross-coupled pair

The degeneration admittance of the cross-coupled pair is known and it is

\[ Y_3 = \frac{1}{R_{\text{deg}}} + sC_{\text{deg}} + \frac{1}{sL_{\text{deg}}} \], \hspace{1cm} (10.6)

where instead of the complex variable \( s \) is used the frequency of the main complex-conjugated pole. The calculated with the help of (10.5) total conductance is

\[ G_{\text{calc}} = 1/R_p + \mathfrak{Re} \left( Y_{cp,\text{pos}} \right) + \mathfrak{Re} \left( Y_{cp,\text{neg}} \right) \], \hspace{1cm} (10.7)

and it is compared against the total conductance obtained from the nominal pole computation \((G_t = -2\mathfrak{Re}(\lambda) / (L_o|\lambda|^2))\). The deviation between the calculated and the actual value of the conductance is estimated as

\[ \varepsilon = \frac{G_t - G_{\text{calc}}}{\max(G_t) - \min(G_t)} = \frac{G_t - G_{\text{calc}}}{\Delta G_t} \], \hspace{1cm} (10.8)

and it is plotted for the three cases (grounded pair, RC-degenerated pair, and RLC degenerated pair) in Fig. 10.4 - Fig. 10.6. The calculation error using (10.5) is less than \( \pm 5\% \), which can be considered as a sufficient precision given that (10.5) is obtained assuming fully-differential conditions.
B. Positive and negative conductance generated by cross-coupled pair

Fig. 10.4. Grounded cross-coupled-pair oscillator: (a) calculated and simulated $G_t$; (b) relative deviation $\epsilon$ for the estimation of $G_t$.

Fig. 10.5. $RC$-degenerated cross-coupled-pair oscillator: (a) calculated and simulated $G_t$; (b) relative deviation $\epsilon$ for the estimation of $G_t$.

Fig. 10.6. $RLC$-degenerated cross-coupled-pair oscillator: (a) calculated and simulated $G_t$; (b) relative deviation $\epsilon$ for the estimation of $G_t$. 
Bibliography


